# 3.3 VOLT ZERO DELAY LOW SKEW BUFFER ICS2305

## Description

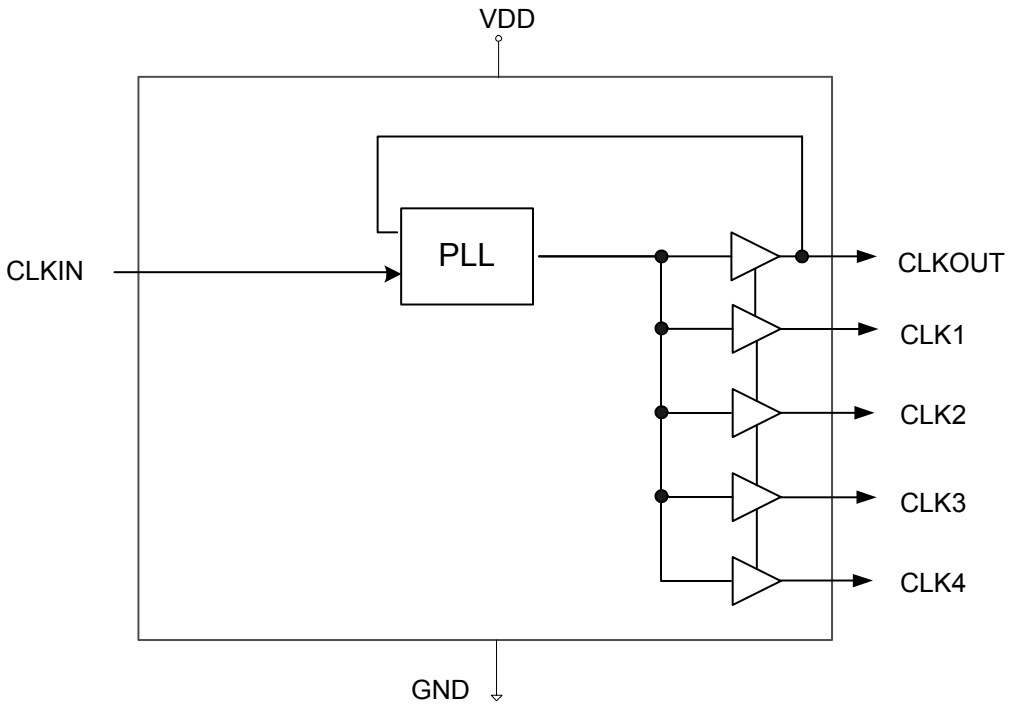
The ICS2305 is a low phase noise, high-speed PLL based, low-skew zero delay buffer. Based on IDT's proprietary low jitter Phase Locked Loop (PLL) techniques, the device provides four low skew outputs at speeds up to 133 MHz at 3.3 V. The outputs can be generated from the PLL (for zero delay), or directly from the input (for testing), and can be set to tri-state mode or to stop at a low level. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

The ICS2305 is available in two different versions. The ICS2305-1 is the base part. The ICS2305-1H is a high drive version with faster rise and fall times.

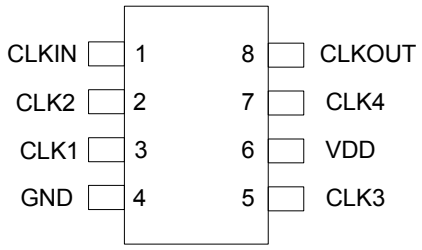
## Features

- Clock outputs from 10 to 133 MHz
- Zero input-output delay
- Four low skew (<250 ps) outputs
- Device-to-device skew <700 ps
- Full CMOS outputs with 25 mA output drive capability at TTL levels
- 5 V tolerant CLKIN
- Tri-state mode for board-level testing
- Advanced, low power, sub-micron CMOS process
- Operating voltage of 3.3 V
- Industrial temperature range available
- Packaged in 8-pin SOIC

## Block Diagram



## Pin Assignment




8 pin ( 150 mil ) SOIC

## Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1 | CLKIN | Input | Clock input (5 V tolerant). |
| 2 | CLK2 | Output | Buffered Clock output 2. |
| 3 | CLK1 | Power | Buffered Clock output 1 |
| 4 | GND | Power | Connect to ground. |
| 5 | CLK3 | Output | Buffered Clock output 3 |
| 6 | VDD | Power | Power supply. Connect to 3.3 V. |
| 7 | CLK4 | Output | Buffered Clock output 4. |
| 8 | CLKOUT | Output | Buffered output. Internall feedback on this pin. |

## External Components

The ICS2305 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01 mF should be connected between VDD and GND on pins 4 and 5, and VDD and GND on pins 13 and 12, as close to the device as possible. A series termination resistor of 33Ω may be used to each clock output pin to reduce reflections.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS2305. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|---|---|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| CLKIN and FBIN inputs | -0.5 V to 5.5 V |
| Electrostatic Discharge (HBM) | 2000 V |
| Ambient Operating Temperature (Commercial) | 0 to +70° C |
| Ambient Operating Temperature (Industrial) | -40 to +85° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 150° C |
| Soldering Temperature | 260° C |

## Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Ambient Operating Temperature (Industrial) | -40 | | +85 | ° C |
| Ambient Operating Temperature (Commercial) | 0 | | +70 | ° C |
| Power Supply Voltage (measured in respect to GND) | +3.0 | | +3.6 | V |

## DC Electrical Characteristics

**ICS2305M-XX**, **VDD = 3.3 V ±10%,** Ambient Temperature -40 to +85° C(Industrial), (0-70° C Commercial)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | | 3.0 | | 3.6 | V |
| Input High Voltage | $V_{IH}$ | | 2 | | | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.8 | V |
| Input Low Current | $I_{IL}$ | VIN = 0V | | | 50 | µA |
| Input High Current | $I_{IH}$ | VIN = VDD | | | 100 | µA |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -12 mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 12 mA | | | 0.4 | V |
| Operating Supply Current | IDD | No Load | | | 32 | mA |
| Power Down Supply Current | | CLKIN = 0, Note 1 | | | 12 | µA |
| Short Circuit Current | $I_{OS}$ | Each output | | ±50 | | mA |
| Input Capacitance | $C_{IN}$ | CLKIN | | 5 | | pF |

Note 1: When there is no clock signal present at CLKIN, the ICS2305 will enter power down mode. The PLL is stopped and the outputs are tri-state.

## AC Electrical Characteristics

**ICS2305M-1**, **VDD=3.3 V ±10%,** Ambient temperature -40 to +85° C(Industrial), (0-70° C Commercial)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Output Clock Frequency | $f_{IN}$ | 10 pF load | 10 | | 133 | MHz |
| Output Clock Frequency | | 30 pF load | 10 | | 100 | MHz |
| Output Rise Time | $t_{OR}$ | 0.8 to 2.0 V, outputs loaded | | | 2.5 | ns |
| Output Fall Time | $t_{OF}$ | 2.0 to 0.8 V, outputs loaded | | | 2.5 | ns |
| Output Clock Duty Cycle | $t_{DC}$ | measured at 1.4V, Fout=66.67 MHz | 40 | 50 | 60 | % |
| Output Clock Duty Cycle | $t_{DC}$ | measured at 1.4V, Fout=50 MHz | 45 | 50 | 55 | % |
| Device to Device Skew | | rising edges at VDD/2 | | | 700 | ps |
| Output to Output Skew | | rising edges at VDD/2 | | | 250 | ps |
| Input to Output Skew | | rising edges at VDD/2 | | | ±350 | ps |
| Cycle to Cycle Jitter | | measured at 66.67M, outputs loaded | | | 200 | ps |
| PLL Lock Time | | Note 2 | | | 1.0 | ms |

Note 2: With VDD at a steady rate and valid input at CLKIN.

**ICS2305M-1H**, **VDD=3.3 V ±10%,** Ambient temperature -40 to +85° C(Industrial), (0-70° C Commercial),

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Output Clock Frequency | $f_{IN}$ | 10 pF load | 10 | | 133 | MHz |
| Output Clock Frequency | | 30 pF load | 10 | | 100 | MHz |
| Output Rise Time | $t_{OR}$ | 0.8 to 2.0 V, outputs loaded | | | 1.5 | ns |
| Output Fall Time | $t_{OF}$ | 2.0 to 0.8 V, outputs loaded | | | 1.5 | ns |
| Output Clock Duty Cycle | $t_{DC}$ | measured at 1.4V, Fout=66.67 MHz | 40 | 50 | 60 | % |
| Output Clock Duty Cycle | $t_{DC}$ | measured at 1.4V, Fout=50 MHz | 45 | 50 | 55 | % |
| Device to Device Skew | | rising edges at VDD/2 | | | 700 | ps |
| Output to Output Skew | | rising edges at VDD/2 | | | 250 | ps |
| Input to Output Skew | | rising edges at VDD/2 | | | ±350 | ps |
| Cycle to Cycle Jitter | | measured at 66.67M, outputs loaded | | | 200 | ps |
| PLL Lock Time | | Note 3 | | | 1.0 | ms |

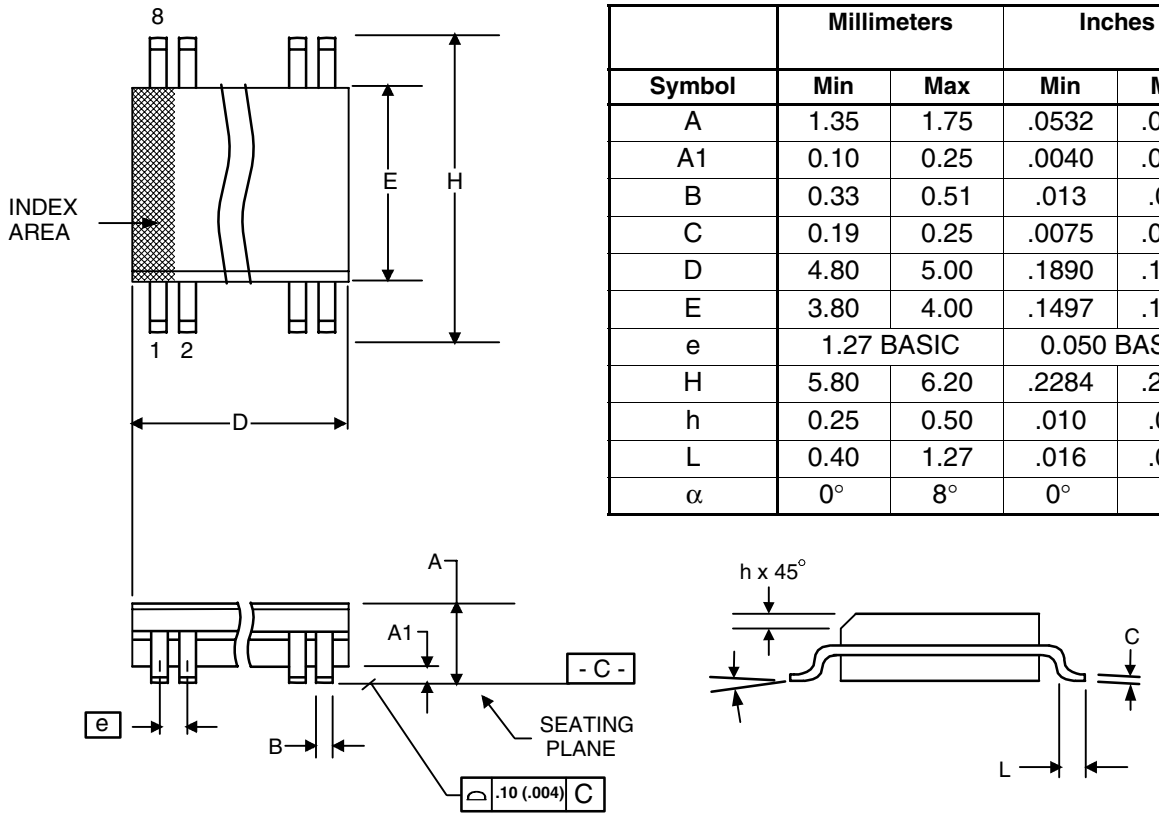
Note 3: With VDD at a steady rate and valid input at CLKIN

## Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air | | 120 | | °C/W |
| | $\theta_{JA}$ | 1 m/s air flow | | 115 | | °C/W |
| | $\theta_{JA}$ | 3 m/s air flow | | 105 | | °C/W |
| Thermal Resistance Junction to Case | $\theta_{JC}$ | | | 58 | | °C/W |

## Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95




| | Millimeters | | Inches | |
|---|---|---|---|---|
| **Symbol** | **Min** | **Max** | **Min** | **Max** |
| A | 1.35 | 1.75 | .0532 | .0688 |
| A1 | 0.10 | 0.25 | .0040 | .0098 |
| B | 0.33 | 0.51 | .013 | .020 |
| C | 0.19 | 0.25 | .0075 | .0098 |
| D | 4.80 | 5.00 | .1890 | .1968 |
| E | 3.80 | 4.00 | .1497 | .1574 |
| e | 1.27 BASIC | | 0.050 BASIC | |
| H | 5.80 | 6.20 | .2284 | .2440 |
| h | 0.25 | 0.50 | .010 | .020 |
| L | 0.40 | 1.27 | .016 | .050 |
| $\alpha$ | 0° | 8° | 0° | 8° |

## Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---|---|---|---|---|
| 2305MI-1LF | 2305MI1L | Tubes | 8-pin SOIC | -40 to +85° C |
| 2305MI-1LFT | 2305MI1L | Tape and Reel | 8-pin SOIC | -40 to +85° C |
| 2305MI-1HLF | 2305I1HL | Tubes | 8-pin SOIC | -40 to +85° C |
| 2305MI-1HLFT | 2305I1HL | Tape and Reel | 8-pin SOIC | -40 to +85° C |
| 2305M-1LF | 2305M1LF | Tubes | 8-pin SOIC | 0 to +70° C |
| 2305M-1LFT | 2305M1LF | Tape and Reel | 8-pin SOIC | 0 to +70° C |
| 2305M-1HLF | 2305M1HL | Tubes | 8-pin SOIC | 0 to +70° C |
| 2305M-1HLFT | 2305M1HL | Tape and Reel | 8-pin SOIC | 0 to +70° C |

“LF” denotes Pb (lead free) package.

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## Revision History

| Rev. | Originator | Date | Description of Change |
|---|---|---|---|
| A | P. Griffith | 12/01/04 | New device/datasheet; Preliminary. |
| B | P. Griffith | 12/27/04 | Made corrections to IDD, IDDP, input capacitance, duty cycle and jitter specs/test conditions. Removed reference to table 2 in output clock frequency test conditions. Removed abslolute and cycle-to-cycle jitter specs for 15 pF load. Added duty cycle spec for Fout=50 MHz. Release from Preliminary to Final. |
| C | P. Griffith | 1/25/05 | Made corrections to test conditions of output rise time, fall-time, duty cycle and cycle-to-cycle jitter. |
| D | J. Sarma | 2/25/05 | Added LF packing info. |
| E | | 08/17/09 | Added EOL note per PDN U-09-01. |
| F | | 05/13/10 | Removed EOL note and non-green orderable parts. |

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