LM5069 Positive High Voltage Hot Swap / Inrush Current Controller with Power Limiting

Check for Samples: LM5069

FEATURES

- **Wide Operating Range: +9V to +80V**
- **In-rush Current Limit for Safe Board Insertion into Live Power Sources**
- **Programmable Maximum Power Dissipation in the External Pass Device**
- **Adjustable Current Limit**
- **Circuit Breaker Function for Severe Over-Current Events**
- **Internal High Side Charge Pump and Gate Driver for External N-channel MOSFET**
- **Adjustable Under-Voltage Lockout (UVLO) and Hysteresis**
- **Adjustable Over-Voltage Lockout (OVLO) and Hysteresis**
- **Initial Insertion Timer Allows Ringing and Transients to Subside after System Connection**
- **Programmable Fault Timer Avoids Nuisance Trips**
- **Active High Open Drain POWER GOOD Output**
- **Available in Latched Fault and Automatic Restart Versions**

APPLICATIONS

- **Server Backplane Systems**
- **Base Station Power Distribution Systems**
- **Solid State Circuit Breaker**
- **24V/48V Industrial Systems**

PACKAGE

- **VSSOP-10**

DESCRIPTION

The LM5069 positive hot swap controller provides intelligent control of the power supply connections during insertion and removal of circuit cards from a live system backplane or other "hot" power sources. The LM5069 provides in-rush current control to limit system voltage droop and transients. The current limit and power dissipation in the external series pass N-Channel MOSFET are programmable, ensuring operation within the Safe Operating Area (SOA). The POWER GOOD output indicates when the output voltage is within 1.25V of the input voltage. The input under-voltage and over-voltage lockout levels and hysteresis are programmable, as well as the initial insertion delay time and fault detection time. The LM5069-1 latches off after a fault detection, while the LM5069-2 automatically restarts at a fixed duty cycle. The LM5069 is available in a 10 pin VSSOP package.

TYPICAL APPLICATION

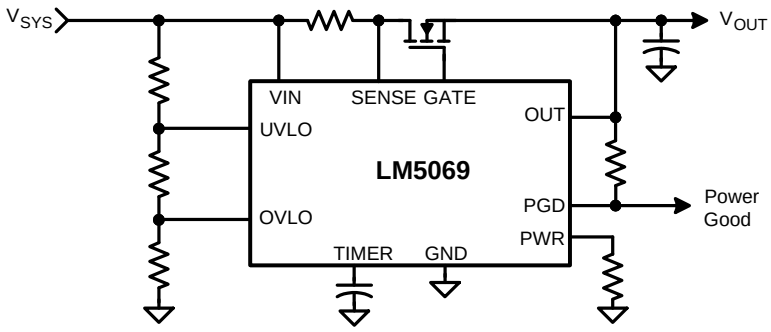


Figure 1. Positive Power Supply Control

CONNECTION DIAGRAM

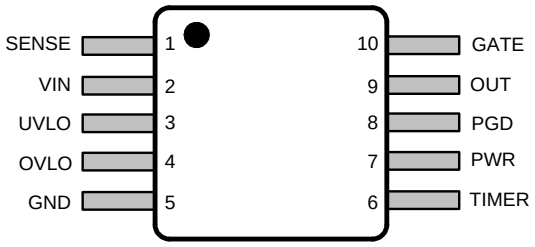


Figure 2. Top View
10-Lead VSSOP

PIN DESCRIPTIONS

Pin #	Name	Description	Applications Information
1	SENSE	Current sense input	The voltage across the current sense resistor (R_S) is measured from VIN to this pin. If the voltage across R_S reaches 55mV the load current is limited and the fault timer activates.
2	VIN	Positive supply input	A small ceramic bypass capacitor close to this pin is recommended to suppress transients which occur when the load current is switched off.
3	UVLO	Under-voltage lockout	An external resistor divider from the system input voltage sets the under-voltage turn-on threshold. An internal 21 µA current source provides hysteresis. The enable threshold at the pin is 2.5V. This pin can also be used for remote shutdown control.
4	OVLO	Over-voltage lockout	An external resistor divider from the system input voltage sets the over-voltage turn-off threshold. An internal 21 µA current source provides hysteresis. The disable threshold at the pin is 2.5V.
5	GND	Circuit ground	
6	TIMER	Timing capacitor	An external capacitor connected to this pin sets the insertion time delay and the Fault Timeout Period. The capacitor also sets the restart timing of the LM5069-2.
7	PWR	Power limit set	An external resistor connected to this pin, in conjunction with the current sense resistor (R_S), sets the maximum power dissipation allowed in the external series pass MOSFET.
8	PGD	Power Good indicator	An open drain output. When the external MOSFET V_{DS} decreases below 1.25V, the PGD indicator is active (high). When the external MOSFET V_{DS} increases above 2.5V the PGD indicator switches low.
9	OUT	Output feedback	Connect to the output rail (external MOSFET source). Internally used to determine the MOSFET V_{DS} voltage for power limiting, and to control the PGD indicator.
10	GATE	Gate drive output	Connect to the external MOSFET's gate. This pin's voltage is typically 12V above the OUT pin when enabled.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

VIN to GND (3)		-0.3V to 100V
SENSE, OUT, PGD to GND		-0.3V to 100V
GATE to GND (3)		-0.3V to 100V
UVLO to GND		-0.3V to 100V
OVLO to GND		-0.3V to 7V
VIN to SENSE		-0.3V to +0.3V
ESD Rating (4)	Human Body Model	2kV
Storage Temperature		-65°C to +150°C
Junction Temperature		+150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and conditions see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The GATE pin voltage is typically 12V above VIN when the LM5069 is enabled. Therefore the Absolute Maximum Ratings for VIN (100V) applies only when the LM5069 is disabled, or for a momentary surge to that voltage since the Absolute Maximum Rating for the GATE pin is also 100V.
(4) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

OPERATING RATINGS (1)

VIN Supply Voltage	+9.0V to 80V
PGD Off Voltage	0V to 80V
Junction Temp. Range	−40°C to +125°C

(1) For detailed information on soldering plastic VSSOP packages refer to the SNOA549 available from Texas Instruments.

ELECTRICAL CHARACTERISTICS

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN = 48V.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Input (VIN pin)						
I_{IN-EN}	Input Current, enabled	UVLO > 2.5V and OVLO < 2.5V		1.3	**1.6**	mA
I_{IN-DIS}	Input Current, disabled	UVLO <2.5V or OVLO >2.5V		480	**650**	µA
POR_{IT}	Power On Reset threshold at VIN to trigger insertion timer	VIN Increasing		7.6	**8.0**	V
POR_{EN}	Power On Reset threshold at VIN to enable all functions	VIN increasing		8.4	**9.0**	V
POR_{EN-HYS}	POR_{EN} hysteresis	VIN decreasing		90		mV
OUT pin						
I_{OUT-EN}	OUT bias current, enabled	OUT = VIN, Normal operation		11		µA
$I_{OUT-DIS}$	OUT bias current, disabled (1)	Disabled, OUT = 0V, SENSE = VIN		50		
UVLO, OVLO pins						
$UVLO_{TH}$	UVLO threshold		**2.45**	2.5	**2.55**	V
$UVLO_{HYS}$	UVLO hysteresis current	UVLO = 1V	**12**	21	**30**	µA
$UVLO_{DEL}$	UVLO delay	Delay to GATE high		55		µs
		Delay to GATE low		11		
$UVLO_{BIAS}$	UVLO bias current	UVLO = 48V			**1**	µA
$OVLO_{TH}$	OVLO threshold		**2.40**	2.5	**2.60**	V
$OVLO_{HYS}$	OVLO hysteresis current	OVLO = 2.6V	**12**	21	**30**	µA

(1) OUT bias current (disabled) due to leakage current through an internal 1.0 MΩ resistance from SENSE to VOUT.

ELECTRICAL CHARACTERISTICS (continued)

Limits in standard type are for T_J = 25°C only; limits in boldface type apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN = 48V.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$OVLO_{DEL}$	OVLO delay	Delay to GATE high		55		µs
		Delay to GATE low		11		
$OVLO_{BIAS}$	OVLO bias current	OVLO = 2.4V			**1**	µA
Power Limit (PWR pin)						
PWR_{LIM-1}	Power limit sense voltage (VIN-SENSE)	SENSE-OUT = 48V, R_{PWR} = 150 kΩ	**19**	25	**31**	mV
PWR_{LIM-2}		SENSE-OUT = 24V, R_{PWR} = 75 kΩ		25		mV
I_{PWR}	PWR pin current	V_{PWR} = 2.5V		20		µA
Gate Control (GATE pin)						
I_{GATE}	Source current	Normal Operation, GATE-OUT = 5V	**10**	16	**22**	µA
	Sink current	UVLO < 2.5V	**1.75**	2	**2.6**	mA
		VIN - SENSE = 150 mV or VIN < POR_{IT}, V_{GATE} = 5V	**45**	110	**175**	mA
V_{GATE}	Gate output voltage in normal operation	GATE-OUT voltage	**11.4**	12	**12.6**	V
Current Limit						
V_{CL}	Threshold voltage	VIN-SENSE voltage	**48.5**	55	**61.5**	mV
t_{CL}	Response time	VIN-SENSE stepped from 0 mV to 80 mV		45		µs
I_{SENSE}	SENSE input current	Enabled, SENSE = OUT		23		µA
		Disabled, OUT = 0V		60		
Circuit Breaker						
V_{CB}	Threshold voltage	VIN - SENSE	**80**	105	**130**	mV
t_{CB}	Response time	VIN - SENSE stepped from 0 mV to 150 mV, time to GATE low, no load		0.44	**1.2**	µs
Timer (TIMER pin)						
V_{TMRH}	Upper threshold		**3.76**	4	**4.16**	V
V_{TMRL}	Lower threshold	Restart cycles (LM5069-2)	**1.187**	1.25	**1.313**	V
		End of 8th cycle (LM5069-2)		0.3		V
		Re-enable Threshold (LM5069-1)		0.3		V
I_{TIMER}	Insertion time current		**3**	5.5	**8**	µA
	Sink current, end of insertion time	TIMER pin = 2V	**1.0**	1.5	**2.0**	mA
	Fault detection current		**51**	85	**120**	µA
	Fault sink current		**1.25**	2.5	**3.75**	µA
DC_{FAULT}	Fault Restart Duty Cycle	LM5069-2 only		0.5		%
t_{FAULT}	Fault to GATE low delay	TIMER pin reaches 4.0V		12		µs
Power Good (PGD pin)						
PGD_{TH}	Threshold measured at SENSE-OUT	Decreasing	**0.67**	1.25	**1.85**	V
		Increasing, relative to decreasing threshold	**0.95**	1.25	**1.55**	
PGD_{VOL}	Output low voltage	I_{SINK} = 2 mA		60	**150**	mV
PGD_{IOH}	Off leakage current	V_{PGD} = 80V			**5**	µA

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified the following conditions apply: T_J = 25°C, V_{IN} = 48V

VIN Pin Input Current vs. VIN

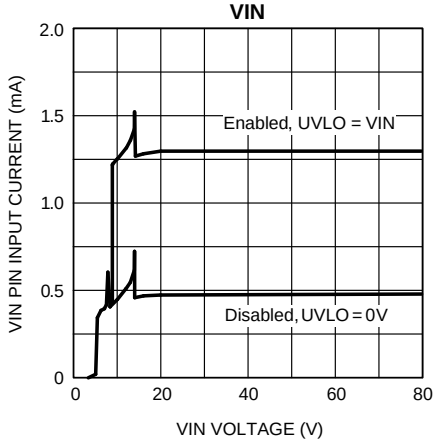


Figure 3.

SENSE Pin Input Current

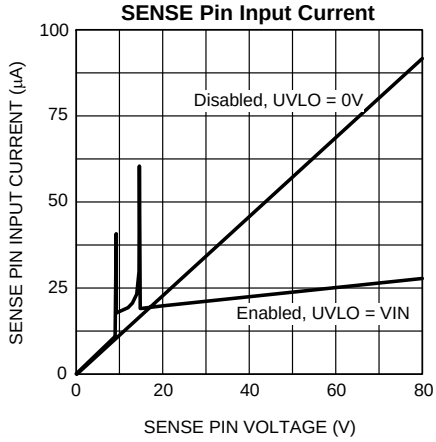


Figure 4.

OUT Pin Current

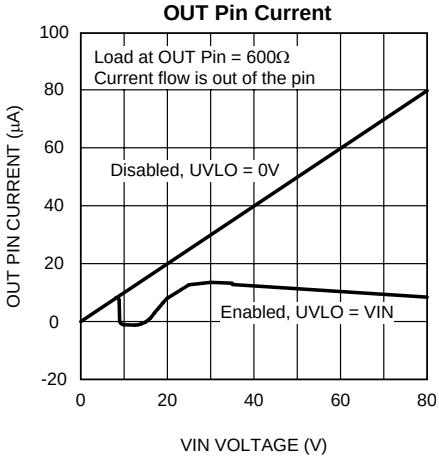


Figure 5.

GATE Pin Voltage vs. V_{IN}

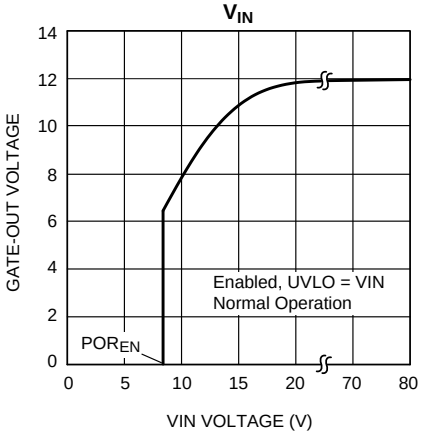


Figure 6.

GATE Pin Source Current vs. V_{IN}

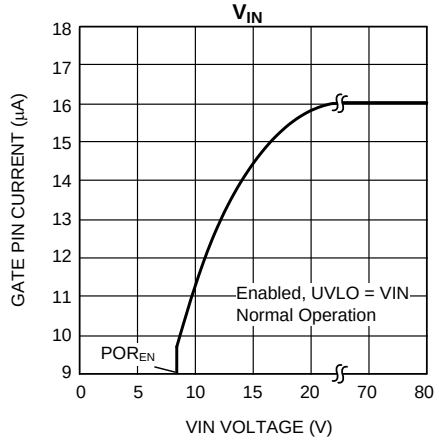


Figure 7.

PGD Pin Low Voltage vs. Sink Current

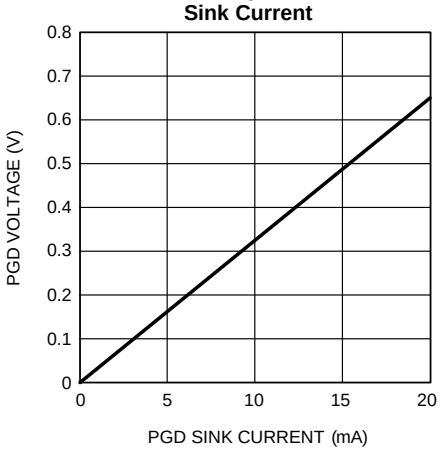


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified the following conditions apply: T_J = 25°C, V_{IN} = 48V

MOSFET Power Dissipation Limit vs. R_{PWR} and R_S

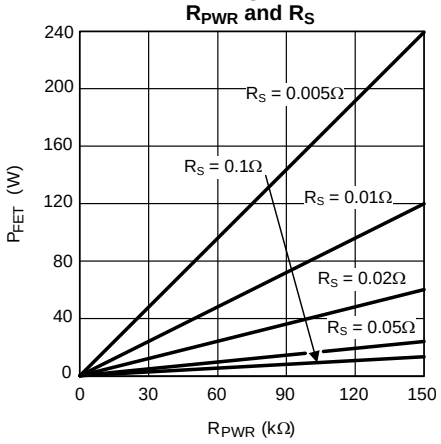


Figure 9.

GATE Pull-Down Current, Circuit Breaker vs GATE Voltage

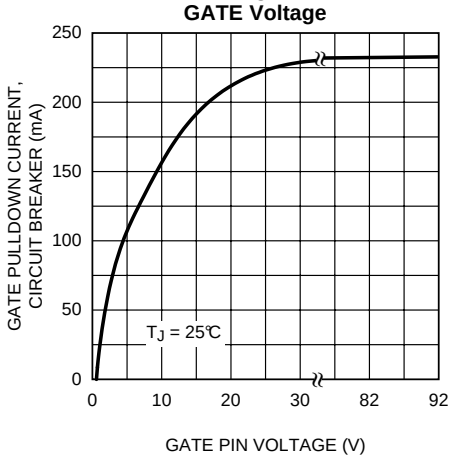


Figure 10.

UVLO Hysteresis Current vs. Temperature

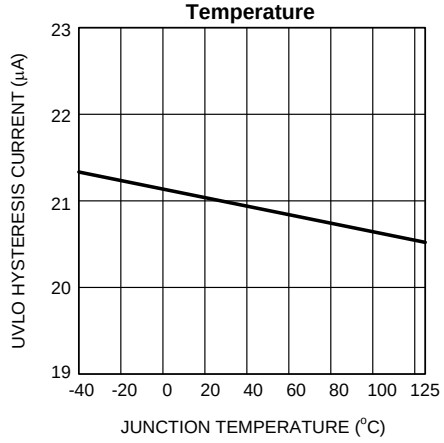


Figure 11.

OVLO Hysteresis Current vs. Temperature

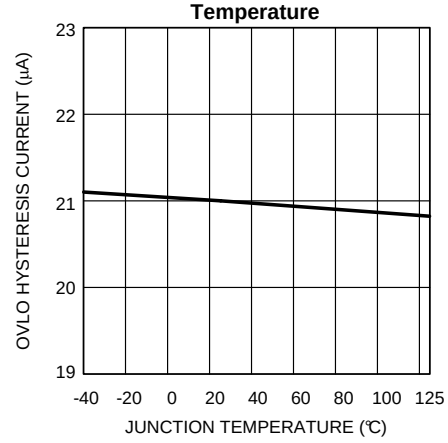


Figure 12.

UVLO, OVLO Threshold vs. Temperature

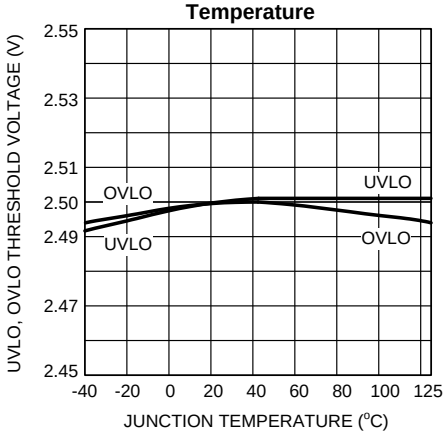


Figure 13.

Input Current, Enabled vs. Temperature

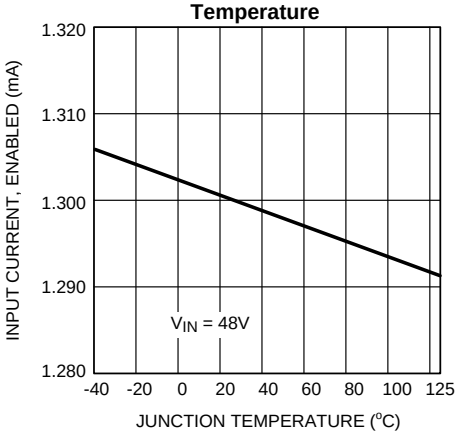


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified the following conditions apply: T_J = 25°C, V_{IN} = 48V

Current Limit Threshold vs. Temperature

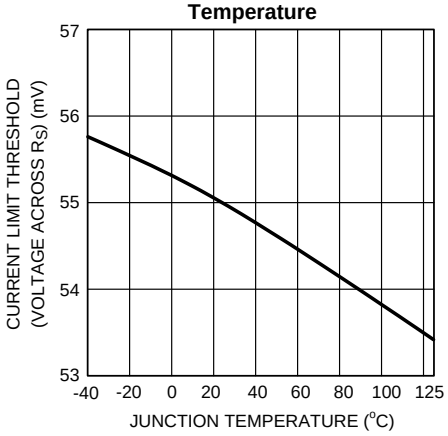


Figure 15.

Circuit Breaker Threshold vs. Temperature

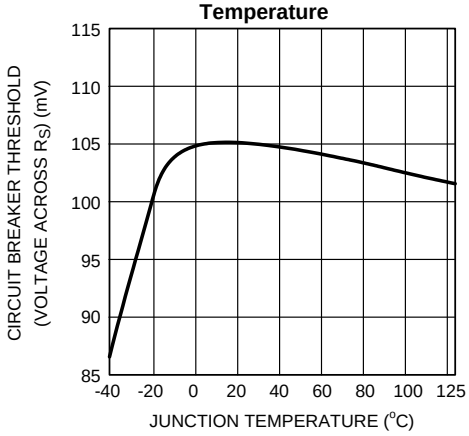


Figure 16.

Power Limit Threshold vs. Temperature

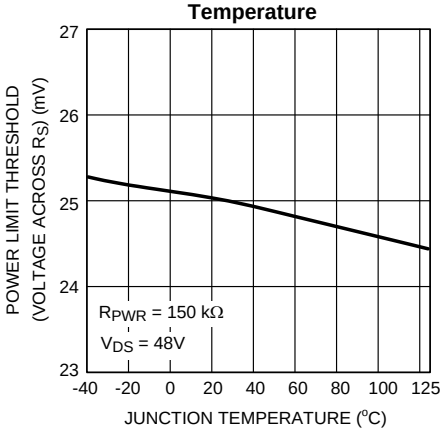


Figure 17.

GATE Output Voltage vs. Temperature

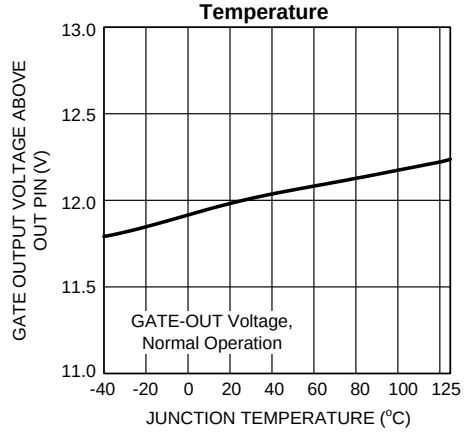


Figure 18.

GATE Source Current vs. Temperature

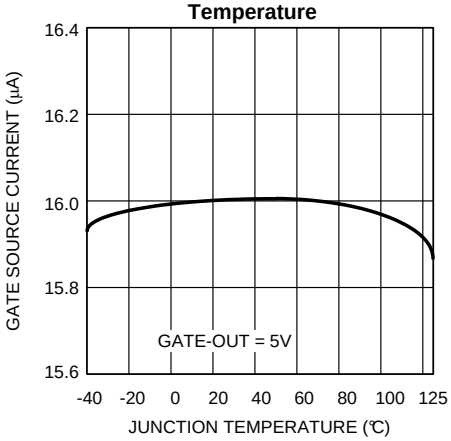


Figure 19.

GATE Pull-Down Current, Circuit Breaker vs. Temperature

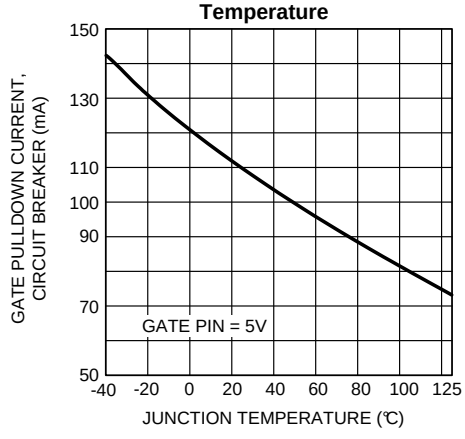


Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified the following conditions apply: T_J = 25°C, V_{IN} = 48V

PGD Low Voltage vs. Temperature

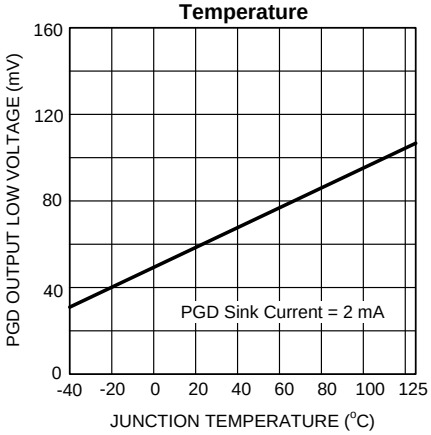
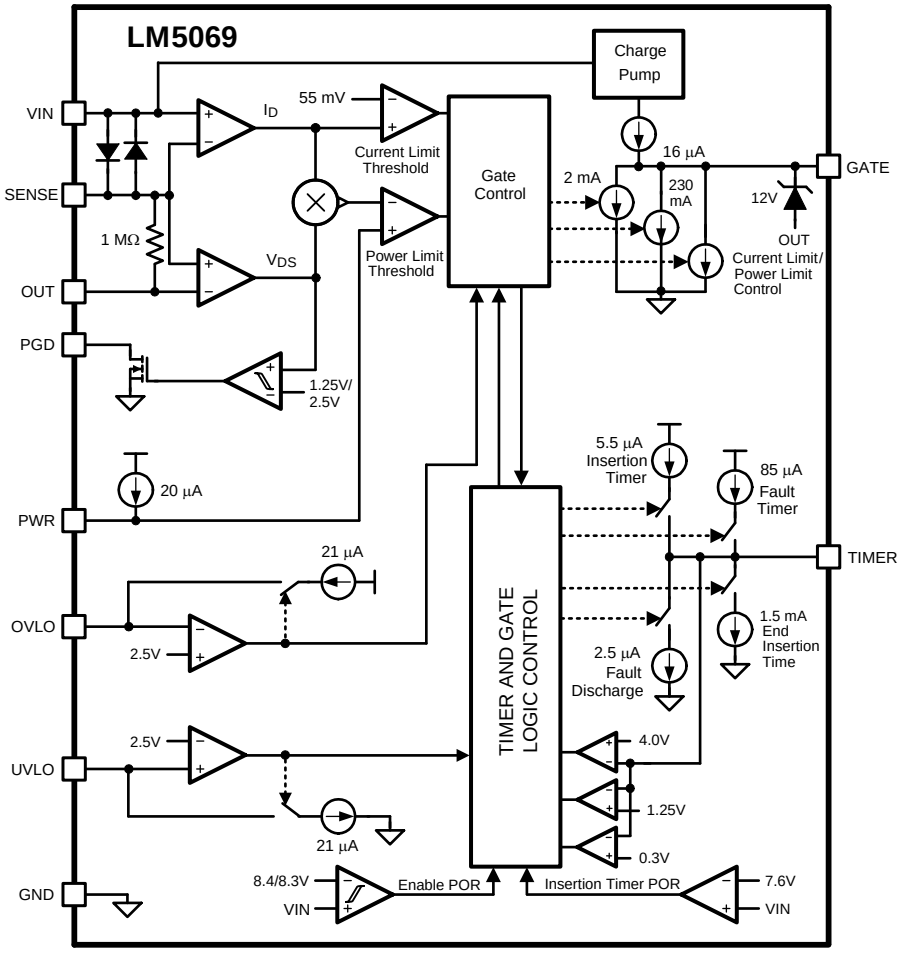


Figure 21.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

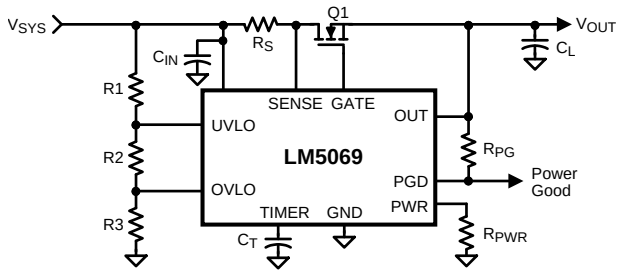


Figure 22. Basic Application Circuit

The LM5069 is designed to control the in-rush current to the load upon insertion of a circuit card into a live backplane or other "hot" power source, thereby limiting the voltage sag on the backplane's supply voltage, and the dV/dt of the voltage applied to the load. Effects on other circuits in the system are minimized, preventing possible unintended resets. A controlled shutdown when the circuit card is removed can also be implemented using the LM5069. In addition to a programmable current limit, the LM5069 monitors and limits the maximum power dissipation in the series pass device to maintain operation within the device Safe Operating Area (SOA). Either current limiting or power limiting for an extended period of time results in the shutdown of the series pass device. In this event, the LM5069-1 latches off until the circuit is re-enabled by external control, while the LM5069-2 automatically restarts with defined timing. The circuit breaker function quickly switches off the series pass device upon detection of a severe over-current condition. The Power Good (PGD) output pin indicates when the output voltage is within 1.25V of the system input voltage (V_{SYS}). Programmable under-voltage lock-out (UVLO) and over-voltage lock-out (OVLO) circuits shut down the LM5069 when the system input voltage is outside the desired operating range. The typical configuration of a circuit card with LM5069 hot swap protection is shown in Figure 23.

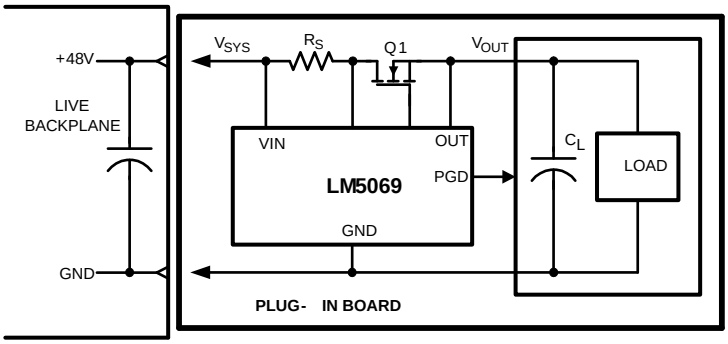


Figure 23. LM5069 Application

Power Up Sequence

The VIN operating range of the LM5069 is +9V to +80V, with a transient capability to +100V. Referring to the Block Diagram and Figure 22 and Figure 24, as the voltage at VIN initially increases, the external N-channel MOSFET (Q1) is held off by an internal 230 mA pull-down current at the GATE pin. The strong pull-down current at the GATE pin prevents an inadvertent turn-on as the MOSFET's gate-to-drain (Miller) capacitance is charged. Additionally, the TIMER pin is initially held at ground. When the VIN voltage reaches the POR_{IT} threshold (7.6V) the insertion time begins. During the insertion time, the capacitor at the TIMER pin (C_T) is charged by a 5.5 µA current source, and Q1 is held off by a 2 mA pull-down current at the GATE pin regardless of the VIN voltage. The insertion time delay allows ringing and transients at VIN to settle before Q1 can be enabled. The insertion time ends when the TIMER pin voltage reaches 4.0V. C_T is then quickly discharged by an internal 1.5 mA pull-down current. After the insertion time, the LM5069 control circuitry is enabled when VIN reaches the POR_{EN} threshold (8.4V). The GATE pin then switches on Q1 when V_{SYS} exceeds the UVLO threshold (UVLO pin >2.5V). If V_{SYS} is above the UVLO threshold at the end of the insertion time, Q1 switches on at that time. The GATE pin charge pump sources 16 µA to charge Q1's gate capacitance. The maximum gate-to-source voltage of Q1 is limited by an internal 12V zener diode.

As the voltage at the OUT pin increases, the LM5069 monitors the drain current and power dissipation of MOSFET Q1. In-rush current limiting and/or power limiting circuits actively control the current delivered to the load. During the in-rush limiting interval (t2 in Figure 24) an internal 85 µA fault timer current source charges C_T. If Q1's power dissipation and the input current reduce below their respective limiting thresholds before the TIMER pin reaches 4.0V the 85 µA current source is switched off, and C_T is discharged by the internal 2.5 µA current sink (t3 in Figure 24). The in-rush limiting interval is complete when the voltage at the OUT pin increases to within 1.25V of the input voltage (V_{SYS}), and the PGD pin switches high.

If the TIMER pin voltage reaches 4.0V before in-rush current limiting or power limiting ceases (during t2), a fault is declared and Q1 is turned off. See the Fault Timer & Restart section for a complete description of the fault mode.

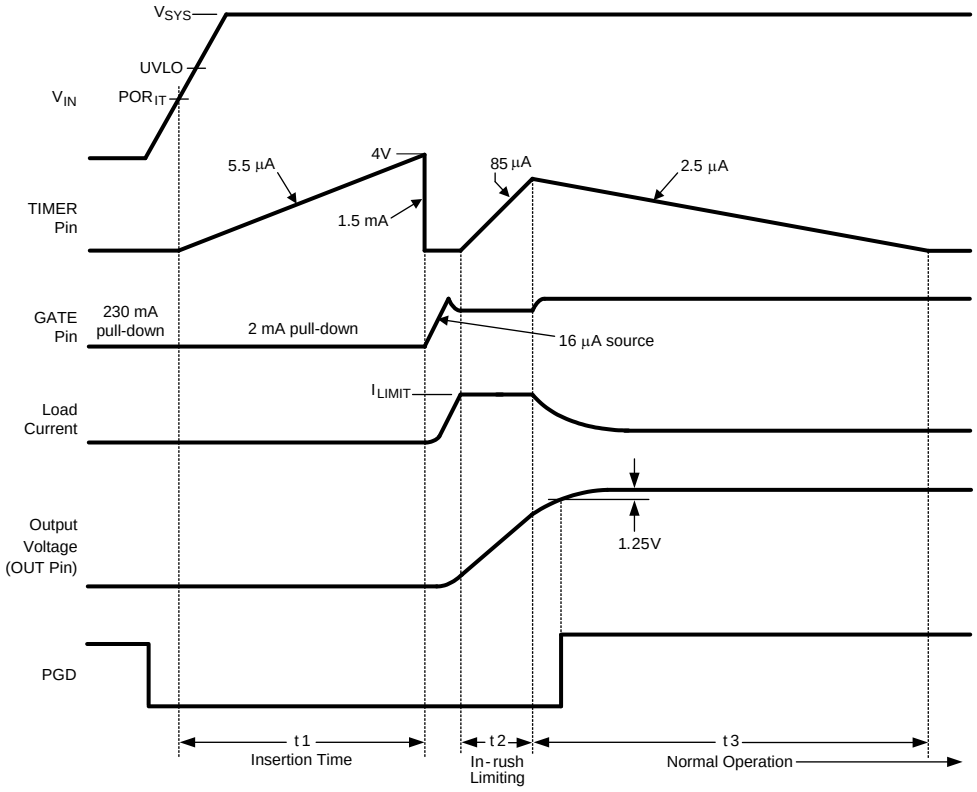


Figure 24. Power Up Sequence (Current Limit only)

Gate Control

A charge pump provides internal bias voltage above the output voltage (OUT pin) to enhance the N-Channel MOSFET's gate. The gate-to-source voltage is limited by an internal 12V zener diode. During normal operating conditions (t3 in Figure 24) the gate of Q1 is held charged by an internal 16 µA current source to approximately 12V above OUT. If the maximum V_{GS} rating of Q1 is less than 12V, a lower voltage external zener diode must be added between the GATE and OUT pins. The external zener diode must have a forward current rating of at least 250 mA.

When the system voltage is initially applied, the GATE pin is held low by a 230 mA pull-down current. This helps prevent an inadvertent turn-on of the MOSFET through its drain-gate capacitance as the applied system voltage increases.

During the insertion time (t1 in Figure 24) the GATE pin is held low by a 2 mA pull-down current. This maintains Q1 in the off-state until the end of t1, regardless of the voltage at VIN or UVLO.

Following the insertion time, during t2 in Figure 24, the gate voltage of Q1 is modulated to keep the current or power dissipation level from exceeding the programmed levels. While in the current or power limiting mode the TIMER pin capacitor is charging. If the current and power limiting cease before the TIMER pin reaches 4V the TIMER pin capacitor then discharges, and the circuit enters normal operation.

If the in-rush limiting condition persists such that the TIMER pin reached 4V during t2, the GATE pin is then pulled low by the 2 mA pull-down current. The GATE pin is then held low until either a power up sequence is initiated (LM5069-1), or until the end of the restart sequence (LM5069-2). See the Fault Timer & Restart section.

If the system input voltage falls below the UVLO threshold, or rises above the OVLO threshold, the GATE pin is pulled low by the 2 mA pull-down current to switch off Q1.

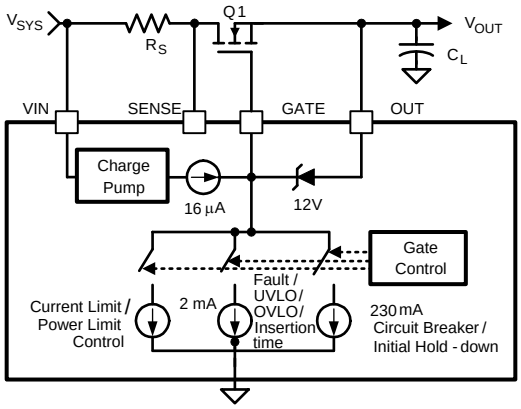


Figure 25. Gate Control

Current Limit

The current limit threshold is reached when the voltage across the sense resistor R_S (VIN to SENSE) reaches 55 mV. In the current limiting condition, the GATE voltage is controlled to limit the current in MOSFET Q1. While the current limit circuit is active, the fault timer is active as described in the Fault Timer & Restart section. If the load current falls below the current limit threshold before the end of the Fault Timeout Period, the LM5069 resumes normal operation. For proper operation, the R_S resistor value should be no larger than 100 mΩ.

Circuit Breaker

If the load current increases rapidly (e.g., the load is short-circuited) the current in the sense resistor (R_S) may exceed the current limit threshold before the current limit control loop is able to respond. If the current exceeds twice the current limit threshold (105 mV/R_S), Q1 is quickly switched off by the 230 mA pull-down current at the GATE pin, and a Fault Timeout Period begins. When the voltage across R_S falls below 105 mV the 230 mA pull-down current at the GATE pin is switched off, and the gate voltage of Q1 is then determined by the current limit or the power limit functions. If the TIMER pin reaches 4.0V before the current limiting or power limiting condition ceases, Q1 is switched off by the 2 mA pull-down current at the GATE pin as described in the Fault Timer & Restart section.

Power Limit

An important feature of the LM5069 is the MOSFET power limiting. The Power Limit function can be used to maintain the maximum power dissipation of MOSFET Q1 within the device SOA rating. The LM5069 determines the power dissipation in Q1 by monitoring its drain-source voltage (SENSE to OUT), and the drain current through the sense resistor (VIN to SENSE). The product of the current and voltage is compared to the power limit threshold programmed by the resistor at the PWR pin. If the power dissipation reaches the limiting threshold, the GATE voltage is modulated to reduce the current in Q1. While the power limiting circuit is active, the fault timer is active as described in the Fault Timer & Restart section.

Fault Timer & Restart

When the current limit or power limit threshold is reached during turn-on or as a result of a fault condition, the gate-to-source voltage of Q1 is modulated to regulate the load current and power dissipation. When either limiting function is activated, an 85 µA fault timer current source charges the external capacitor (C_T) at the TIMER pin as shown in Figure 27 (Fault Timeout Period). If the fault condition subsides during the Fault Timeout Period before the TIMER pin reaches 4.0V, the LM5069 returns to the normal operating mode and C_T is discharged by the 2.5 µA current sink. If the TIMER pin reaches 4.0V during the Fault Timeout Period, Q1 is switched off by a 2 mA pull-down current at the GATE pin. The subsequent restart procedure then depends on which version of the LM5069 is in use.

The LM5069-1 latches the GATE pin low at the end of the Fault Timeout Period. C_T is then discharged to ground by the 2.5 µA fault current sink. The GATE pin is held low by the 2 mA pull-down current until a power up sequence is externally initiated by cycling the input voltage (V_{SYS}), or momentarily pulling the UVLO pin below 2.5V with an open-collector or open-drain device as shown in Figure 26. The voltage at the TIMER pin must be <0.3V for the restart procedure to be effective.

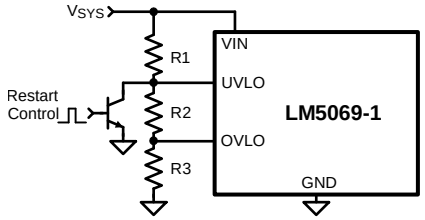


Figure 26. Latched Fault Restart Control

The LM5069-2 provides an automatic restart sequence which consists of the TIMER pin cycling between 4.0V and 1.25V seven times after the Fault Timeout Period, as shown in Figure 27. The period of each cycle is determined by the 85 µA charging current, and the 2.5 µA discharge current, and the value of the capacitor C_T. When the TIMER pin reaches 0.3V during the eighth high-to-low ramp, the 16 µA current source at the GATE pin turns on Q1. If the fault condition is still present, the Fault Timeout Period and the restart cycle repeat.

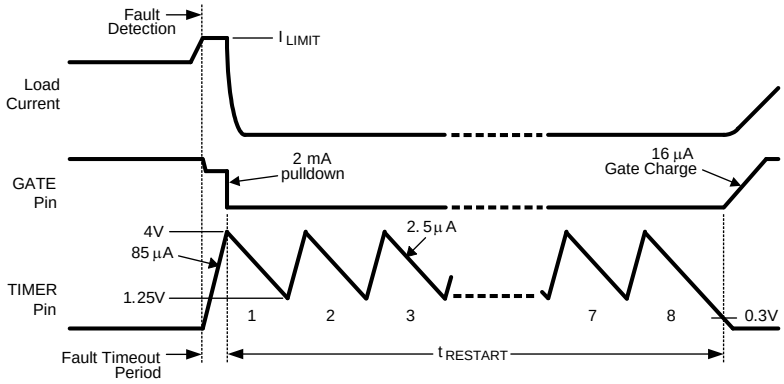


Figure 27. Restart Sequence (LM5069-2)

Under-Voltage Lock-Out (UVLO)

The series pass MOSFET (Q1) is enabled when the input supply voltage (V_{SYS}) is within the operating range defined by the programmable under-voltage lockout (UVLO) and over-voltage lock-out (OVLO) levels. Typically the UVLO level at V_{SYS} is set with a resistor divider (R1-R3) as shown in Figure 22. When V_{SYS} is below the UVLO level, the internal 21 µA current source at UVLO is enabled, the current source at OVLO is off, and Q1 is held off by the 2 mA pull-down current at the GATE pin. As V_{SYS} is increased, raising the voltage at UVLO above 2.5V, the 21 µA current source at UVLO is switched off, increasing the voltage at UVLO, providing hysteresis for this threshold. With the UVLO pin above 2.5V, Q1 is switched on by the 16 µA current source at the GATE pin if the insertion time delay has expired (Figure 24). See the Applications Section for a procedure to calculate the values of the threshold setting resistors (R1-R3). The minimum possible UVLO level at V_{SYS} can be set by connecting the UVLO pin to VIN. In this case Q1 is enabled when the VIN voltage reaches the POR_{EN} threshold.

Over-Voltage Lock-Out (OVLO)

The series pass MOSFET (Q1) is enabled when the input supply voltage (V_{SYS}) is within the operating range defined by the programmable under-voltage lockout (UVLO) and over-voltage lock-out (OVLO) levels. If V_{SYS} raises the OVLO pin voltage above 2.5V Q1 is switched off by the 2 mA pull-down current at the GATE pin, denying power to the load. When the OVLO pin is above 2.5V, the internal 21 µA current source at OVLO is switched on, raising the voltage at OVLO to provide threshold hysteresis. When V_{SYS} is reduced below the OVLO level Q1 is enabled. See the Applications Section for a procedure to calculate the threshold setting resistor values.

Shutdown Control

The load current can be remotely switched off by taking the UVLO pin below its 2.5V threshold with an open collector or open drain device, as shown in Figure 28. Upon releasing the UVLO pin the LM5069 switches on the load current with in-rush current and power limiting.

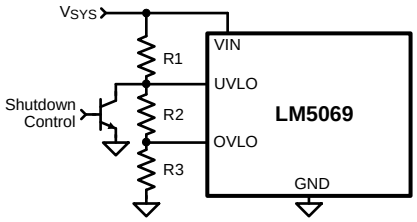


Figure 28. Shutdown Control

Power Good Pin

The Power Good indicator pin (PGD) is connected to the drain of an internal N-channel MOSFET capable of sustaining 80V in the off-state, and transients up to 100V. An external pull-up resistor is required at PGD to an appropriate voltage to indicate the status to downstream circuitry. The off-state voltage at the PGD pin can be higher or lower than the voltages at VIN and OUT. PGD is switched high when the voltage from SENSE to OUT (the external MOSFET's V_{DS}) decreases below 1.25V. PGD switches low when the MOSFET's V_{DS} is increased past 2.5V. If the UVLO pin is taken below 2.5V, or the OVLO pin taken above 2.5V, to disable the LM5069, PGD switches low within 10 µs without waiting for the voltage at OUT to fall 2.5V below the voltage at SENSE. The PGD output pin is high when the voltage at VIN is less than 5V.

APPLICATION INFORMATION

(REFER TO Figure 22)

CURRENT LIMIT, R_S

The LM5069 monitors the current in the external MOSFET (Q1) by measuring the voltage across the sense resistor (R_S), connected from VIN to SENSE. The required resistor value is calculated from:

$$R_S = \frac{55\ mV}{I_{LIM}} \quad (1)$$

where I_{LIM} is the desired current limit threshold. If the voltage across R_S reaches 55 mV, the current limit circuit modulates the gate of Q1 to regulate the current at I_{LIM}. While the current limiting circuit is active, the fault timer is active as described in the Fault Timer & Restart section. For proper operation, R_S must be no larger than 100 mΩ.

While the maximum load current in normal operation can be used to determine the required power rating for resistor R_S, basing it on the current limit value provides a more reliable design since the circuit can operate near the current limit threshold continuously. The resistor's surge capability must also be considered since the circuit breaker threshold is twice the current limit threshold. Connections from R_S to the LM5069 should be made using Kelvin techniques. In the suggested layout of Figure 29 the small pads at the lower corners of the sense resistor connect only to the sense resistor terminals, and not to the traces carrying the high current. With this technique, only the voltage across the sense resistor is applied to VIN and SENSE, eliminating the voltage drop across the high current solder connections.

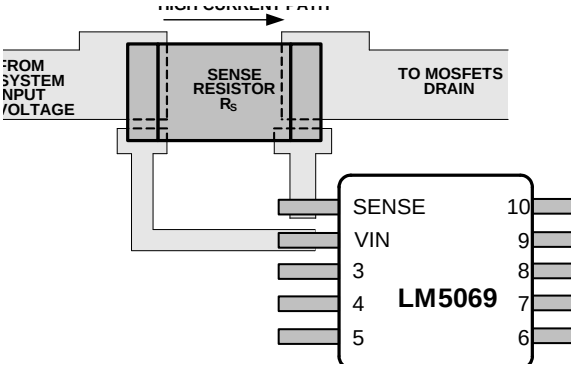


Figure 29. Sense Resistor Connections

POWER LIMIT THRESHOLD

The LM5069 determines the power dissipation in the external MOSFET (Q1) by monitoring the drain current (the current in R_S), and the V_{DS} of Q1 (SENSE to OUT pins). The resistor at the PWR pin (R_{PWR}) sets the maximum power dissipation for Q1, and is calculated from the following equation:

$$R_{PWR} = 1.25 \times 10^5 \times R_S \times P_{FET(LIM)} \quad (2)$$

where $P_{FET(LIM)}$ is the desired power limit threshold for Q1, and R_S is the current sense resistor described in the Current Limit section. For example, if R_S is 10 mΩ , and the desired power limit threshold is 60W, R_{PWR} calculates to 75 kΩ. If Q1's power dissipation reaches the threshold Q1's gate is modulated to reduce the load current, keeping Q1's power from exceeding the threshold. For proper operation of the power limiting feature, R_{PWR} must be ≤150 kΩ. While the power limiting circuit is active, the fault timer is active as described in the Fault Timer & Restart section. Typically, power limit is reached during startup, or if the output voltage falls due to a severe overload or short circuit.

The programmed maximum power dissipation should have a reasonable margin from the maximum power defined by the FET's SOA chart if the LM5069-2 is used since the FET will be repeatedly stressed during fault restart cycles. The FET manufacturer should be consulted for guidelines.

If the application does not require use of the power limit function the PWR pin can be left open.

TURN-ON TIME

The output turn-on time depends on whether the LM5069 operates in current limit, or in both power limit and current limit, during turn-on.

A) Turn-on with current limit only: The current limit threshold (I_{LIM}) is determined by the current sense resistor (R_S). If the current limit threshold is less than the current defined by the power limit threshold at maximum V_{DS} the circuit operates at the current limit threshold only during turn-on. Referring to Figure 32a, as the load current reaches I_{LIM}, the gate-to-source voltage is controlled at V_{GSL} to maintain the current at I_{LIM}. As the output voltage reaches its final value (V_{DS} ≅ 0V) the drain current reduces to its normal operating value, and the gate is charged to approximately 12V (V_{GATE}). The time for the OUT pin voltage to transition from zero volts to V_{SYS} is equal to:

$$t_{ON} = \frac{V_{SYS} \times C_L}{I_{LIM}}$$

where C_L is the load capacitance. For example, if V_{SYS} = 48V, C_L = 1000 µF, and I_{LIM} = 1A, t_{ON} calculates to 48 ms. The maximum instantaneous power dissipated in the MOSFET is 48W. This calculation assumes the time from t1 to t2 in Figure 32a is small compared to t_{ON}, and the load does not draw any current until after the output voltage has reached its final value, and PGD switches high (Figure 30). If the load draws current during the turn-on sequence (Figure 31), the turn-on time is longer than the above calculation, and is approximately equal to:

$$t_{ON} = -(R_L \times C_L) \times \ln\left[\frac{(I_{LIM} \times R_L) - V_{SYS}}{(I_{LIM} \times R_L)}\right]$$

where R_L is the load resistance. The Fault Timeout Period must be set longer than t_{ON} to prevent a fault shutdown before the turn-on sequence is complete.

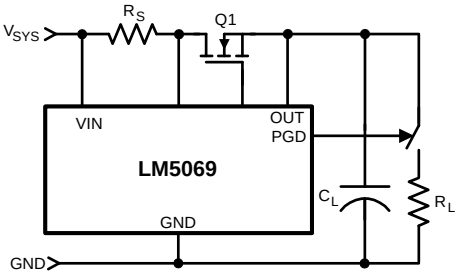


Figure 30. No Load Current During Turn-On

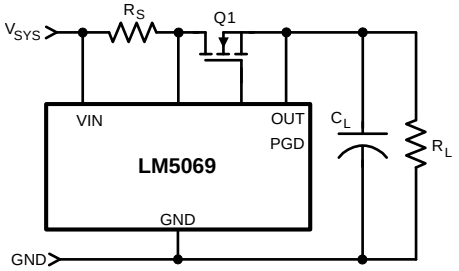


Figure 31. Load Draws Current During Turn-On

B) Turn-on with power limit and current limit: The maximum allowed power dissipation in Q1 ($P_{FET(LIM)}$) is defined by the resistor at the PWR pin, and the current sense resistor R_S. See the Power Limit Threshold section. If the current limit threshold (I_{LIM}) is higher than the current defined by the power limit threshold at maximum V_{DS} ($P_{FET(LIM)}/V_{SYS}$) the circuit operates initially at the power limit mode when the V_{DS} of Q1 is high, and then transitions to current limit mode as the current increases to I_{LIM} and V_{DS} decreases. See Figure 32ab. Assuming the load (R_L) is not connected during turn-on, the time for the output voltage to reach its final value is approximately equal to:

$$t_{ON} = \frac{C_L \times V_{SYS}^2}{2 \times P_{FET(LIM)}} + \frac{C_L \times P_{FET(LIM)}}{2 \times I_{LIM}^2}$$

For example, if V_{SYS} = 48V, C_L = 1000 µF, I_{LIM} = 1A, and $P_{FET(LIM)}$ = 20W, t_{ON} calculates to ≅68 ms, and the initial current level (I_P) is approximately 0.42A. The Fault Timeout Period must be set longer than t_{ON}.

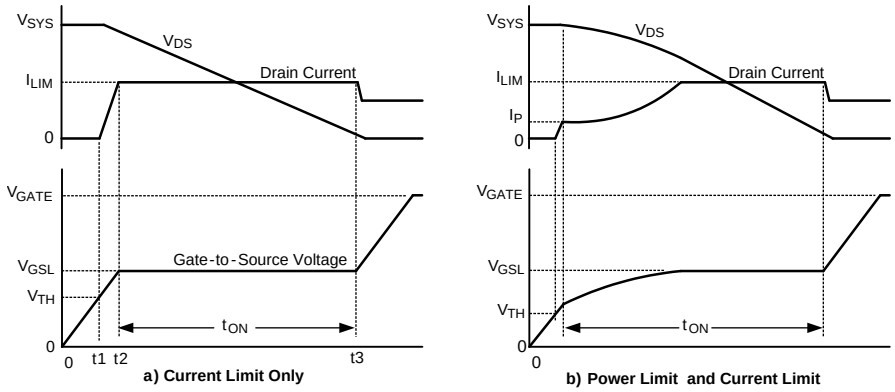


Figure 32. MOSFET Power Up Waveforms

MOSFET SELECTION

It is recommended that the external MOSFET (Q1) selection be based on the following criteria:

- The BV_{DSS} rating should be greater than the maximum system voltage (V_{SYS}), plus ringing and transients which can occur at V_{SYS} when the circuit card, or adjacent cards, are inserted or removed.

- The maximum continuous current rating should be based on the current limit threshold (55 mV/R_S), not the maximum load current, since the circuit can operate near the current limit threshold continuously.

- The Pulsed Drain Current spec (I_{DM}) must be greater than the current threshold for the circuit breaker function (105 mV/R_S).

- The SOA (Safe Operating Area) chart of the device, and the thermal properties, should be used to determine the maximum power dissipation threshold set by the R_{PWR} resistor. The programmed maximum power dissipation should have a reasonable margin from the maximum power defined by the FET's SOA chart if the LM5069-2 is used since the FET will be repeatedly stressed during fault restart cycles. The FET manufacturer should be consulted for guidelines.

- $R_{DS(on)}$ should be sufficiently low that the power dissipation at maximum load current ($I_{L(max)}^2$ x $R_{DS(on)}$) does not raise its junction temperature above the manufacturer's recommendation.

If the device chosen for Q1 has a maximum V_{GS} rating less than 12V, an external zener diode must be added from its gate to source, with the zener voltage less than the maximum V_{GS} rating. The zener diode's forward current rating must be at least 250 mA to conduct the GATE pull-down current during startup and in the circuit breaker mode.

TIMER CAPACITOR, C_T

The TIMER pin capacitor (C_T) sets the timing for the insertion time delay, fault timeout period, and restart timing of the LM5069-2.

A) Insertion Delay - Upon applying the system voltage (V_{SYS}) to the circuit, the external MOSFET (Q1) is held off during the insertion time (t1 in Figure 24) to allow ringing and transients at V_{SYS} to settle. Since each backplane's response to a circuit card plug-in is unique, the worst case settling time must be determined for each application. The insertion time starts when VIN reaches the POR_{IT} threshold, at which time the internal 5.5 µA current source charges C_T from 0V to 4.0V. The required capacitor value is calculated from:

$$C_T = \frac{t1 \times 5.5\ \mu A}{4V} = t1 \times 1.38 \times 10^{-6}$$

For example, if the desired insertion delay is 250 ms, C_T calculates to 0.345 µF. At the end of the insertion delay, C_T is quickly discharged by a 1.5 mA current sink.

B) Fault Timeout Period - During in-rush current limiting or upon detection of a fault condition where the current limit and/or power limit circuits regulate the current through Q1, the fault timer current source (85 µA) is switched on to charge C_T. The Fault Timeout Period is the time required for the TIMER pin voltage to reach 4.0V, at which time Q1 is switched off. The required capacitor value for the desired Fault Timeout Period t_{FAULT} is calculated from:

$$C_T = \frac{t_{FAULT} \times 85\ \mu A}{4V} = t_{FAULT} \times 2.13 \times 10^{-5} \quad (3)$$

For example, if the desired Fault Timeout Period is 16 ms, C_T calculates to 0.34 µF. After the Fault Timeout Period, the LM5069-1 latches the GATE pin low until a power up sequence is initiated by external circuitry. C_T is discharged by the 2.5 µA current sink at the end of the Fault Timeout Period. See the Fault Timer & Restart section and Figure 26. When the Fault Timeout Period of the LM5069-2 expires, a restart sequence starts as described below (Restart Timing). Since the LM5069 normally operates in power limit and/or current limit during a power up sequence, the Fault Timeout Period must be longer than the time required for the output voltage to reach its final value. See the Turn-on Time section.

C) Restart Timing For the LM5069-2, after the Fault Timeout Period described above, C_T is discharged by the 2.5 µA current sink to 1.25V. The TIMER pin then cycles through seven additional charge/discharge cycles between 1.25V and 4.0V as shown in Figure 27. The restart time ends when the TIMER pin voltage reaches 0.3V during the final high-to-low ramp. The restart time, after the Fault Timeout Period, is equal to:

$$t_{RESTART} = C_T \times \left[\frac{7 \times 2.75V}{2.5\ \mu A} + \frac{7 \times 2.75V}{85\ \mu A} + \frac{3.7V}{2.5\ \mu A} \right]$$

$$= C_T \times 9.4 \times 10^6$$

For example, if C_T = 0.33 µF, $t_{RESTART}$ = 3.1 seconds. At the end of the restart time, Q1 is switched on. If the fault is still present, the fault timeout and restart sequence repeats. The on-time duty cycle of Q1 is approximately 0.5% in this mode.

UVLO, OVLO

By programming the UVLO and OVLO thresholds the LM5069 enables the series pass device (Q1) when the input supply voltage (V_{SYS}) is within the desired operational range. If V_{SYS} is below the UVLO threshold, or above the OVLO threshold, Q1 is switched off, denying power to the load. Hysteresis is provided for each threshold.

Option A: The configuration shown in Figure 33 requires three resistors (R1-R3) to set the thresholds.

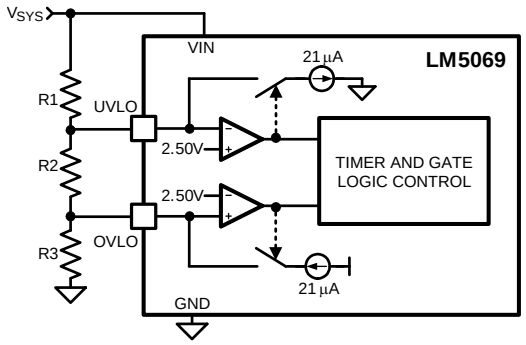


Figure 33. UVLO and OVLO Thresholds Set By R1-R3

The procedure to calculate the resistor values is as follows:

- Choose the upper UVLO threshold (V_{UVH}), and the lower UVLO threshold (V_{UVL}).

- Choose the upper OVLO threshold (V_{OVH}).

- The lower OVLO threshold (V_{OVL}) cannot be chosen in advance in this case, but is determined after the values for R1-R3 are determined. If V_{OVL} must be accurately defined in addition to the other three thresholds, see Option B below.

The resistors are calculated as follows:

$$R1 = \frac{V_{UVH} - V_{UVL}}{21\ \mu A} = \frac{V_{UV(HYS)}}{21\ \mu A}$$

$$R3 = \frac{2.5V \times R1 \times V_{UVL}}{V_{OVH} \times (V_{UVL} - 2.5V)}$$

$$R2 = \frac{2.5V \times R1}{V_{UVL} - 2.5V} - R3$$

The lower OVLO threshold is calculated from:

$$V_{OVL} = [(R1 + R2) \times ((\frac{2.5V}{R3}) - 21\ \mu A)] + 2.5V$$

As an example, assume the application requires the following thresholds: V_{UVH} = 36V, V_{UVL} = 32V, V_{OVH} = 60V.

$$R1 = \frac{36V - 32V}{21\ \mu A} = \frac{4V}{21\ \mu A} = 190.5\ k\Omega$$

$$R3 = \frac{2.5V \times 190.5\ k\Omega \times 32V}{60V \times (32V - 2.5V)} = 8.61\ k\Omega$$

$$R2 = \frac{2.5V \times 190.5\ k\Omega}{(32V - 2.5V)} - 8.61\ k\Omega = 7.53\ k\Omega$$

The lower OVLO threshold calculates to 55.8V, and the OVLO hysteresis is 4.2V. Note that the OVLO hysteresis is always slightly greater than the UVLO hysteresis in this configuration. When the R1-R3 resistor values are known, the threshold voltages and hysteresis are calculated from the following:

$$V_{UVH} = 2.5V + [R1 \times (21\ \mu A + \frac{2.5V}{(R2 + R3)})]$$

$$V_{UVL} = \frac{2.5V \times (R1 + R2 + R3)}{R2 + R3}$$

$$V_{UV(HYS)} = R1 \times 21\ \mu A$$

$$V_{OVH} = \frac{2.5V \times (R1 + R2 + R3)}{R3}$$

$$V_{OVL} = [(R1 + R2) \times \frac{(2.5V)}{R3} - 21\ \mu A)] + 2.5V$$

$$V_{OV(HYS)} = (R1 + R2) \times 21\ \mu A$$

Option B: If all four thresholds must be accurately defined, the configuration in Figure 34 can be used.

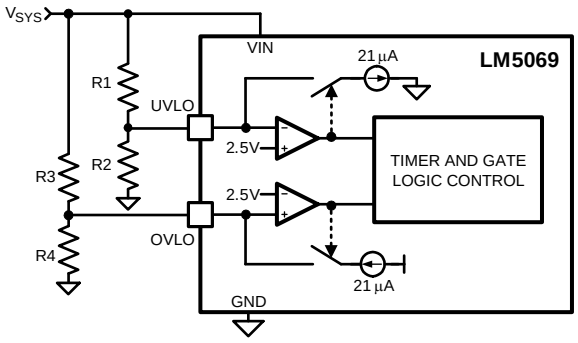


Figure 34. Programming the Four Thresholds

The four resistor values are calculated as follows:

- Choose the upper and lower UVLO thresholds (V_{UVH}) and (V_{UVL}).

$$R1 = \frac{V_{UVH} - V_{UVL}}{21\ \mu A} = \frac{V_{UV(HYS)}}{21\ \mu A}$$

$$R2 = \frac{2.5V \times R1}{(V_{UVL} - 2.5V)}$$

-Choose the upper and lower OVLO threshold (V_{OVH}) and (V_{OVL}).

$$R3 = \frac{V_{OVH} - V_{OVL}}{21\ \mu A} = \frac{V_{OV(HYS)}}{21\ \mu A}$$

$$R4 = \frac{2.5V \times R3}{(V_{OVH} - 2.5V)}$$

As an example, assume the application requires the following thresholds: V_{UVH} = 22V, V_{UVL} = 17V, V_{OVH} = 60V, and V_{OVL} = 58V. Therefore $V_{UV(HYS)}$ = 5V, and $V_{OV(HYS)}$ = 2V. The resistor values are:

R1 = 238 kΩ, R2 = 41 kΩ

R3 = 95.2 kΩ, R4 = 4.14 kΩ

Where the R1-R4 resistor values are known, the threshold voltages and hysteresis are calculated from the following:

$$V_{UVH} = 2.5V + [R1 \times (\frac{2.5V}{R2} + 21\ \mu A)]$$

$$V_{UVL} = \frac{2.5V \times (R1 + R2)}{R2}$$

$$V_{UV(HYS)} = R1 \times 21\ \mu A$$

$$V_{OVH} = \frac{2.5V \times (R3 + R4)}{R4}$$

$$V_{OVL} = 2.5V + [R3 \times (\frac{2.5V}{R4} - 21\ \mu A)]$$

$$V_{OV(HYS)} = R3 \times 21\ \mu A$$

Option C: The minimum UVLO level is obtained by connecting the UVLO pin to VIN as shown in Figure 35. Q1 is switched on when the VIN voltage reaches the POR_{EN} threshold (≅8.4V). An external transistor can be connected to UVLO to provide remote shutdown control, and to restart the LM5069-1 after a fault detection. The OVLO thresholds are set using R3, R4. Their values are calculated using the procedure in Option B.

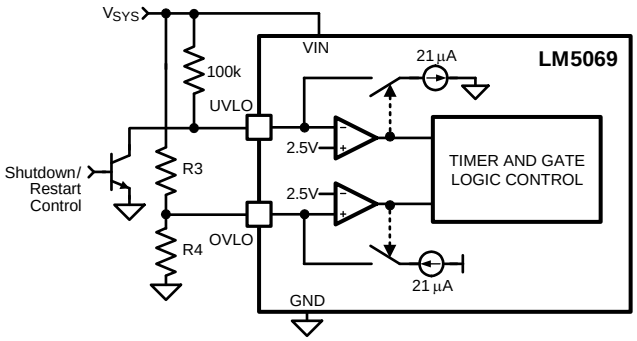


Figure 35. UVLO = POR_{EN} with Shutdown/Restart Control

Option D: The OVLO function can be disabled by grounding the OVLO pin. The UVLO thresholds are set as described in Option B or Option C.

POWER GOOD PIN

During turn-on, the Power Good pin (PGD) is high until the voltage at VIN increases above ≅ 5V. PGD then switches low, remaining low as the VIN voltage increases. When the voltage at OUT increases to within 1.25V of the SENSE pin (V_{DS} <1.25V), PGD switches high. PGD switches low if the V_{DS} of Q1 increases above 2.5V. A pull-up resistor is required at PGD as shown in Figure 36. The pull-up voltage (V_{PGD}) can be as high as 80V, with transient capability to 100V, and can be higher or lower than the voltages at VIN and OUT.

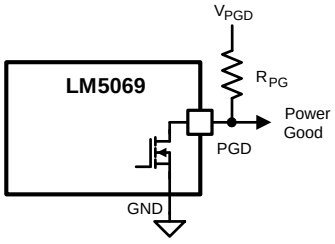


Figure 36. Power Good Output

If a delay is required at PGD, suggested circuits are shown in Figure 37. In Figure 37a, capacitor C_{PG} adds delay to the rising edge, but not to the falling edge. In Figure 37b, the rising edge is delayed by R_{PG1} + R_{PG2} and C_{PG}, while the falling edge is delayed a lesser amount by R_{PG2} and C_{PG}. Adding a diode across R_{PG2} (Figure 37c) allows for equal delays at the two edges, or a short delay at the rising edge and a long delay at the falling edge.

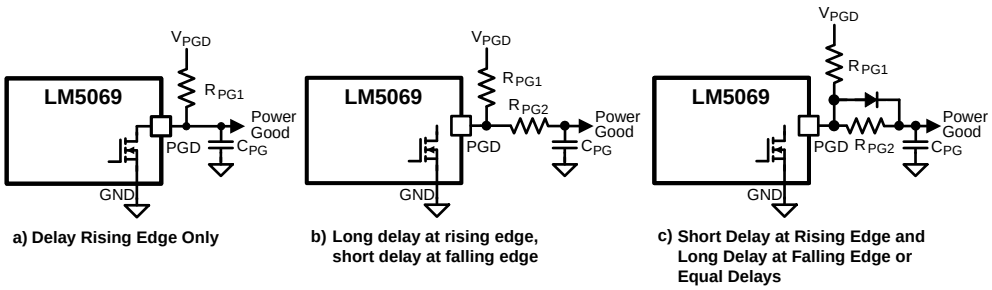


Figure 37. Adding Delay to the Power Good Output Pin

Design-in Procedure

The recommended design-in procedure is as follows:

- Determine the current limit threshold (I_{LIM}). This threshold must be higher than the normal maximum load current, allowing for tolerances in the current sense resistor value and the LM5069 Current Limit threshold voltage. Use Equation 1 to determine the value for R_S.
- Determine the maximum allowable power dissipation for the series pass FET (Q1), using the device's SOA information. Use Equation 2 to determine the value for R_{PWR}.
- Determine the value for the timing capacitor at the TIMER pin (C_T) using Equation 3. The fault timeout period (t_{FAULT}) must be longer than the circuit's turn-on-time. The turn-on time can be estimated using the equations in the Turn-on Time section of this data sheet, but should be verified experimentally. Review the resulting insertion time, and restart timing if the LM5069-2 is used.
- Choose option A, B, C, or D from the UVLO, OVLO section of the Application Information for setting the UVLO and OVLO thresholds and hysteresis. Use the procedure for the appropriate option to determine the resistor values at the UVLO and OVLO pins.
- Choose the appropriate voltage, and pull-up resistor, for the Power Good output.

PC Board Guidelines

The following guidelines should be followed when designing the PC board for the LM5069:

- Place the LM5069 close to the board's input connector to minimize trace inductance from the connector to the FET.
- Place a small capacitor (1000 pF) directly adjacent to the VIN and GND pins of the LM5069 to help minimize transients which may occur on the input supply line. Transients of several volts can easily occur when the load current is shut off.
- The sense resistor (R_S) should be close to the LM5069, and connected to it using the Kelvin techniques shown in Figure 29.
- The high current path from the board's input to the load (via Q1), and the return path, should be parallel and close to each other to minimize loop inductance.
- The ground connection for the various components around the LM5069 should be connected directly to each other, and to the LM5069's GND pin, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.
- Provide adequate heat sinking for the series pass device (Q1) to help reduce stresses during turn-on and turn-off.
- The board's edge connector can be designed to shut off the LM5069 as the board is removed, before the supply voltage is disconnected from the LM5069. In Figure 38 the voltage at the UVLO pin goes to ground before V_{SYS} is removed from the LM5069 due to the shorter edge connector pin. When the board is inserted into the edge connector, the system voltage is applied to the LM5069's VIN pin before the UVLO voltage is taken high.

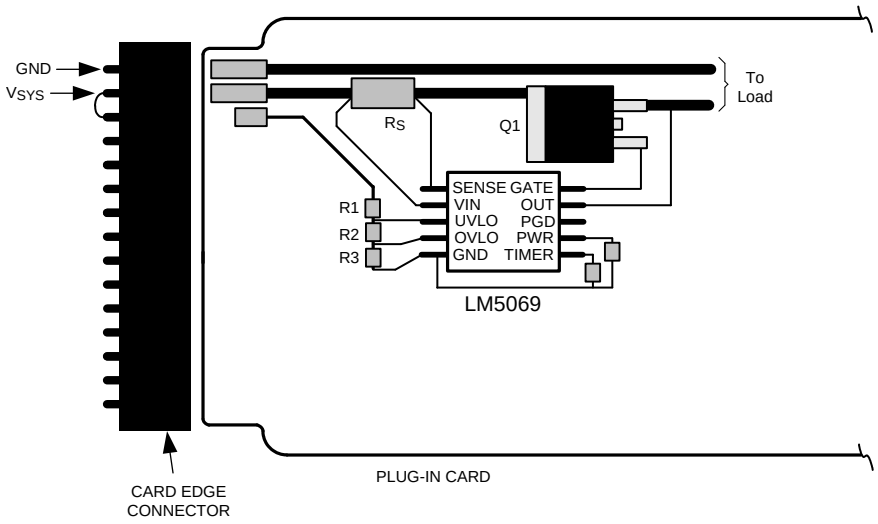


Figure 38. Recommended Board Connector Design

System Considerations

A) Continued proper operation of the LM5069 hot swap circuit requires capacitance be present on the supply side of the connector into which the hot swap circuit is plugged in, as depicted in Figure 23. The capacitor in the "Live Backplane" section is necessary to absorb the transient generated whenever the hot swap circuit shuts off the load current. If the capacitance is not present, inductance in the supply lines will generate a voltage transient at shut-off which can exceed the absolute maximum rating of the LM5069, resulting in its destruction.

B) If the load powered via the LM5069 hot swap circuit has inductive characteristics, a diode is required across the LM5069's output. The diode provides a recirculating path for the load's current when the LM5069 shuts off that current. Adding the diode prevents possible damage to the LM5069 as the OUT pin will be taken below ground by the inductive load at shutoff. See Figure 39.

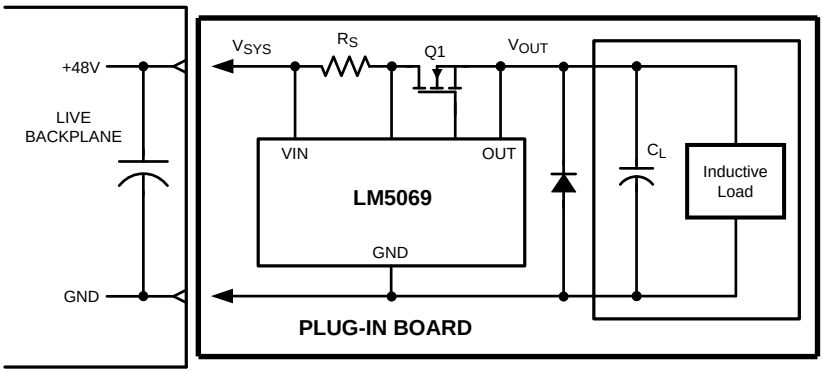


Figure 39. Output Diode Required for Inductive Loads

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5069MM-1/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SNAB	Samples
LM5069MM-2	ACTIVE	VSSOP	DGS	10	1000	TBD	Call TI	Call TI	-40 to 125	SNBB	Samples
LM5069MM-2/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SNBB	Samples
LM5069MMX-1	ACTIVE	VSSOP	DGS	10	3500	TBD	Call TI	Call TI	-40 to 125	SNAB	Samples
LM5069MMX-1/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SNAB	Samples
LM5069MMX-2	ACTIVE	VSSOP	DGS	10	3500	TBD	Call TI	Call TI	-40 to 125	SNBB	Samples
LM5069MMX-2/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SNBB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

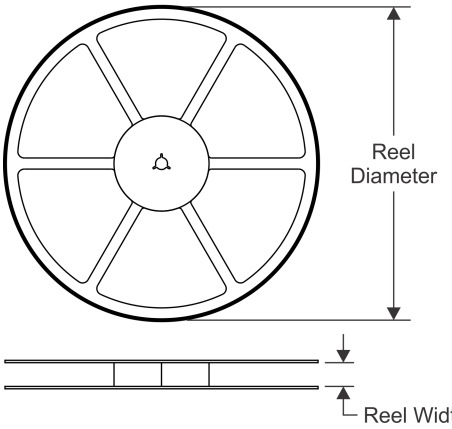
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

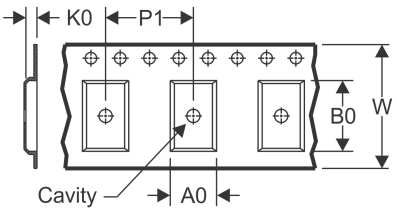
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

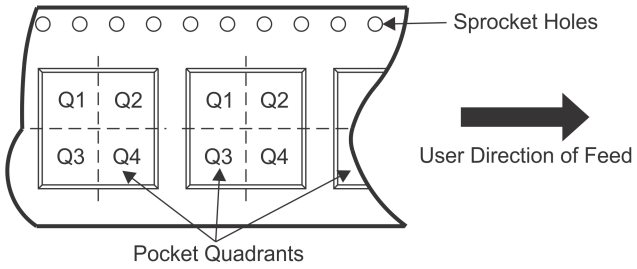


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

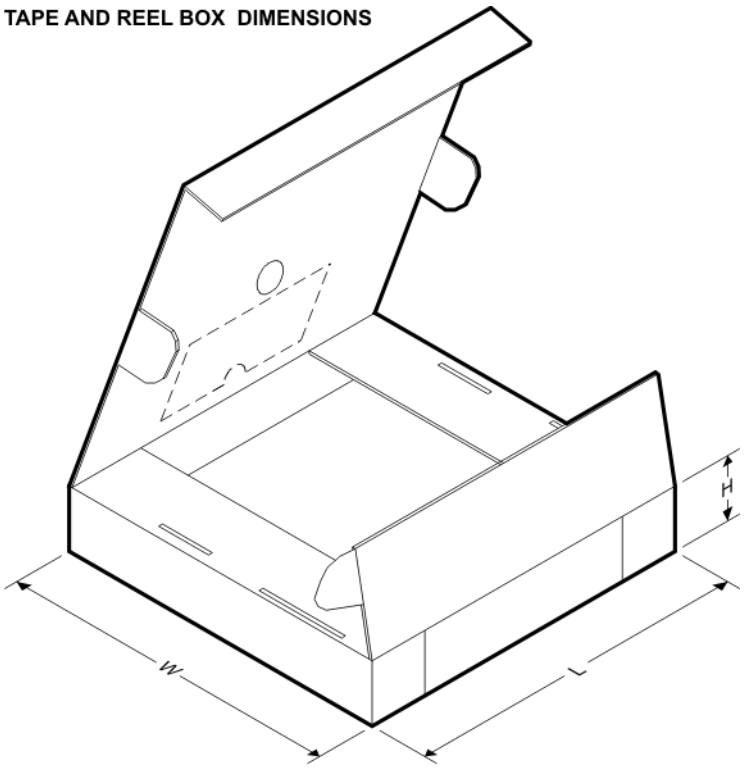
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5069MM-1/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5069MM-2	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5069MM-2/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5069MMX-1	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5069MMX-1/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5069MMX-2	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5069MMX-2/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

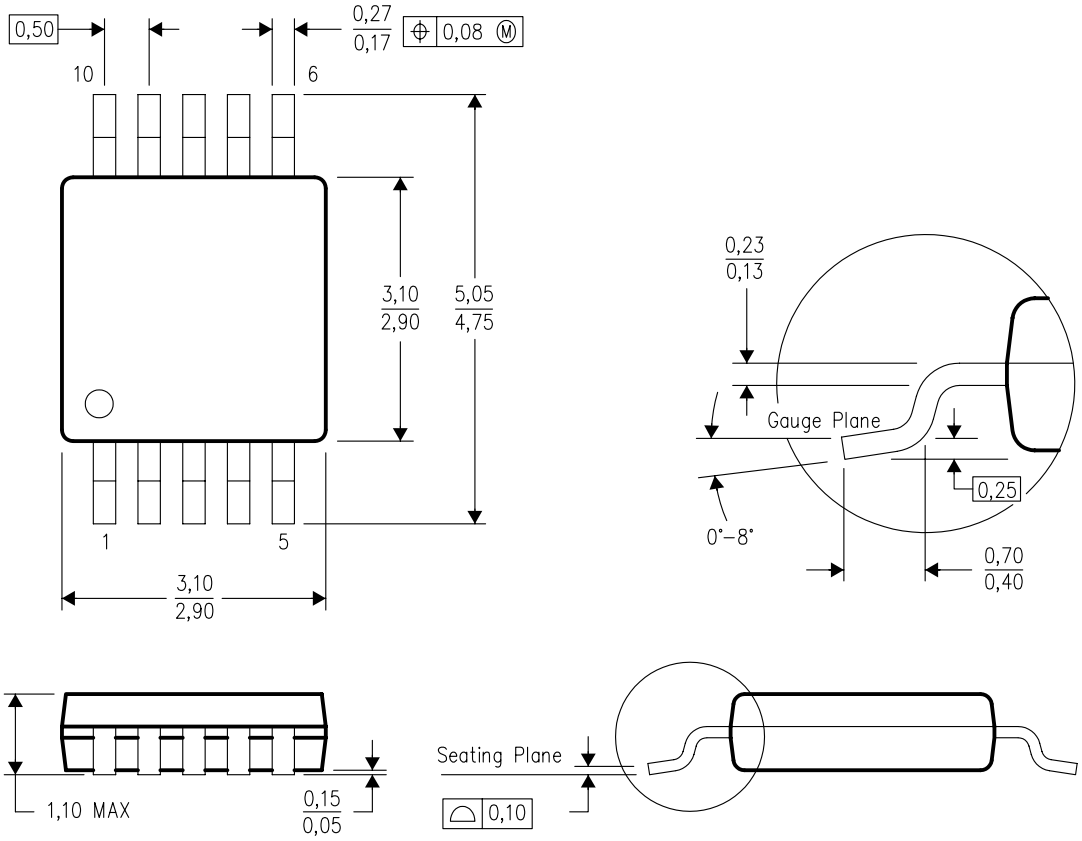
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5069MM-1/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LM5069MM-2	VSSOP	DGS	10	1000	210.0	185.0	35.0
LM5069MM-2/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LM5069MMX-1	VSSOP	DGS	10	3500	367.0	367.0	35.0
LM5069MMX-1/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0
LM5069MMX-2	VSSOP	DGS	10	3500	367.0	367.0	35.0
LM5069MMX-2/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

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