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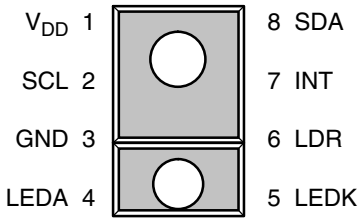
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Features

- Ambient Light Sensing, Proximity Detection, and IR LED in a Single Module
- Register Set- and Pin-Compatible with the TMD2771 Series
- Ambient Light Sensing (ALS)
  - Approximates Human Eye Response
  - Programmable Analog Gain and Integration Time
  - 8,000,000:1 Dynamic Range
  - Very High Sensitivity — Ideally Suited for Operation Behind Dark Glass
- Proximity Detection
  - Reduced Proximity Count Variation *
  - Programmable Offset *
  - Saturation Indicator *
  - Current Sink Driver for IR LED
  - 16,000:1 Dynamic Range
- Maskable ALS and Proximity Interrupt
  - Programmable Upper and Lower Thresholds with Persistence Filter
- Power Management
  - Low Power 2.2 μA Sleep State with User-Selectable Sleep-After-Interrupt Mode
  - 90 μA Wait State with Programmable Wait Time from 2.7 ms to > 8 seconds
- I^2C Fast Mode Compatible Interface
  - Data Rates up to 400 kbit/s
  - Input Voltage Levels Compatible with V_{DD} or 1.8-V Bus
- 3.94 mm × 2.36 mm × 1.35 mm Package

* New or improved feature

PACKAGE
MODULE–8
(TOP VIEW)



Package Drawing is Not to Scale

Applications

- Display Backlight Control
- Cell Phone Touch Screen Disable
- Mechanical Switch Replacement
- Industrial Process Control
- Medical Diagnostics
- Printer Paper Alignment

End Products and Market Segments

- Mobile Handsets, Tablets, Laptops, HDTVs, Monitors, and PMP (Portable Media Players)
- Medical and Industrial Instrumentation
- White Goods
- Toys
- Industrial/Commercial Lighting
- Digital Signage
- Printers

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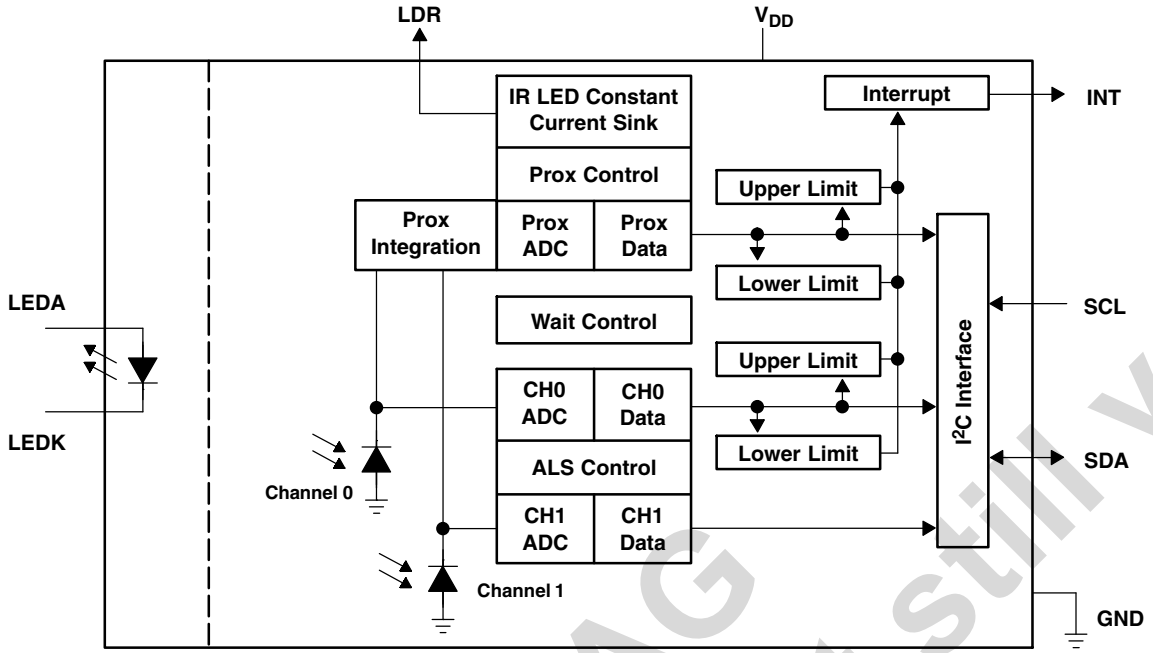
Description

The TMD2772 family of devices provides digital ambient light sensing (ALS), a complete proximity detection system, and digital interface logic in a single 8-pin surface mount module. The devices are register-set and pin-compatible with the TMD2771 family of devices and include new and improved ALS and proximity detection features. The ALS enhancements include a reduced-gain mode that extends the operating range in sunlight. Proximity detection includes improved signal-to-noise performance and more accurate factory calibration. A proximity offset register allows compensation for optical system crosstalk between the IR LED and the sensor. To prevent false proximity data measurement readings, a proximity saturation indicator bit signals that the internal analog circuitry has reached saturation.

The TMD2772 ALS is based on the TAOS patented dual-diode technology that enables accurate results and approximates human eye response to light intensity under a variety of lighting conditions. The proximity detection system includes an LED driver and an IR LED, which are factory trimmed to eliminate the need for end-equipment calibration due to component variations.

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Functional Block Diagram



Detailed Description

The light-to-digital device provides on-chip photodiodes, integrating amplifiers, ADCs, accumulators, clocks, buffers, comparators, a state machine, and an I^2C interface. Each device combines one photodiode (CH0), which is responsive to both visible and infrared light, and a second photodiode (CH1), which is responsive primarily to infrared light. Two integrating ADCs simultaneously convert the amplified photodiode currents to a digital value providing up to 16-bits of resolution. Upon completion of the conversion cycle, the conversion result is transferred to the Ch0 and Ch1 data registers. This digital output can be read by a microprocessor where the luminance (ambient light level in lux) is derived using an empirical formula to approximate the human eye response.

A fully integrated proximity detection solution is provided with an 850-nm IR LED, LED driver circuit, and proximity detection engine. An internal LED driver pin (LDR) is externally connected to the LED cathode (LEDK) to provide a controlled LED sink current. This is accomplished with a proprietary current calibration technique that accounts for all variances in silicon, optics, package, and most important, IR LED output power. This eliminates or greatly reduces the need for factory calibration that is required for most discrete proximity sensor solutions. The *device* is factory calibrated to achieve a proximity count reading at a specified distance with a specific number of pulses. In use, the number of proximity LED pulses can be programmed from 1 to 255 pulses, which allows different proximity distances to be achieved. Each pulse has a 16 μs period with a 7.2 μs on time.

Communication with the device is accomplished through a fast (up to 400 kHz), two-wire I^2C serial bus for easy connection to a microcontroller or embedded controller. The digital output of the device is inherently more immune to noise when compared to an analog photodiode interface.

The device provides a separate pin for level-style interrupts. When interrupts are enabled and a pre-set value is exceeded, the interrupt pin is asserted and remains asserted until cleared by the controlling firmware. The interrupt feature simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity or proximity value. An interrupt is generated when the value of an ALS or proximity conversion exceeds either an upper or lower threshold. In addition, a programmable interrupt persistence feature allows the user to determine how many consecutive exceeded thresholds are necessary to trigger an interrupt. Interrupt thresholds and persistence settings are configured independently for both ALS and proximity.

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Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
GND	3		Power supply ground. All voltages are referenced to GND.
INT	7	O	Interrupt — open drain (active low).
LDR	6	O	LED driver input for proximity IR LED, constant current source LED driver.
LEDA	4		LED anode.
LEDK	5		LED cathode. Connect to LDR pin when using internal LED driver circuit.
SCL	2	I	I^2C serial clock input terminal — clock signal for I^2C serial data.
SDA	8	I/O	I^2C serial data I/O terminal — serial data I/O for I^2C .
V_{DD}	1		Supply voltage.

Available Options

DEVICE	ADDRESS	PACKAGE – LEADS	INTERFACE DESCRIPTION	ORDERING NUMBER
TMD27721	0x39	Module–8	I^2C Vbus = V_{DD} Interface	TMD27721
TMD27723	0x39	Module–8	I^2C Vbus = 1.8 V Interface	TMD27723
TMD27725†	0x29	Module–8	I^2C Vbus = V_{DD} Interface	TMD27725
TMD27727†	0x29	Module–8	I^2C Vbus = 1.8 V Interface	TMD27727

† Contact TAOS for availability.

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (Note 1) . . . . . 3.8 V
Digital I/O Voltage (except LDR) . . . . . –0.5 V to 3.8 V
Max LEDA Voltage (T_A=0 to 70C, 4.4V otherwise. Note 2) . . . . . 4.8 V
Max LDR Voltage (T_A=0 to 70C, 4.4V otherwise. Note 3) . . . . . 4.8 V
Output terminal current (except LDR) . . . . . –1 mA to 20 mA
Storage temperature range, T_{stg} . . . . . –40°C to 85°C
ESD tolerance, human body model . . . . . 2000 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to GND.

2. Maximum 4.8V DC over 7 years lifetime.
Maximum 5.0V spikes with up to 250s cumulative duration over 7 years lifetime.
Maximum 5.5V spikes with up to 10s (=1000* 10ms) cumulative duration over 7 years lifetime.

3. Maximum voltage with LDR = off.

Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	2.2	3	3.6	V
Supply voltage accuracy, V_{DD} total error including transients	–3		3	%
LED Supply Voltage (Max shown for T_A=0 to 70C, 4.4V otherwise)	2.5		4.8	V
Operating free-air temperature, T_A (Note 2)	–30		85	°C

NOTE 2: While the device is operational across the temperature range, functionality will vary with temperature. Specifications are stated only at 25°C unless otherwise noted.

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Operating Characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	Active — LDR pulse off		195	250	µA
		Wait state		90		
		Sleep state — no I^2C activity		2.2	4	
V_{OL}	INT, SDA output low voltage	3 mA sink current	0		0.4	V
		6 mA sink current	0		0.6	
I_{LEAK}	Leakage current, SDA, SCL, INT pins		–5		5	µA
I_{LEAK}	Leakage current, LDR pin		–5		5	µA
V_{IH}	SCL, SDA input high voltage	TMD27721	0.7 V_{DD}			V
		TMD27723	1.25			
V_{IL}	SCL, SDA input low voltage	TMD27721			0.3 V_{DD}	V
		TMD27723			0.54	

ALS Characteristics, V_{DD} = 3 V, T_A = 25°C, AGAIN = 16×, AEN = 1 (unless otherwise noted) (Notes 1 ,2, 3)

PARAMETER	TEST CONDITIONS	CHANNEL	MIN	TYP	MAX	UNIT
Dark ADC count value	E_e = 0, AGAIN = 120×, ATIME = 0xDB (100 ms)	CH0	0	1	5	counts
		CH1	0	1	5	
ADC integration time step size	ATIME = 0xFF		2.58	2.73	2.9	ms
ADC number of integration steps			1		256	steps
ADC counts per step	ATIME = 0xFF		0		1024	counts
ADC count value	ATIME = 0xC0		0		65535	counts
ADC count value	λ_p = 625 nm, E_e = 46.8 µW/cm², ATIME = 0xF6 (27 ms) (Note 2)	CH0	4000	5000	6000	counts
		CH1		950		
	λ_p = 850 nm, E_e = 61.7 µW/cm², ATIME = 0xF6 (27 ms) (Note 3)	CH0	4000	5000	6000	
		CH1		2900		
ADC count value ratio: CH1/CH0	λ_p = 625 nm, ATIME = 0xF6 (27 ms) (Note 2)		0.152	0.19	0.228	
	λ_p = 850 nm, ATIME = 0xF6 (27 ms) (Note 3)		0.43	0.58	0.73	
R_e Irradiance responsivity	λ_p = 625 nm, ATIME = 0xF6 (27 ms) (Note 2)	CH0		107.2		counts/(µW/cm²)
		CH1		20.4		
	λ_p = 850 nm, ATIME = 0xF6 (27 ms) (Note 3)	CH0		81.5		
		CH1		47.3		
Gain scaling, relative to 1× gain setting	AGAIN = 1× and AGL = 1			0.16		×
	AGAIN = 8× and AGL = 0		7.2	8.0	8.8	
	AGAIN = 16× and AGL = 0		14.4	16.0	17.6	
	AGAIN = 120× and AGL = 0		108	120	132	

NOTES: 1. Optical measurements are made using small-angle incident radiation from light-emitting diode optical sources. Red 625 nm and infrared 850 nm LEDs are used for final product testing for compatibility with high-volume production.
2. The 625 nm irradiance E_e is supplied by an AlInGaP light-emitting diode with the following typical characteristics: peak wavelength λp = 625 nm and spectral halfwidth Δλ½ = 20 nm.
3. The 850 nm irradiance E_e is supplied by a GaAs light-emitting diode with the following typical characteristics: peak wavelength λp = 850 nm and spectral halfwidth Δλ½ = 42 nm.

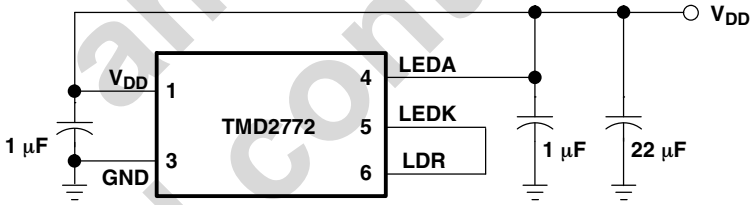
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Proximity Characteristics, V_{DD} = V_{LEDA} = 3 V, T_A = 25°C, PEN = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	LED On		3		mA
I_{LEDA}	LEDA current (Note 1)	LED On, PDRIVE = 0		100		mA
		LED On, PDRIVE = 1		50		
		LED On, PDRIVE = 2		25		
		LED On, PDRIVE = 3		12.5		
PTIME	ADC conversion steps		1		256	steps
PTIME	ADC conversion time	PTIME = 0xFF (= 1 conversion step)	2.58	2.73	2.9	ms
PTIME	ADC counts per step	PTIME = 0xFF (= 1 conversion step)	0		1023	counts
PPULSE	LED pulses (Note 5)		0		255	pulses
LED On	LED pulse width	PPULSE = 1, PDRIVE = 0		7.3		µs
	LED pulse period	PPULSE = 2, PDRIVE = 0		16.0		µs
	Proximity response, no target (offset)	PPULSE = 8, PDRIVE = 0, PGAIN = 4×, (Note 2)		100		counts
	Prox count, 100-mm target (Note 3)	73 mm × 83 mm, 90% reflective Kodak Gray Card, PGAIN = 4×, PPULSE = 8, PDRIVE = 0, PTIME = 0xFF (Note 4)	450	520	590	counts

NOTES: 1. Value is factory-adjusted to meet the Prox count specification. Considerable variation (relative to the typical value) is possible after adjustment.
2. Proximity offset varies with power supply characteristics and noise.
3. I_{LEDA} is factory calibrated to achieve this specification. Offset and crosstalk directly sum with this value and is system dependent.
4. No glass or aperture above the module. Tested value is the average of 5 consecutive readings.
5. These parameters are ensured by design and characterization and are not 100% tested.
6. Proximity test was done using the following circuit. See the **Application Information: Hardware** section for recommended application circuit.



IR LED Characteristics, V_{DD} = 3 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_F	Forward Voltage	I_F = 20 mA		1.4	1.5	V
V_R	Reverse Voltage	I_R = 10 µA	5			V
P_O	Radiant Power	I_F = 20 mA	4.5			mW
λ_p	Peak Wavelength	I_F = 20 mA		850		nm
$\Delta\lambda$	Spectral Radiation Bandwidth	I_F = 20 mA		40		nm
T_R	Optical Rise Time	I_F = 100 mA, T_W = 125 ns, duty cycle = 25%		20	40	ns
T_F	Optical Fall Time	I_F = 100 mA, T_W = 125 ns, duty cycle = 25%		20	40	ns

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Wait Characteristics, V_{DD} = 3 V, T_A = 25°C, WEN = 1 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Wait steps		1		256	steps
Wait time	WTIME = 0xFF (= 1 wait step)		2.73	2.9	ms

AC Electrical Characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER†		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SCL)}$	Clock frequency (I^2C only)		0		400	kHz
$t_{(BUF)}$	Bus free time between start and stop condition		1.3			µs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.		0.6			µs
$t_{(SUSTA)}$	Repeated start condition setup time		0.6			µs
$t_{(SUSTO)}$	Stop condition setup time		0.6			µs
$t_{(HDDAT)}$	Data hold time		0			µs
$t_{(SUDAT)}$	Data setup time		100			ns
$t_{(LOW)}$	SCL clock low period		1.3			µs
$t_{(HIGH)}$	SCL clock high period		0.6			µs
t_F	Clock/data fall time				300	ns
t_R	Clock/data rise time				300	ns
C_i	Input pin capacitance				10	pF

† Specified by design and characterization; not production tested.

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PARAMETER MEASUREMENT INFORMATION

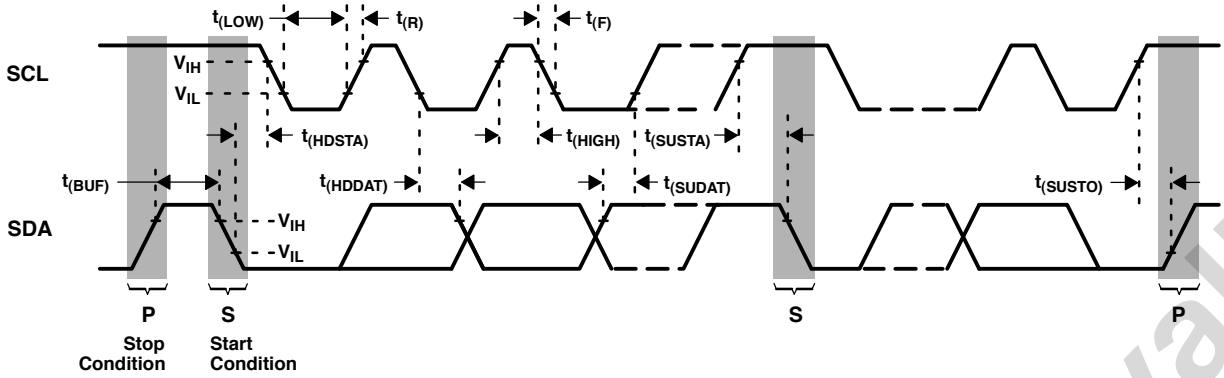


Figure 1. Timing Diagrams

TYPICAL CHARACTERISTICS

SPECTRAL RESPONSIVITY

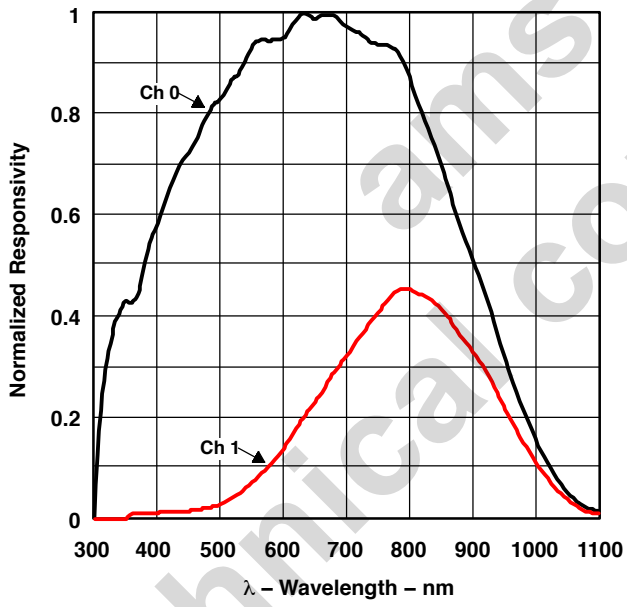


Figure 2

NORMALIZED RESPONSIVITY vs. ANGULAR DISPLACEMENT

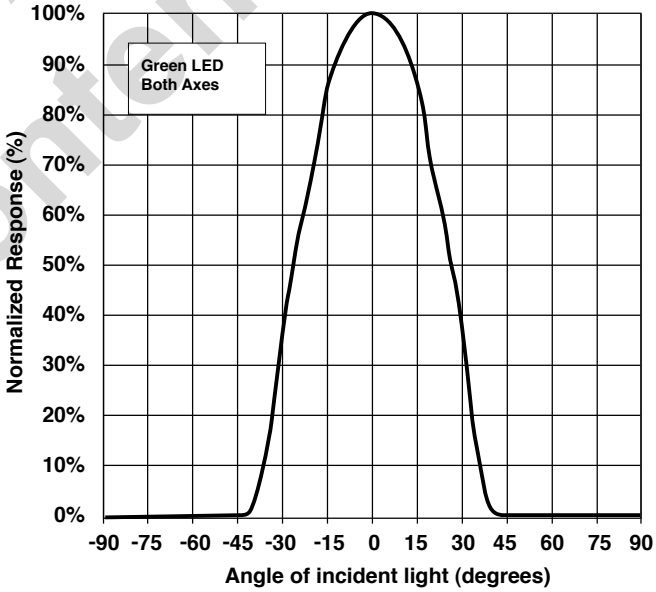


Figure 3

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TYPICAL CHARACTERISTICS

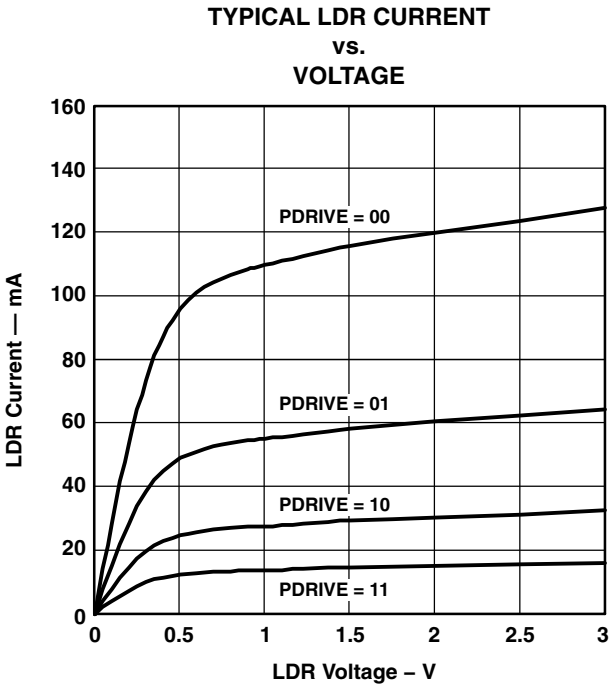


Figure 4

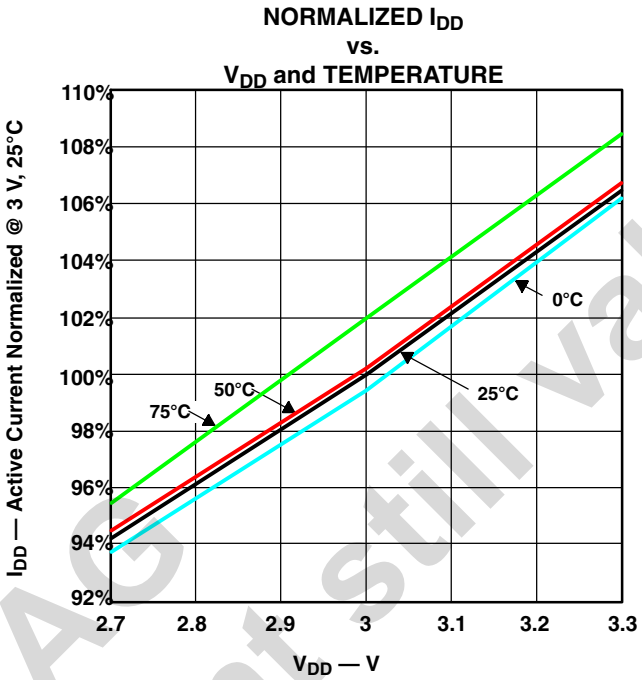


Figure 5

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PRINCIPLES OF OPERATION

System State Machine

An internal state machine provides system control of the ALS, proximity detection, and power management features of the device. At power up, an internal power-on-reset initializes the device and puts it in a low-power Sleep state.

When a start condition is detected on the I^2C bus, the device transitions to the Idle state where it checks the Enable register (0x00) PON bit. If PON is disabled, the device will return to the Sleep state to save power. Otherwise, the device will remain in the Idle state until a proximity or ALS function is enabled. Once enabled, the device will execute the Prox, Wait, and ALS states in sequence as indicated in Figure 5. Upon completion and return to Idle, the device will automatically begin a new prox–wait–ALS cycle as long as PON and either PEN or AEN remain enabled.

If the Prox or ALS function generates an interrupt and the Sleep-After-Interrupt (SAI) feature is enabled, the device will transition to the Sleep state and remain in a low-power mode until an I^2C command is received. See the Interrupts section for additional information.

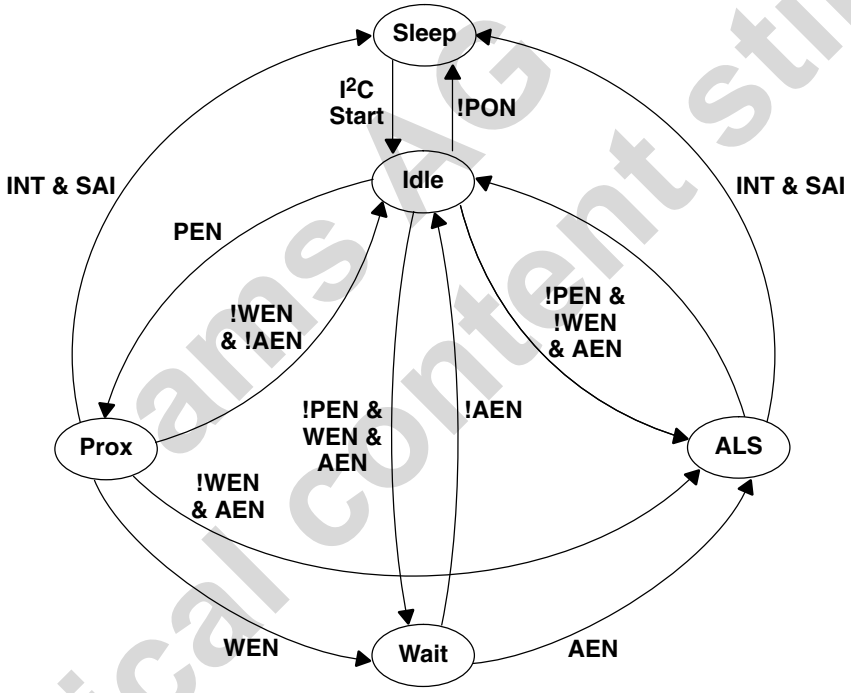


Figure 6. Simplified State Diagram

Photodiodes

Conventional ALS detectors respond strongly to infrared light, which the human eye does not see. This can lead to significant error when the infrared content of the ambient light is high (such as with incandescent lighting).

This problem is overcome through the use of two photodiodes. The Channel 0 photodiode, referred to as the CH0 channel, is sensitive to both visible and infrared light, while the Channel 1 photodiode, referred to as CH1, is sensitive primarily to infrared light. Two integrating ADCs convert the photodiode currents to digital outputs. The ADC digital outputs from the two channels are used in a formula to obtain a value that approximates the human eye response in units of lux.

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ALS Operation

The ALS engine contains ALS gain control (AGAIN) and two integrating analog-to-digital converters (ADC), one for the CH0 and one for the CH1 photodiodes. The ALS integration time (ATIME) impacts both the resolution and the sensitivity of the ALS reading. Integration of both channels occurs simultaneously and upon completion of the conversion cycle, the results are transferred to the data registers (C0DATA and C1DATA). This data is also referred to as channel *count*. The transfers are double-buffered to ensure data integrity.

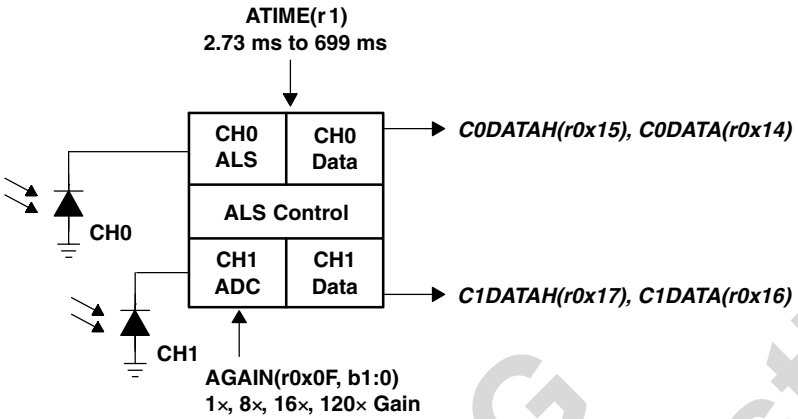


Figure 7. ALS Operation

The registers for programming the integration and wait times are a 2's compliment values. The actual time can be calculated as follows:

ATIME = 256 – Integration Time / 2.73 ms

Inversely, the time can be calculated from the register value as follows:

Integration Time = 2.73 ms × (256 – ATIME)

In order to reject 50/60-Hz ripple strongly present in fluorescent lighting, the integration time needs to be programmed in multiples of 10 / 8.3 ms or the half cycle time. Both frequencies can be rejected with a programmed value of 50 ms (ATIME = 0xED) or multiples of 50 ms (i.e. 100, 150, 200, 400, 600).

The registers for programming the AGAIN hold a two-bit value representing a gain of 1×, 8×, 16×, or 120×. The gain, in terms of amount of gain, will be represented by the value AGAINx, i.e. AGAINx = 1, 8, 16, or 120. With the AGL bit set, the gains will be lowered to 1/6, 8/6, 16/6, and 20×, allowing for up to 60k lux.

Lux Equation

The lux calculation is a function of CH0 channel count (C0DATA), CH1 channel count (C1DATA), ALS gain (AGAINx), and ALS integration time in milliseconds (ATIME_ms). If an aperture, glass/plastic, or a light pipe attenuates the light equally across the spectrum (300 nm to 1100 nm), then a scaling factor referred to as glass attenuation (GA) can be used to compensate for attenuation. For a device in open air with no aperture or glass/plastic above the device, GA = 1. If it is not spectrally flat, then a custom lux equation with new coefficients should be generated. (See TAOS application note).

Counts per Lux (CPL) needs to be calculated only when ATIME or AGAIN is changed, otherwise it remains a constant. The first segment of the equation (Lux1) covers fluorescent and incandescent light. The second segment (Lux2) covers dimmed incandescent light. The final lux is the maximum of Lux1, Lux2, or 0.

CPL = (ATIME_ms × AGAINx) / 20
Lux1 = (C0DATA – 1.75 × C1DATA) / CPL
Lux2 = (0.63 × C0DATA – 1.00 × C1DATA) / CPL
Lux = MAX(Lux1, Lux2, 0)

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Proximity Detection

Proximity detection is accomplished by measuring the amount of IR energy, from the internal IR LED, reflected off an object to determine its distance. The internal proximity IR LED is driven by the integrated proximity LED current driver as shown in Figure 8.

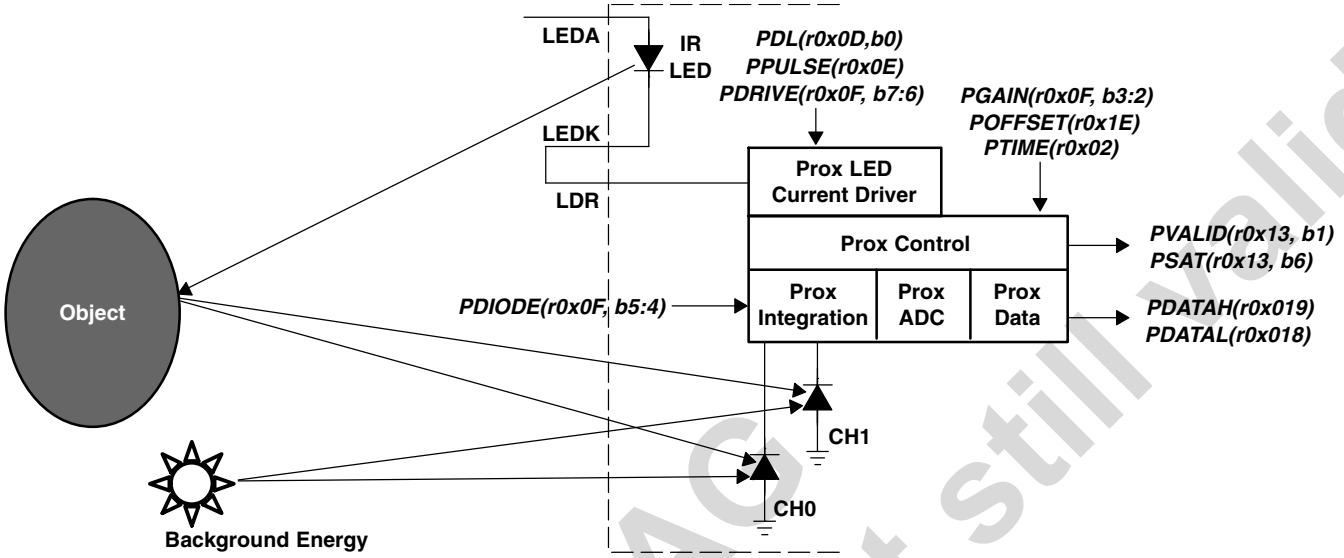


Figure 8. Proximity Detection

The LED current driver, output on the LDR terminal, provides a regulated current sink that eliminates the need for an external current limiting resistor. The combination of proximity LED drive strength (PDRIVE) and proximity drive level (PDL) determine the drive current. PDRIVE sets the drive current to 116 mA, 58 mA, 29 mA, or 14.5 mA when PDL is not asserted. However, when PDL is asserted, the drive current is reduced by a factor of 9.

Referring to the Detailed State Machine figure, the LED current driver pulses the IR LED as shown in Figure 9 during the Prox Accum state. Figure 9 also illustrates that the LED On pulse has a fixed width of 7.3 µs and period of 16.0 µs. So, in addition to setting the proximity drive current, 1 to 255 proximity pulses (PPULSE) can be programmed. When deciding on the number of proximity pulses, keep in mind that the signal increases proportionally to PPULSE, while noise increases by the square root of PPULSE.

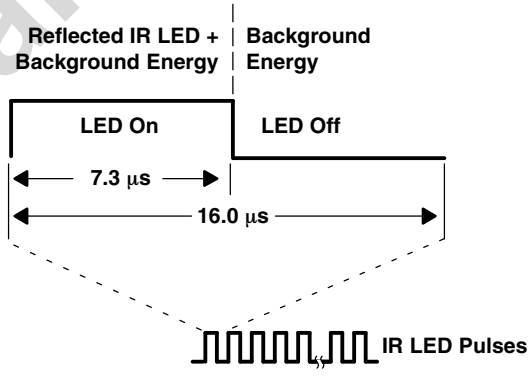


Figure 9. Proximity LED Current Driver Waveform

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Figure 8 illustrates light rays emitting from the internal IR LED, reflecting off an object, and being absorbed by the CH0 and CH1 photodiodes. The proximity diode selector (PDIODE) determines which of the two photodiodes is used for a given proximity measurement. Note that neither photodiode is selected when the device first powers up, so PDIODE must be set for proximity detection to work.

Referring again to Figure 9, the reflected IR LED and the background energy is integrated during the LED On time, then during the LED Off time, the integrated background energy is subtracted from the LED On time energy, leaving the IR LED energy to accumulate from pulse to pulse. The proximity gain (PGAIN) determines the integration rate, which can be programmed to 1×, 2×, 4×, or 8× gain. At power up, PGAIN defaults to 1× gain, which is recommended for most applications. For reference, PGAIN equal to 8× is comparable to the TMD2771's 1× gain setting. During LED On time integration, the proximity saturation bit in the Status register (0x13) will be set if the integrator saturates. This condition can occur if the proximity gain is set too high for the lighting conditions, such as in the presence of bright sunlight. Once asserted, PSAT will remain set until a special function proximity interrupt clear command is received from the host (see command register).

After the programmed number of proximity pulses have been generated, the proximity ADC converts and scales the proximity measurement to a 16-bit value, then stores the result in two 8-bit proximity data (PDATAx) registers. ADC scaling is controlled by the proximity ADC conversion time (PTIME) which is programmable from 1 to 256 2.73-ms time units. However, depending on the application, scaling the proximity data will equally scale any accumulated noise. Therefore, in general, it is recommended to leave PTIME at the default value of one 2.73-ms ADC conversion time (0xFF).

In many practical proximity applications, a number of optical system and environmental conditions can produce an offset in the proximity measurement result. To counter these effects, a proximity offset (POFFSET) is provided which allows the proximity data to be shifted positive or negative. Additional information on the use of the proximity offset feature is provided in available TAOS application notes.

Once the first proximity cycle has completed, the proximity valid (PVALID) bit in the Status register will be set and remain set until the proximity detection function is disabled (PEN).

For additional information on using the proximity detection function behind glass and for optical system design guidance, please see available TAOS application notes.

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Interrupts

The interrupt feature simplifies and improves system efficiency by eliminating the need to poll the sensor for light intensity or proximity values outside of a user-defined range. While the interrupt function is always enabled and its status is available in the status register (0x13), the output of the interrupt state can be enabled using the proximity interrupt enable (PIEN) or ALS interrupt enable (AIEN) fields in the enable register (0x00).

Four 16-bit interrupt threshold registers allow the user to set limits below and above a desired light level and proximity range. An interrupt can be generated when the ALS CH0 data (C0DATA) falls outside of the desired light level range, as determined by the values in the ALS interrupt low threshold registers (AILTx) and ALS interrupt high threshold registers (AIHTx). Likewise, an out-of-range proximity interrupt can be generated when the proximity data (PDATA) falls below the proximity interrupt low threshold (PILTx) or exceeds the proximity interrupt high threshold (PIHTx).

It is important to note that the thresholds are evaluated in sequence, first the low threshold, then the high threshold. As a result, if the low threshold is set above the high threshold, the high threshold is ignored and only the low threshold is evaluated.

To further control when an interrupt occurs, the device provides a persistence filter. The persistence filter allows the user to specify the number of consecutive out-of-range ALS or proximity occurrences before an interrupt is generated. The persistence filter register (0x0C) allows the user to set the ALS persistence filter (APERS) and the proximity persistence filter (PPERS) values. See the persistence filter register for details on the persistence filter values. Once the persistence filter generates an interrupt, it will continue until a special function interrupt clear command is received (see command register).

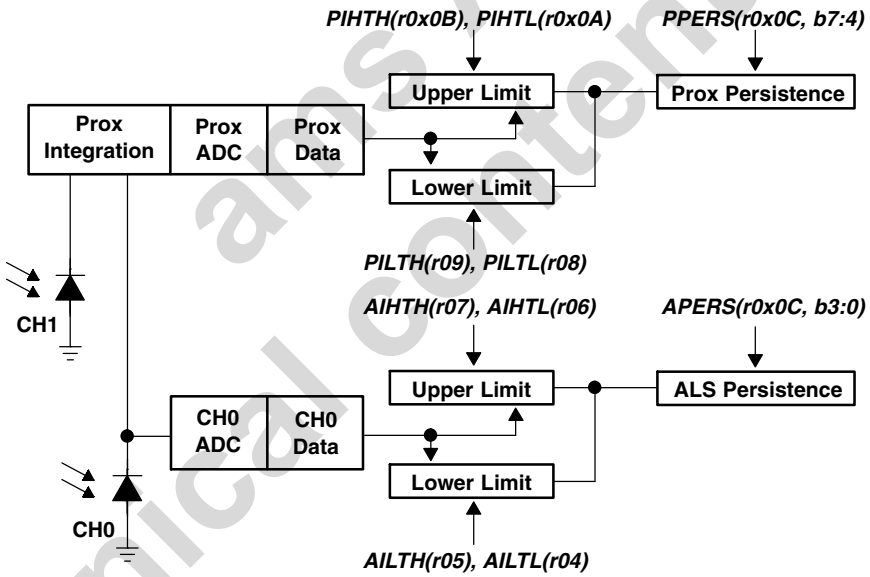


Figure 10. Programmable Interrupt

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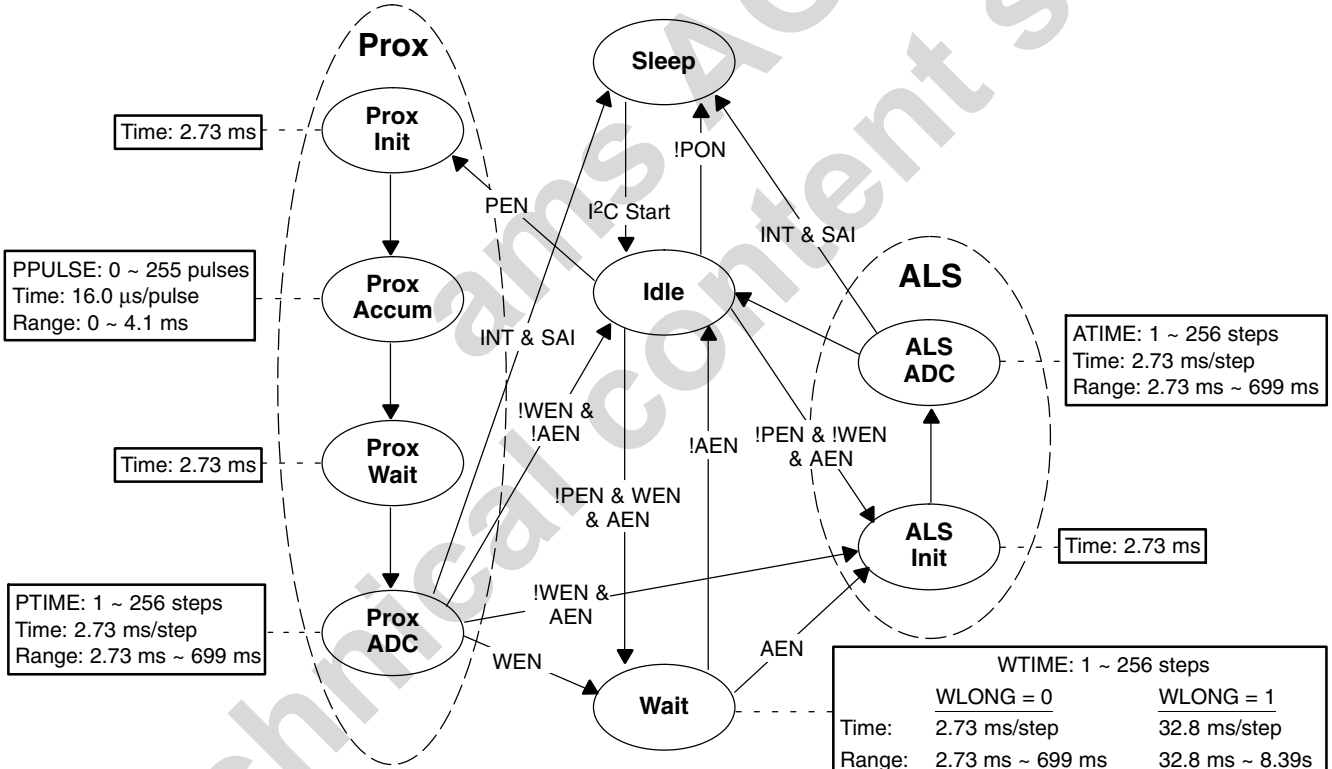
System State Machine Timing

The system state machine shown in Figure 5 provides an overview of the states and state transitions that provide system control of the device. This section highlights the programmable features, which affect the state machine cycle time, and provides details to determine system level timing.

When the proximity detection feature is enabled (PEN), the state machine transitions through the Prox Init, Prox Accum, Prox Wait, and Prox ADC states. The Prox Init and Prox Wait times are a fixed 2.73 ms, whereas the Prox Accum time is determined by the number of proximity LED pulses (PPULSE) and the Prox ADC time is determined by the integration time (PTIME). The formulas to determine the Prox Accum and Prox ADC times are given in the associated boxes in Figure 10. If an interrupt is generated as a result of the proximity cycle, it will be asserted at the end of the Prox ADC state and transition to the Sleep state if SAI is enabled.

When the power management feature is enabled (WEN), the state machine will transition in turn to the Wait state. The wait time is determined by WLONG, which extends normal operation by 12× when asserted, and WTIME. The formula to determine the wait time is given in the box associated with the Wait state in Figure 9.

When the ALS feature is enabled (AEN), the state machine will transition through the ALS Init and ALS ADC states. The ALS Init state takes 2.73 ms, while the ALS ADC time is dependent on the integration time (ATIME). The formula to determine ALS ADC time is given in the associated box in Figure 9. If an interrupt is generated as a result of the ALS cycle, it will be asserted at the end of the ALS ADC state and transition to the Sleep state if SAI is enabled.



Note: PON, PEN, WEN, AEN, and SAI are fields in the Enable register (0x00).

Figure 11. Detailed State Diagram

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Power Management

Power consumption can be managed with the Wait state, because the Wait state typically consumes only 90 µA of I_{DD} current. An example of the power management feature is given below. With the assumptions provided in the example, average I_{DD} is estimated to be 176 µA.

Table 1. Power Management

SYSTEM STATE MACHINE STATE	PROGRAMMABLE PARAMETER	PROGRAMMED VALUE	DURATION	TYPICAL CURRENT
Prox Init			2.73 ms	0.195 mA
Prox Accum	PPULSE	0x04	0.064 ms	
Prox Accum – LED On			0.029 ms (Note 1)	103 mA
Prox Accum – LED OFF			0.035 ms (Note 2)	0.195 mA
Prox Wait			2.73 ms	0.195 mA
Prox ADC	PTIME	0xFF	2.73 ms	0.195 mA
Wait	WTIME	0xEE	49.2 ms	0.090 mA
	WLONG	0		
ALS Init			2.73 ms	0.195 mA
ALS ADC	ATIME	0xEE	49.2 ms	0195 mA

NOTES: 1. Prox Accum – LED On time = 7.3 µs per pulse × 4 pulses = 29.3µs = 0.029 ms
2. Prox Accum – LED Off time = 8.7 µs per pulse × 4 pulses = 34.7µs = 0.035 ms

Average I_{DD} Current = ((0.029 × 103) + (0.035 x 0.195) + (2.73 × 0.195) +
(49.2 × 0.090) + (49.2 × 0.195) + (2.73 × 0.195 × 3)) / 109 ≈ 176 µA

Keeping with the same programmed values as the example, Table 2 shows how the average I_{DD} current is affected by the Wait state time, which is determined by WEN, WTIME, and WLONG. Note that the worst-case current occurs when the Wait state is not enabled.

Table 2. Average I_{DD} Current

WEN	WTIME	WLONG	WAIT STATE	AVERAGE I_{DD} CURRENT
0	n/a	n/a	0 ms	245 µA
1	0xFF	0	2.73 ms	238 µA
1	0xEE	0	49.2 ms	175 µA
1	0x00	0	699 ms	102 µA
1	0x00	1	8389 ms	91 µA

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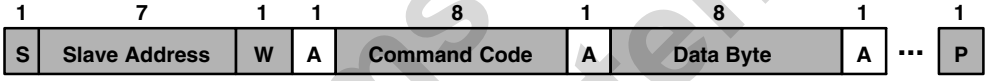
I²C Protocol

Interface and control are accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The devices support the 7-bit I²C addressing protocol.

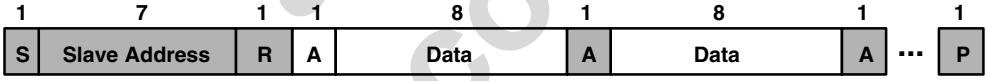
The I²C standard provides for three types of bus transaction: read, write, and a combined protocol (Figure 13). During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at http://www.i2c–bus.org/references/.

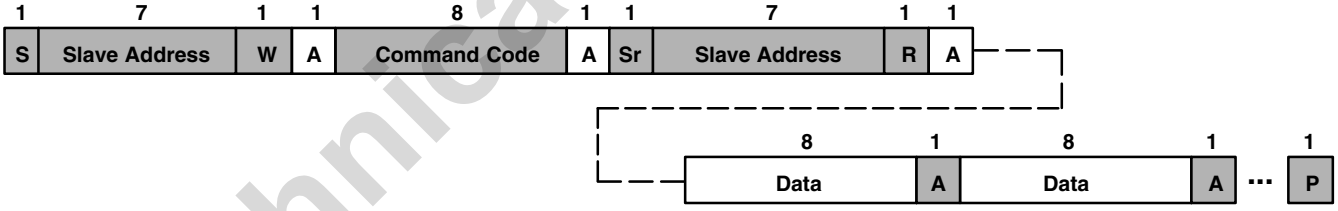
A Acknowledge (0)
N Not Acknowledged (1)
P Stop Condition
R Read (1)
S Start Condition
Sr Repeated Start Condition
W Write (0)
... Continuation of protocol
Master-to-Slave
Slave-to-Master



I²C Write Protocol



I²C Read Protocol



I²C Read Protocol — Combined Format

Figure 12. I²C Protocols

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Register Set

The device is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Table 1.

Table 3. Register Address

ADDRESS	RESISTER NAME	R/W	REGISTER FUNCTION	RESET VALUE
––	COMMAND	W	Specifies register address	0x00
0x00	ENABLE	R/W	Enables states and interrupts	0x00
0x01	ATIME	R/W	ALS time	0xFF
0x02	PTIME	R/W	Proximity time	0xFF
0x03	WTIME	R/W	Wait time	0xFF
0x04	AILTL	R/W	ALS interrupt low threshold low byte	0x00
0x05	AILTH	R/W	ALS interrupt low threshold high byte	0x00
0x06	AIHTL	R/W	ALS interrupt high threshold low byte	0x00
0x07	AIHTH	R/W	ALS interrupt high threshold high byte	0x00
0x08	PILTL	R/W	Proximity interrupt low threshold low byte	0x00
0x09	PILTH	R/W	Proximity interrupt low threshold high byte	0x00
0x0A	PIHTL	R/W	Proximity interrupt high threshold low byte	0x00
0x0B	PIHTH	R/W	Proximity interrupt high threshold high byte	0x00
0x0C	PERS	R/W	Interrupt persistence filters	0x00
0x0D	CONFIG	R/W	Configuration	0x00
0x0E	PPULSE	R/W	Proximity pulse count	0x00
0x0F	CONTROL	R/W	Control register	0x00
0x11	REVISION	R	Die revision number	Rev Num.
0x12	ID	R	Device ID	ID
0x13	STATUS	R	Device status	0x00
0x14	C0DATA	R	CH0 ADC low data register	0x00
0x15	C0DATAH	R	CH0 ADC high data register	0x00
0x16	C1DATA	R	CH1 ADC low data register	0x00
0x17	C1DATAH	R	CH1 ADC high data register	0x00
0x18	PDATAL	R	Proximity ADC low data register	0x00
0x19	PDATAH	R	Proximity ADC high data register	0x00
0x1E	POFFSET	R/W	Proximity offset register	0x00

The mechanics of accessing a specific register depends on the specific protocol used. See the section on I^2C protocols on the previous pages. In general, the COMMAND register is written first to specify the specific control/status register for following read/write operations.

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Command Register

The command registers specifies the address of the target register for future write and read operations.

Table 4. Command Register

	7	6	5	4	3	2	1	0	
COMMAND	**COMMAND**	**TYPE**			**ADD**				**Reset 0x00**

FIELD	BITS	DESCRIPTION	
COMMAND	7	Select Command Register. Must write as 1 when addressing COMMAND register.	
TYPE	6:5	Selects type of transaction to follow in subsequent data transfers:	
		FIELD VALUE	**DESCRIPTION**
		00	Repeated byte protocol transaction
		01	Auto-increment protocol transaction
		10	Reserved — Do not use
		11	Special function — See description below
		Transaction type 00 will repeatedly read the same register with each data access. Transaction type 01 will provide an auto-increment function to read successive register bytes.	
ADD	4:0	Address field/special function field. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control-status-register for following write and read transactions. The field values listed below apply only to special function commands:	
		FIELD VALUE	**DESCRIPTION**
		00000	Normal — no action
		00101	Proximity interrupt clear
		00110	ALS interrupt clear
		00111	Proximity and ALS interrupt clear
		other	Reserved — Do not write
		ALS/Proximity Interrupt Clear clears any pending ALS/Proximity interrupt. This special function is self clearing.	

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Enable Register (0x00)

The ENABLE register is used to power the device on/off, enable functions, and interrupts.

Table 5. Enable Register

	7	6	5	4	3	2	1	0	
ENABLE	**Reserved**	**SAI**	**PIEN**	**AIEN**	**WEN**	**PEN**	**AEN**	**PON**	**Reset 0x00**

FIELD	BITS	DESCRIPTION
Reserved	7	Reserved. Write as 0.
SAI	6	Sleep after interrupt. When asserted, the device will power down at the end of a proximity or ALS cycle if an interrupt has been generated.
PIEN	5	Proximity interrupt mask. When asserted, permits proximity interrupts to be generated.
AIEN	4	ALS interrupt mask. When asserted, permits ALS interrupts to be generated.
WEN	3	Wait Enable. This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
PEN	2	Proximity enable. This bit activates the proximity function. Writing a 1 enables proximity. Writing a 0 disables proximity.
AEN	1	ALS Enable. This bit actives the two channel ADC. Writing a 1 activates the ALS. Writing a 0 disables the ALS.
PON	0	Power ON. This bit activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator.

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ALS Time Register (0x01)

The ALS time register controls the internal integration time of the ALS channel ADCs in 2.73 ms increments. Upon power up, the ALS time register is set to 0xFF.

Table 6. ALS Integration Time Register

FIELD	BITS	DESCRIPTION			
ATIME	7:0	VALUE	INTEG_CYCLES	TIME	MAX COUNT
		0xFF	1	2.73 ms	1024
		0xF6	10	27.3 ms	10240
		0xDB	37	101 ms	37888
		0xC0	64	175 ms	65535
		0x00	256	699 ms	65535

Proximity Time Register (0x02)

The proximity time register controls the integration time of the proximity ADC in 2.73 ms increments. Upon power up, the proximity time register is set to 0xFF. It is recommended that this register be programmed to a value of 0xFF (1 integration cycle).

Table 7. Proximity Integration Time Control Register

FIELD	BITS	DESCRIPTION			
PTIME	7:0	VALUE	INTEG_CYCLES	TIME	MAX COUNT
		0xFF	1	2.73 ms	1023

Wait Time Register (0x03)

Wait time is set 2.73 ms increments unless the WLONG bit is asserted in which case the wait times are 12× longer. WTIME is programmed as a 2's complement number. Upon power up, the wait time register is set to 0xFF.

Table 8. Wait Time Register

FIELD	BITS	DESCRIPTION			
WTIME	7:0	REGISTER VALUE	WAIT TIME	TIME (WLONG = 0)	TIME (WLONG = 1)
		0xFF	1	2.73 ms	0.033 sec
		0xB6	74	202 ms	2.4 sec
		0x00	256	699 ms	8.4 sec

NOTE: The Proximity Wait Time Register should be configured before PEN and/or AEN is/are asserted.

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ALS Interrupt Threshold Registers (0x04 – 0x07)

The ALS interrupt threshold registers provides the values to be used as the high and low trigger points for the comparison function for interrupt generation. If C0DATA crosses below the low threshold specified, or above the higher threshold, an interrupt is asserted on the interrupt pin.

Table 9. ALS Interrupt Threshold Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
AILTL	0x04	7:0	ALS low threshold lower byte
AILTH	0x05	7:0	ALS low threshold upper byte
AIHTL	0x06	7:0	ALS high threshold lower byte
AIHTH	0x07	7:0	ALS high threshold upper byte

Proximity Interrupt Threshold Registers (0x08 – 0x0B)

The proximity interrupt threshold registers provide the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by proximity channel crosses below the lower threshold specified, or above the higher threshold, an interrupt is signaled to the host processor.

Table 10. Proximity Interrupt Threshold Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
PILTL	0x08	7:0	Proximity low threshold lower byte
PILTH	0x09	7:0	Proximity low threshold upper byte
PIHTL	0x0A	7:0	Proximity high threshold lower byte
PIHTH	0x0B	7:0	Proximity high threshold upper byte

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Persistence Filter Register (0x0C)

The persistence filter register controls the interrupt capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after every ADC cycle or if the ADC cycle has produced a result that is outside of the values specified by threshold register for some specified amount of time. Separate filtering is provided for proximity and ALS functions. ALS interrupts are generated using C0DATA.

Table 11. Persistence Filter Register

	7	6	5	4	3	2	1	0	
PERS	PPERS				APERS				Reset 0x00

FIELD	BITS	DESCRIPTION		
PPERS	7:4	Proximity interrupt persistence filter. Controls rate of proximity interrupt to the host processor.		
		FIELD VALUE	MEANING	INTERRUPT PERSISTENCE FUNCTION
		0000	–––	Every proximity cycle generates an interrupt
		0001	1	1 proximity value out of range
		0010	2	2 consecutive proximity values out of range
		...	...	...
		1111	15	15 consecutive proximity values out of range
APERS	3:0	ALS Interrupt persistence filter. Controls rate of ALS interrupt to the host processor.		
		FIELD VALUE	MEANING	INTERRUPT PERSISTENCE FUNCTION
		0000	Every	Every ALS cycle generates an interrupt
		0001	1	1 value outside of threshold range
		0010	2	2 consecutive values out of range
		0011	3	3 consecutive values out of range
		0100	5	5 consecutive values out of range
		0101	10	10 consecutive values out of range
		0110	15	15 consecutive values out of range
		0111	20	20 consecutive values out of range
		1000	25	25 consecutive values out of range
		1001	30	30 consecutive values out of range
		1010	35	35 consecutive values out of range
		1011	40	40 consecutive values out of range
		1100	45	45 consecutive values out of range
		1101	50	50 consecutive values out of range
		1110	55	55 consecutive values out of range
		1111	60	60 consecutive values out of range

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Configuration Register (0x0D)

The configuration register sets the proximity LED drive level, wait long time, and ALS gain level.

Table 12. Configuration Register

	7	6	5	4	3	2	1	0	
CONFIG	Reserved					AGL	WLONG	PDL	Reset 0x00

FIELD	BITS	DESCRIPTION
Reserved	7:3	Reserved. Write as 0.
AGL	2	ALS gain level. When asserted, the 1× and 8× ALS gain (AGAIN) modes are scaled by 0.16. Otherwise, AGAIN is scaled by 1. Do not use with AGAIN greater than 8×.
WLONG	1	Wait Long. When asserted, the wait cycles are increased by a factor 12× from that programmed in the WTIME register.
PDL	0	Proximity drive level. When asserted, the proximity LDR drive current is reduced by 9.

Proximity Pulse Count Register (0x0E)

The proximity pulse count register sets the number of proximity pulses that the LDR pin will generate during the Prox Accum state. The pulses are generated at a 62.5-kHz rate.

Table 13. Proximity Pulse Count Register

	7	6	5	4	3	2	1	0	
PPULSE	PPULSE								Reset 0x00

FIELD	BITS	DESCRIPTION
PPULSE	7:0	Proximity Pulse Count. Specifies the number of proximity pulses to be generated.

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Control Register (0x0F)

The Control register provides eight bits of miscellaneous control to the analog block. These bits typically control functions such as gain settings and/or diode selection.

Table 14. Control Register

	7	6	5	4	3	2	1	0	
CONTROL	**PDRIVE**		**PDIODE**		**PGAIN**		**AGAIN**		**Reset 0x00**

FIELD	BITS	DESCRIPTION		
PDRIVE (Note 1)	7:6	Proximity LED Drive Strength.		
		FIELD VALUE	**LED STRENGTH — PDL = 0**	**LED STRENGTH — PDL = 1**
		00	*100 mA*	*11.1 mA*
		01	*50 mA*	*5.6 mA*
		10	*25 mA*	*2.8 mA*
		11	*12.5 mA*	*1.4 mA*
PDIODE	5:4	Proximity Diode Selector.		
		FIELD VALUE	**DIODE SELECTION**	
		00	Proximity uses neither diode	
		01	Proximity uses the CH0 diode	
		10	Proximity uses the CH1 diode	
		11	Reserved — Do not write	
PGAIN	3:2	Proximity Gain.		
		FIELD VALUE	**PROXIMITY GAIN VALUE**	
		00	1× gain	
		01	2× gain	
		10	4× gain	
		11	8× gain	
AGAIN	1:0	ALS Gain.		
		FIELD VALUE	**ALS GAIN VALUE**	
		00	1× gain	
		01	8× gain	
		10	16× gain	
		11	120× gain	

NOTE 1: LED STRENGTH values (italic) are nominal operating values. Specifications can be found in the Proximity Characteristics table.

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Revision Register (0x11)

The Revision register shows the silicon revision number. It is a read-only register and shows the revision level of the silicon used internally.

Table 15. Revision Register

	7	6	5	4	3	2	1	0	
REVISION	Reserved				DIE_REV				Reset Rev Num

FIELD	BITS	DESCRIPTION	
Reserved	7:4	Reserved	Bits read as 0
DIE_REV	3:0	Die revision number	Die revision number

ID Register (0x12)

The ID Register provides the value for the part number. The ID register is a read-only register.

Table 16. ID Register

	7	6	5	4	3	2	1	0	
ID	ID								Reset ID

FIELD	BITS	DESCRIPTION	
ID	7:0	Part number identification	0x30 = TMD27721
			0x39 = TMD27723

Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

Table 17. Status Register

	7	6	5	4	3	2	1	0	
STATUS	Reserved	PSAT	PINT	AINT	Reserved		PVALID	AVALID	Reset 0x00

FIELD	BIT	DESCRIPTION
Reserved	7	Reserved. Bit reads as 0.
PSAT	6	Proximity Saturation. Indicates that the proximity measurement saturated.
PINT	5	Proximity Interrupt. Indicates that the device is asserting a proximity interrupt.
AINT	4	ALS Interrupt. Indicates that the device is asserting an ALS interrupt.
Reserved	3:2	Reserved. Bits read as 0.
PVALID	1	Proximity Valid. Indicates that the proximity channel has completed an integration cycle after PEN has been asserted.
AVALID	0	ALS Valid. Indicates that the ALS channels have completed an integration cycle after AEN has been asserted.

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ADC Channel Data Registers (0x14 – 0x17)

ALS data is stored as two 16-bit values. To ensure the data is read correctly, a two-byte read I^2C transaction should be used with auto increment protocol bits set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored in a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

Table 18. ADC Channel Data Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
C0DATA	0x14	7:0	ALS CH0 data low byte
C0DATAH	0x15	7:0	ALS CH0 data high byte
C1DATA	0x16	7:0	ALS CH1 data low byte
C1DATAH	0x17	7:0	ALS CH1 data high byte

Proximity Data Registers (0x18 – 0x19)

Proximity data is stored as a 16-bit value. To ensure the data is read correctly, a two-byte read I^2C transaction should be utilized with auto increment protocol bits set in the command register. With this operation, when the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if the next ADC cycle ends between the reading of the lower and upper registers.

Table 19. Proximity Data Registers

REGISTER	ADDRESS	BITS	DESCRIPTION
PDATAL	0x18	7:0	Proximity data low byte
PDATAH	0x19	7:0	Proximity data high byte

Proximity Offset Register (0x1E)

The 8-bit proximity offset register provides compensation for proximity offsets caused by device variations, optical crosstalk, and other environmental factors. Proximity offset is a sign-magnitude value where the sign bit, bit 7, determines if the offset is negative (bit 7 = 0) or positive (bit 7 = 1). At power up, the register is set to 0x00. The magnitude of the offset compensation depends on the proximity gain (PGAIN), proximity LED drive strength (PDRIVE), and the number of proximity pulses (PPULSE). Because a number of environmental factors contribute to proximity offset, this register is best suited for use in an adaptive closed-loop control system. See available TAOS application notes for proximity offset register application information.

Table 20. Proximity Offset Register

	7	6	5	4	3	2	1	0	
POFFSET	SIGN	MAGNITUDE							Reset 0x00

FIELD	BIT	DESCRIPTION
SIGN	7	Proximity Offset Sign. The offset sign shifts the proximity data negative when equal to 0 and positive when equal to 1.
MAGNITUDE	6:0	Proximity Offset Magnitude. The offset magnitude shifts the proximity data positive or negative, depending on the proximity offset sign. The actual amount of the shift depends on the proximity gain (PGAIN), proximity LED drive strength (PDRIVE), and the number of proximity pulses (PPULSE).

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APPLICATION INFORMATION: HARDWARE

LED Driver Pin with Proximity Detection

In a proximity sensing system, the included IR LED can be pulsed with more than 100 mA of rapidly switching current, therefore, a few design considerations must be kept in mind to get the best performance. The key goal is to reduce the power supply noise coupled back into the device during the LED pulses. Averaging of multiple proximity samples is recommended to reduce the proximity noise.

The first recommendation is to use two power supplies; one for the device V_{DD} and the other for the IR LED. In many systems, there is a quiet analog supply and a noisy digital supply. By connecting the quiet supply to the V_{DD} pin and the noisy supply to the LEDA pin, the key goal can be met. Place a 1-µF low-ESR decoupling capacitor as close as possible to the V_{DD} pin and another at the LEDA pin, and at least 10-µF of bulk capacitance to supply the 100-mA current surge. This may be distributed as two 4.7 µF capacitors.

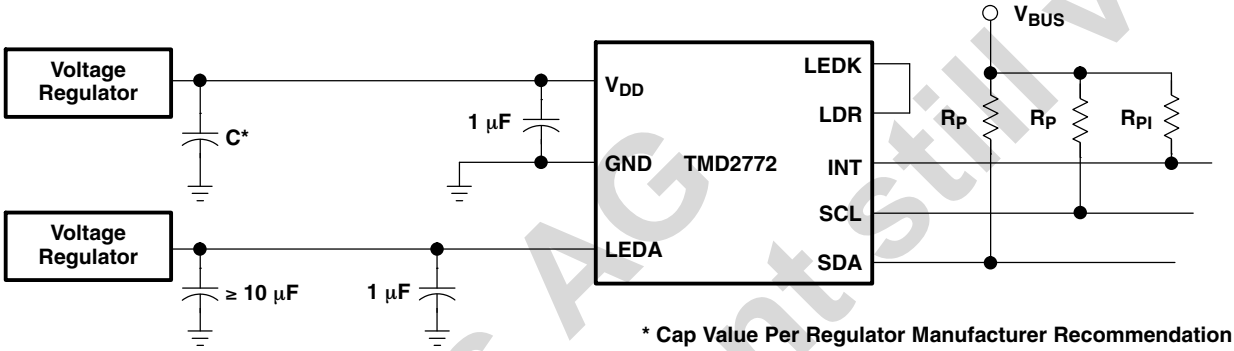


Figure 13. Proximity Sensing Using Separate Power Supplies

If it is not possible to provide two separate power supplies, the device can be operated from a single supply. A 22-Ω resistor in series with the V_{DD} supply line and a 1-µF low ESR capacitor effectively filter any power supply noise. The previous capacitor placement considerations apply.

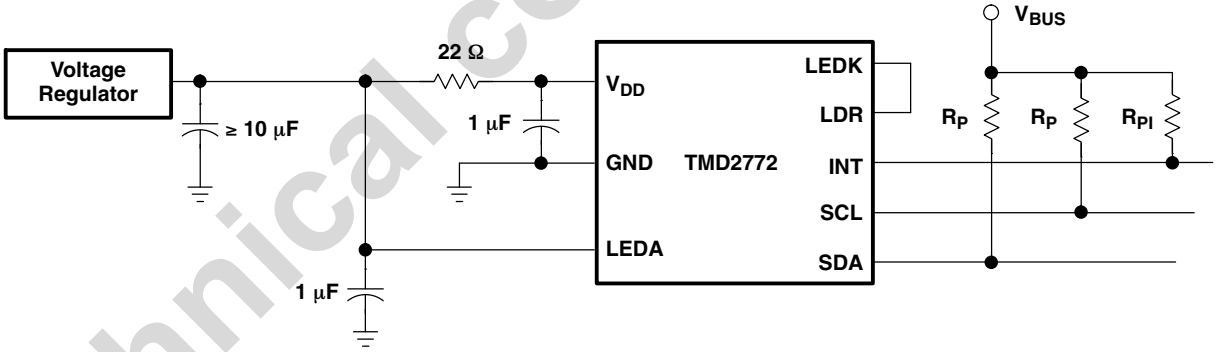


Figure 14. Proximity Sensing Using Single Power Supply

V_{BUS} in the above figures refers to the I^2C bus voltage which is either V_{DD} or 1.8 V. Be sure to apply the specified I^2C bus voltage shown in the Available Options table for the specific device being used.

The I^2C signals and the Interrupt are open-drain outputs and require pull–up resistors. The pull-up resistor (R_P) value is a function of the I^2C bus speed, the I^2C bus voltage, and the capacitive load. The TAOS EVM running at 400 kbps, uses 1.5-kΩ resistors. A 10-kΩ pull-up resistor (R_{PI}) can be used for the interrupt line.

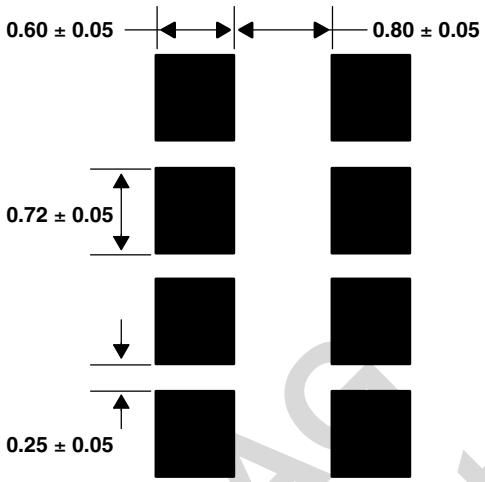
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APPLICATION INFORMATION: HARDWARE

PCB Pad Layout

Suggested PCB pad layout guidelines for the surface mount module are shown in Figure 15. Flash Gold is recommended surface finish for the landing pads.



NOTES: A. All linear dimensions are in mm.
B. This drawing is subject to change without notice.

Figure 15. Suggested Module PCB Layout

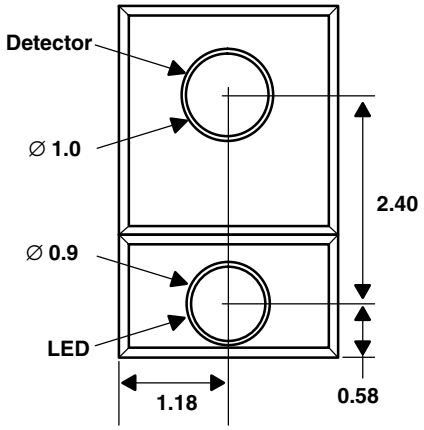
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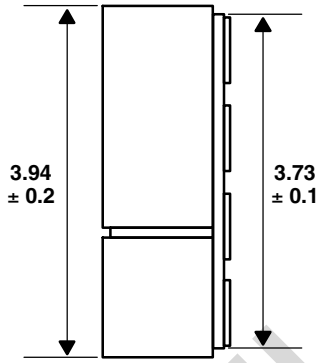
PACKAGE INFORMATION

MODULE **Dual Flat No-Lead**

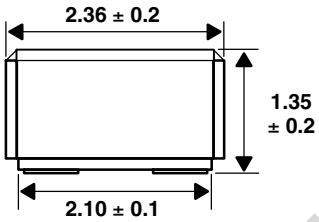
TOP VIEW



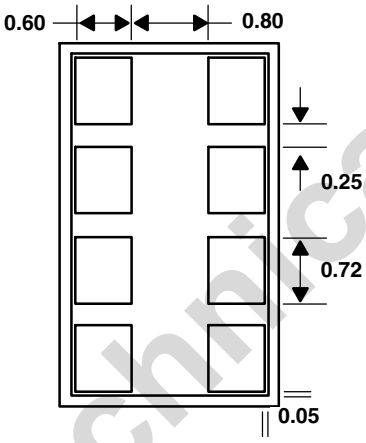
SIDE VIEW



END VIEW



BOTTOM VIEW



Lead Free

NOTES: A. All linear dimensions are in millimeters. Dimension tolerance is ± 0.05 mm unless otherwise noted.
B. Contacts are copper with NiPdAu plating.
C. This package contains no lead (Pb).
D. This drawing is subject to change without notice.

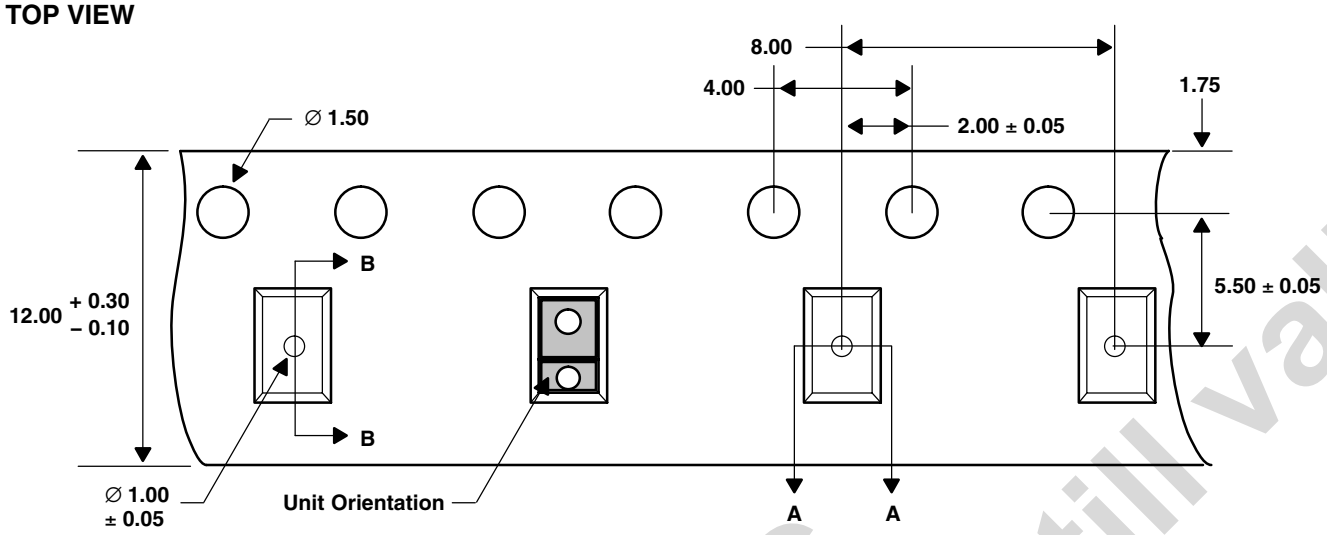
Figure 16. Module Packaging Configuration

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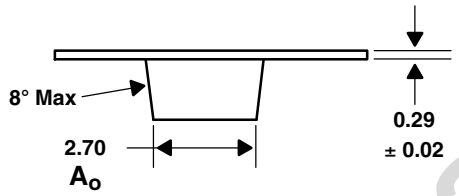
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CARRIER TAPE AND REEL INFORMATION

TOP VIEW



DETAIL A



DETAIL B



NOTES:
A. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
B. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
C. Symbols on drawing A_o, B_o, and K_o are defined in ANSI EIA Standard 481–B 2001.
D. Each reel is 330 millimeters in diameter and contains 2500 parts.
E. TAOS packaging tape and reel conform to the requirements of EIA Standard 481–B.
F. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
G. This drawing is subject to change without notice.

Figure 17. Module Carrier Tape

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SOLDERING INFORMATION

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Table 21. Solder Reflow Profile

PARAMETER	REFERENCE	DEVICE
Average temperature gradient in preheating		2.5°C/sec
Soak time	t_{soak}	2 to 3 minutes
Time above 217°C (T_1)	t_1	Max 60 sec
Time above 230°C (T_2)	t_2	Max 50 sec
Time above T_{peak} –10°C (T_3)	t_3	Max 10 sec
Peak temperature in reflow	T_{peak}	260°C
Temperature gradient in cooling		Max –5°C/sec

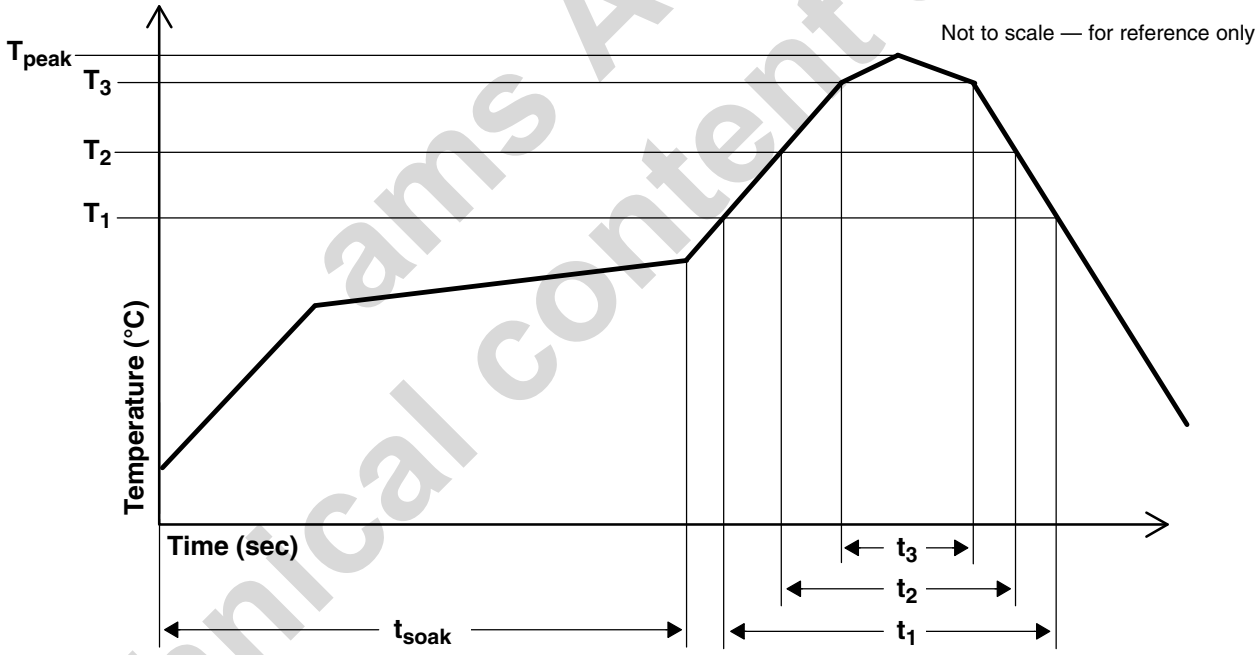


Figure 18. Solder Reflow Profile Graph

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STORAGE INFORMATION

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

Shelf Life:	12 months
Ambient Temperature:	< 40°C
Relative Humidity:	< 90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

Floor Life:	168 hours
Ambient Temperature:	< 30°C
Relative Humidity:	< 60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

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Green (RoHS & no Sb/Br) TAOS defines *Green* to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

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