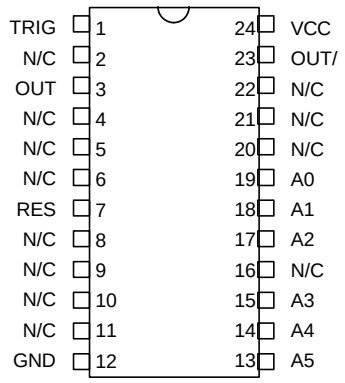
6-BIT PROGRAMMABLE PULSE GENERATOR (SERIES PPG36F)

data delay devices, inc.

FEATURES

- Digitally programmable in 64 steps
- Monotonic pulse-width-vs-address variation
- Rising edge triggered
- Two separate outputs: inverting & non-inverting
- Precise and stable pulse width
- Input & outputs fully TTL interfaced & buffered
- 10 T^2L fan-out capability
- Fits standard 24-pin DIP socket
- Auto-insertable

PACKAGES



PPG36F-xx	DIP	PPG36F-xxM	Military DIP
PPG36F-xxC4	Gull-Wing	PPG36F-xxMC4	Military Gull-Wing

FUNCTIONAL DESCRIPTION

The PPG36F-series device is a 6-bit digitally programmable pulse generator. The width, PW_A, depends on the address code (A5-A0) according to the following formula:

$$PW_A = PW_0 + T_{INC} * A$$

where A is the address code, T_{INC} is the incremental pulse width of the device, and PW_0 is the inherent pulse width of the device. The incremental width is specified by the dash number of the device and can range from 0.5ns through 10ns, inclusively. RESET is held LOW during normal operation. When it is brought HIGH, OUT and OUT/ are forced into LOW and HIGH states, respectively, and the unit is ready for the next trigger input. The address is not latched and must remain asserted while the output pulse is active.

PIN DESCRIPTIONS

TRIG	Trigger Input
OUT	Non-inverted Output
OUT/	Inverted Output
A0-A5	Address Bits
RES	Reset
VCC	+5 Volts
GND	Ground

SERIES SPECIFICATIONS

- **Programmed pulse width tolerance:** 5% or 2ns, whichever is greater
- **Inherent width (PW_0):** 12ns typical
- **Inherent delay (T_{TO}):** 3.5ns ± 2ns
- **Operating temperature:** 0° to 70° C
- **Supply voltage V_{CC}:** 5VDC ± 5%
- **Supply current:** I_{CC} = 60ma typical

DASH NUMBER SPECIFICATIONS

Part Number	Incremental Width Per Step (ns)	Total Width Change (ns)
PPG36F-.5	0.5 ± 0.3	31.5 ± 2.00
PPG36F-1	1 ± 0.5	63.0 ± 3.15
PPG36F-2	2 ± 0.5	126.0 ± 6.30
PPG36F-3	3 ± 1.0	189.0 ± 9.45
PPG36F-4	4 ± 1.0	252.0 ± 12.6
PPG36F-5	5 ± 1.5	315.0 ± 15.8
PPG36F-6	6 ± 1.5	378.0 ± 18.9
PPG36F-7	7 ± 1.5	441.0 ± 22.1
PPG36F-8	8 ± 2.0	504.0 ± 25.2
PPG36F-9	9 ± 2.0	567.0 ± 28.4
PPG36F-10	10 ± 2.0	630.0 ± 31.5

NOTE: Any dash number between .5 and 10 not shown is also available

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APPLICATION NOTES

DEVICE TIMING

The timing definitions and restrictions for the PPG36F are shown in Figure 1. The unit is activated by a rising edge on the TRIG input. After a time, T_{TO} (called the inherent delay), the rising edge of the pulse appears at OUT. The duration of the pulse is given by the above equation. For the duration of the pulse, the device ignores subsequent triggers. Once the falling edge of the pulse has appeared at OUT, an additional time, T_{OTR}, is required before the device can respond to the next trigger.

At power-up, the state of the PPG36F is unknown. Consequently, after power is applied, the unit may not respond to input triggers for a time equal to the maximum pulse width, PW_T. After this time, the unit will function properly. If your application requires that the device function immediately, issue a quick reset at power-up.

POWER SUPPLY BYPASSING

The PPG36F relies on a stable power supply to produce repeatable pulses within the stated tolerances. A 0.1uf capacitor from VCC to GND, located as close as possible to each VCC pin, is recommended. A wide VCC trace should connect all VCC pins externally, and a clean ground plane should be used.

INCREMENT TOLERANCES

Please note that the increment tolerances listed represent a design goal. Although most increments will fall within tolerance, they are not guaranteed throughout the address range of the unit. Monotonicity is, however, guaranteed over all addresses.

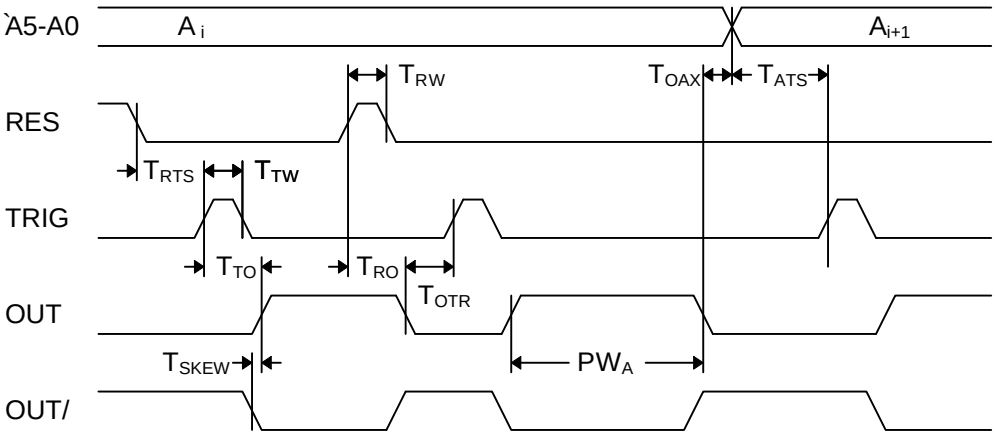


Figure 1: Timing Diagram

DEVICE SPECIFICATIONS

TABLE 1: AC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Total Programmable Pulse Width	PW_T		63		T_{INC}
Inherent Pulse Width	PW_0	8.0	12.0	16.0	ns
Trigger to Output Delay	T_{TO}	1.5	3.5	5.5	ns
Reset to Output Delay	T_{RO}			17.0	ns
Output Skew	T_{SKEW}		1.5		ns
Trigger Pulse Width	T_{TW}	5.0			ns
Reset Pulse Width	T_{RW}	10.0			ns
Reset to Trigger Setup Time	T_{RTS}	9.0			ns
Address to Trigger Setup Time	T_{ATS}	6.0			ns
Output Low to Address Change	T_{OAX}	0.0			ns
Output to Trigger Recovery Time	T_{OTR}	15			% of PW_T

*or 10ns, whichever is greater

TABLE 2: ABSOLUTE MAXIMUM RATINGS

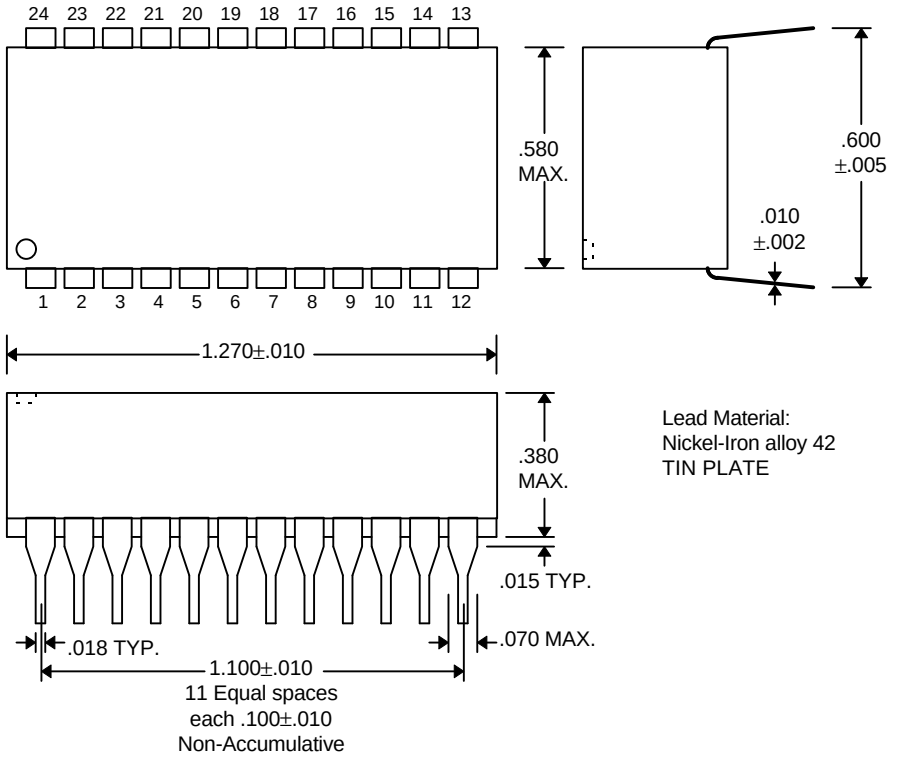
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	-0.3	7.0	V	
Input Pin Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Storage Temperature	T_{STRG}	-55	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

TABLE 3: DC ELECTRICAL CHARACTERISTICS

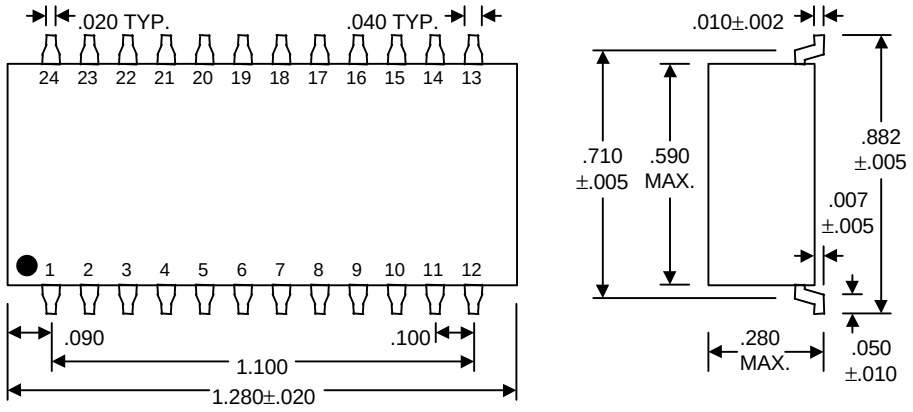
(0C to 70C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
High Level Output Voltage	V_{OH}	2.5	3.4		V	V_{CC} = MIN, I_{OH} = MAX V_{IH} = MIN, V_{IL} = MAX
Low Level Output Voltage	V_{OL}		0.35	0.5	V	V_{CC} = MIN, I_{OL} = MAX V_{IH} = MIN, V_{IL} = MAX
High Level Output Current	I_{OH}			-1.0	mA	
Low Level Output Current	I_{OL}			20.0	mA	
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
Input Clamp Voltage	V_{IK}			-1.2	V	V_{CC} = MIN, I_I = I_{IK}
Input Current at Maximum Input Voltage	I_{IHH}			0.1	mA	V_{CC} = MAX, V_I = 7.0V
High Level Input Current	I_{IH}			20	µA	V_{CC} = MAX, V_I = 2.7V
Low Level Input Current	I_{IL}			-0.6	mA	V_{CC} = MAX, V_I = 0.5V
Short-circuit Output Current	I_{OS}	-60		-150	mA	V_{CC} = MAX
Output High Fan-out				25	Unit	
Output Low Fan-out				12.5	Load	

PACKAGE DIMENSIONS



DIP (PPG36F-xx, PPG36F-xxM)



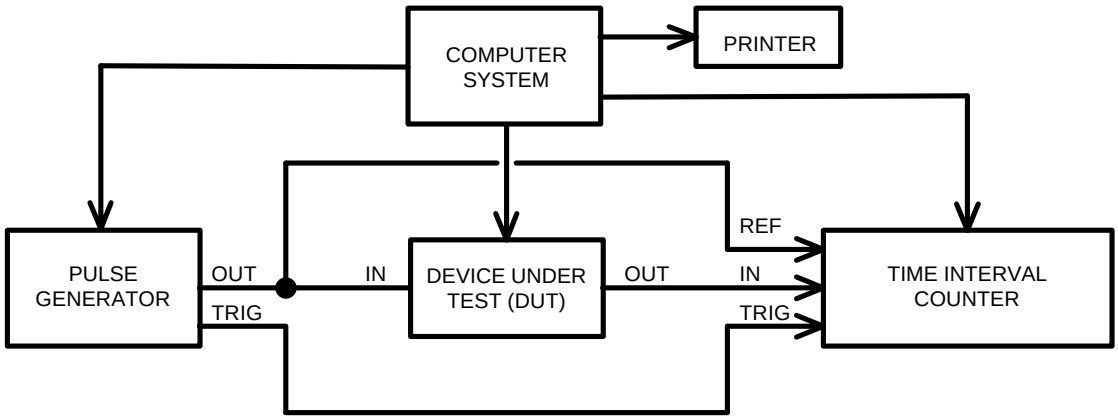
Gull-Wing (PPG36F-xxC4, PPG36F-xxMC4)

DELAY LINE AUTOMATED TESTING

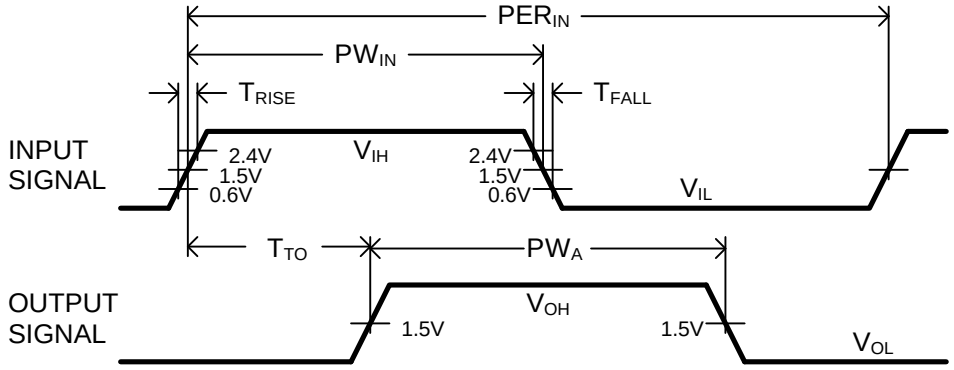
TEST CONDITIONS

INPUT:		**OUTPUT:**	
Ambient Temperature:	$25^oC \pm 3^oC$	**Load:**	1 FAST-TTL Gate
Supply Voltage (Vcc):	5.0V ± 0.1V	**C_{load}:**	5pf ± 10%
Input Pulse:	High = 3.0V ± 0.1V Low = 0.0V ± 0.1V	**Threshold:**	1.5V (Rising & Falling)
Source Impedance:	50Ω Max.		
Rise/Fall Time:	3.0 ns Max. (measured between 0.6V and 2.4V)		
Pulse Width:	PW_{IN} = 10ns		
Period:	PER_{IN} = 2 x Max. Pulse Width		

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Test Setup



Timing Diagram For Testing