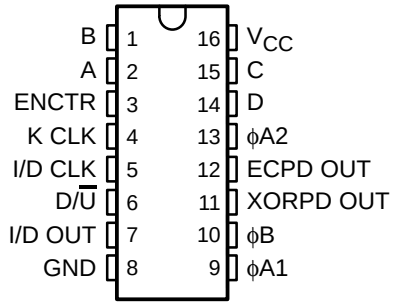
- **Speed of Bipolar FCT, AS, and S, With Significantly Reduced Power Consumption**
- **Digital Design Avoids Analog Compensation Errors**
- **Easily Cascadable for Higher-Order Loops**
- **Useful Frequency Range**
  - **– DC to 110 MHz Typical (K CLK)**
  - **– DC to 70 MHz Typical (I/D CLK)**
- **Dynamically Variable Bandwidth**
- **Very Narrow Bandwidth Attainable**
- **Power-On Reset**
- **Output Capability**
  - **– Standard: XORPD OUT, ECPD OUT**
  - **– Bus Driver: I/D OUT**
- **SCR Latch-Up-Resistant CMOS Process and Circuit Design**
- **Balanced Propagation Delays**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015**

M PACKAGE
(TOP VIEW)



description/ordering information

The CD74ACT297 provides a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. This device contains all the necessary circuits, with the exception of the divide-by-N counter, to build first-order phase-locked loops as shown in Figure 1.

Both exclusive-OR phase detectors (XORPDs) and edge-controlled (ECPD) phase detectors are provided for maximum flexibility.

Proper partitioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation or to cascade to higher-order phase-locked loops.

The length of the up/down K counter is digitally programmable according to the K-counter function table. With A, B, C, and D all low, the K counter is disabled. With A high and B, C, and D low, the K counter is only three stages long, which widens the bandwidth, or capture range, and shortens the lock time of the loop. When A, B, C, and D are programmed high, the K counter becomes 17 stages long, which narrows the bandwidth, or capture range, and lengthens the lock time. Real-time control of loop bandwidth by manipulating the A-through-D inputs can maximize the overall performance of the digital phase-locked loop.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC – M	Tube	CD74ACT297M	ACT297M
		Tape and reel	CD74ACT297M96	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

This device performs the classic first-order phase-locked-loop function without using analog components. The accuracy of the digital phase-locked loop (DPLL) is not affected by V_{CC} and temperature variations, but depends solely on accuracies of the K clock (K CLK), increment/decrement clock (I/D CLK), and loop propagation delays. The I/D clock frequency and the divide-by-N modulos determine the center frequency of the DPLL. The center frequency is defined by the relationship f_c = I/D clock/2N (Hz).

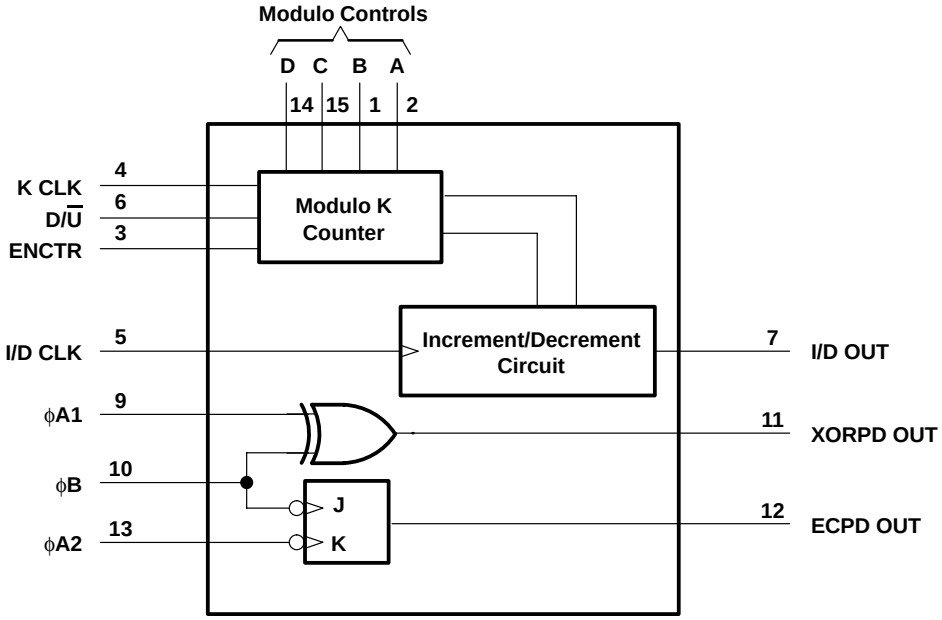


Figure 1. Simplified Block Diagram

Function Tables

K COUNTER
(digital control)

D	C	B	A	MODULO (K)
L	L	L	L	Inhibited
L	L	L	H	2^3
L	L	H	L	2^4
L	L	H	H	2^5
L	H	L	L	2^6
L	H	L	H	2^7
L	H	H	L	2^8
L	H	H	H	2^9
H	L	L	L	2^{10}
H	L	L	H	2^{11}
H	L	H	L	2^{12}
H	L	H	H	21^3
H	H	L	L	2^{14}
H	H	L	H	2^{15}
H	H	H	L	2^{16}
H	H	H	H	2^{17}

EXCLUSIVE-OR PHASE DETECTOR

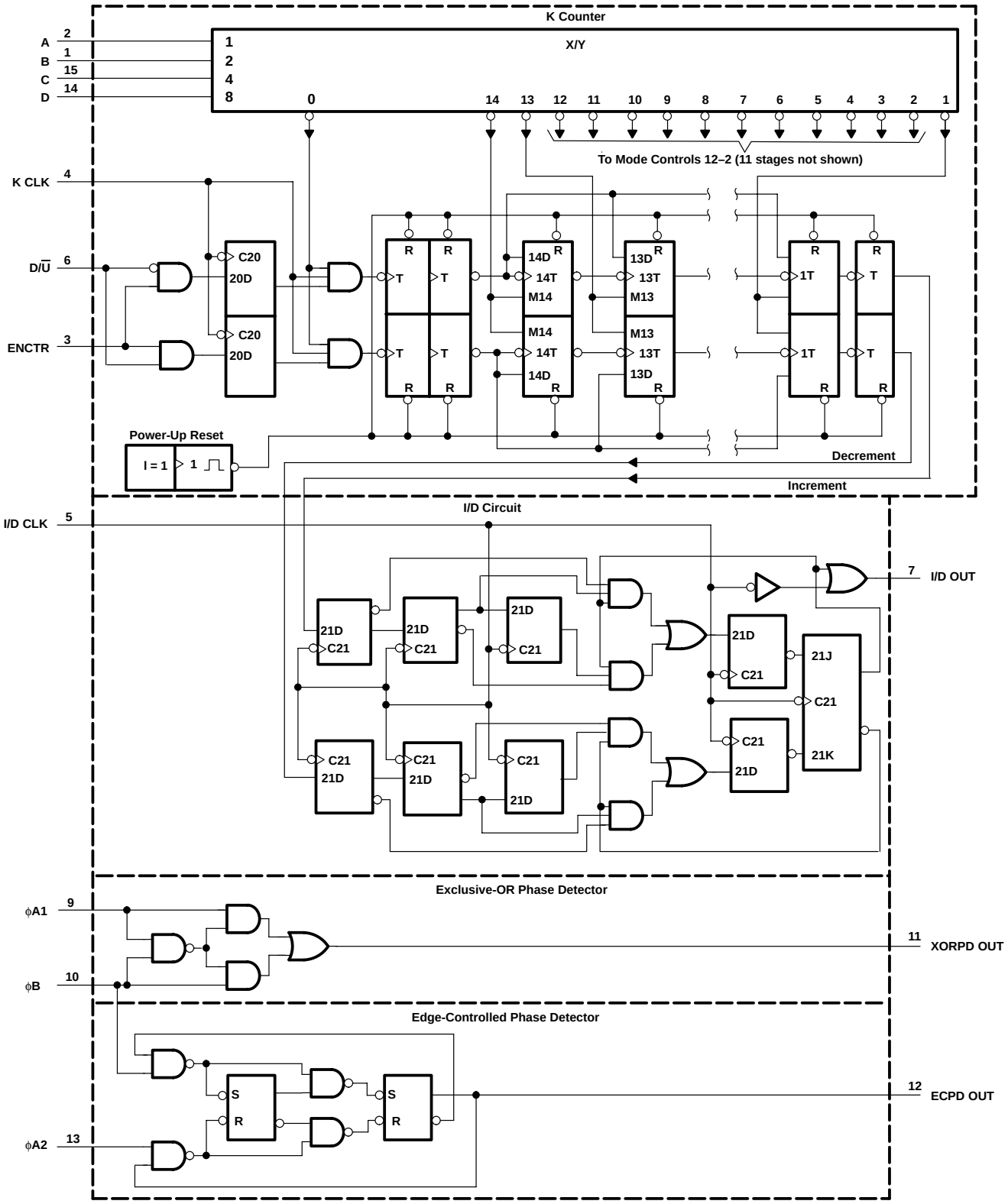
ϕA1	ϕB	XORPD OUT
L	L	L
L	H	H
H	L	H
H	H	L

EDGE-CONTROLLED PHASE DETECTOR

ϕA2	ϕB	ECPD OUT
H or L	↓	H
↓	H or L	L
H or L	↑	No change
↑	H or L	No change

H = steady-state high level
L = steady-state low level
↓ = transition from high to low
↑ = transition from low to high

functional block diagram



detailed description

The phase detector generates an error-signal waveform that, at zero phase error, is a 50% duty-cycle square wave. At the limits of linear operation, the phase-detector output is either high or low all of the time, depending on the direction of the phase error ($\phi_{in} - \phi_{out}$). Within these limits, the phase-detector output varies linearly with the input phase error according to the gain k_d, which is expressed in terms of phase-detector output per cycle of phase error. The phase-detector output can be varied between ±1 according to the relation:

$$\text{Phase-detector output} = \frac{\%\ \text{high} - \%\ \text{low}}{100} \quad (1)$$

The output of the phase detector is $k_d\ \phi_e$, where the phase error $\phi_e = \phi_{in} - \phi_{out}$.

XORPD and ECPD are commonly used digital types. The ECPD is more complex than the XORPD, but can be described generally as a circuit that changes states on one of the transitions of its inputs. For an XORPD, $k_d = 4$, because its output remains high (PD output = 1) for a phase error of one-fourth cycle. Similarly, for the ECPD, $k_d = 2$, because its output remains high for a phase error of one-half cycle. The type of phase detector determines the zero-phase-error point, i.e., the phase separation of the phase-detector inputs for ϕ_e is defined to be zero. For the basic DPLL system of Figure 2, $\phi_e = 0$ when the phase-detector output is a square wave. The XORPD inputs are one-fourth cycle out of phase for zero phase error. For the ECPD, $\phi_e = 0$ when the inputs are one-half cycle out of phase.

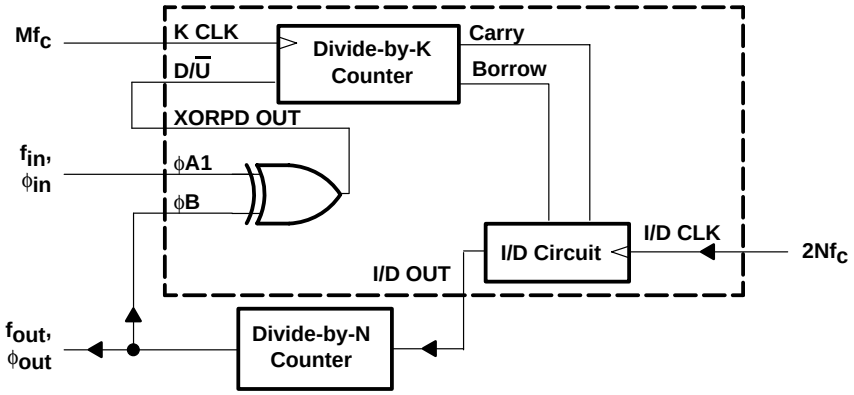


Figure 2. DPLL Using Exclusive-OR Phase Detection

The phase-detector output controls the up/down input to the K counter. The counter is clocked by input frequency Mf_c, which is a multiple M of the loop center frequency f_c. When the K counter recycles up, it generates a carry pulse. Recycling while counting down generates a borrow pulse. If the carry and borrow outputs are conceptually combined into one output that is positive for a carry and negative for a borrow, and if the K counter is considered as a frequency divider with the ratio Mf_c/K, the output of the K counter equals the input frequency multiplied by the division ratio. Thus, the output from the K counter is $k_d\phi_e Mf_c/K$.

The carry and borrow pulses go to the increment/decrement (I/D) circuit, which, in the absence of any carry or borrow pulse, has an output that is one-half of the input clock (I/D CLK). The input clock is just a multiple (2N) of the loop center frequency. In response to a carry or borrow pulse, the I/D circuit either adds or deletes a pulse at I/D OUT. Thus, the output of the I/D circuit is $Nf_c + (k_d\phi_e Mf_c)/2K$.

The output of the N counter (or the output of the phase-locked loop) is:

$$f_o = f_c + (k_d\phi_e Mf_c)/2KN \quad (2)$$

When this result is compared to the equation for a first-order analog phase-locked loop, the digital equivalent of the gain of the VCO is $Mf_c/2KN$, or f_c/K for $M = 2N$.

detailed description (continued)

Thus, the simple first-order phase-locked loop with an adjustable K counter is the equivalent of an analog phase-locked loop with a programmable VCO gain.

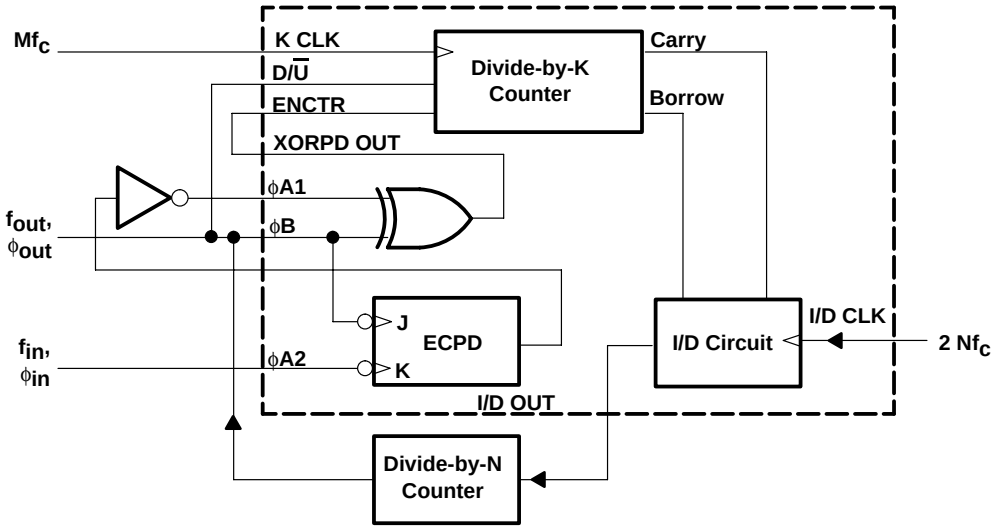


Figure 3. DPLL Using Both Phase Detectors in a Ripple-Cancellation Scheme

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 6 V
DC input diode current, I_{IK} (V_I < –0.5 V or V_I > V_{CC} + 0.5 V) . . . . . ±20 mA
DC input diode current, I_{OK} (V_O < –0.5 V or V_O > V_{CC} + 0.5 V) . . . . . ±50 mA
DC output source or sink current per output pin, I_O (V_O > –0.5 V or V_O < V_{CC} + 0.5 V) . . . . . ±50 mA
Continuous current through V_{CC} or GND (see Note 1) . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 2) . . . . . 73°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. For up to four outputs per device, add ±25 mA for each additional output.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
$\Delta t/\Delta v$	Input rise and fall slew rate		10	ns
T_A	Operating free-air temperature range	–55	125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C		MIN	MAX	UNIT
				MIN	MAX			
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_O = –50 μA	4.5 V	4.4		4.4		V
		I_O = –24 mA	4.5 V	3.4		3.1		
		I_O = –75 mA	5.5 V			3.3		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_O = 50 μA	4.5 V		0.1		0.1	V
		I_O = 24 mA	4.5 V		0.9		1.1	
		I_O = 75 mA†	5.5 V				2.9	
I_I	$V_I = V_{CC}$ or GND		5.5 V		±0.1		±1	μA
I_{CC} (MSI)	$V_I = V_{CC}$ or GND		5.5 V		8		80	μA
I_{CC} (SSI/FF)	$V_I = V_{CC}$ or GND		5.5 V		4		40	μA
ΔI_{CC}	$V_I = V_{CC}$ –2.1 V		4.5 V to 5.5 V		2.4		2.8	mA

† Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C.

ACT INPUT LOAD

INPUT	UNIT LOAD†
ENCTR, D/$\overline{U}$	0.1
A, B, C, D, K CLK, ϕA2	0.2
I/D CLK, ϕA1, ϕB	0.5

† Unit Load is ΔI_{CC} limit specified in electrical characteristics table (e.g., 2.4 mA at 25°C).

timing requirements over recommended supply-voltage range and recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency	K CLK		55		45	MHz
		I/D CLK		40		35	
t_w	Pulse duration	K CLK	6		8		ns
		I/D CLK	7		9		
t_{su}	Setup time before K CLK↑	D/$\overline{U}$	13		17		ns
		ENCTR	12		16		
t_h	Hold time after K CLK↑	D/$\overline{U}$	3		7		ns
		ENCTR	2		6		

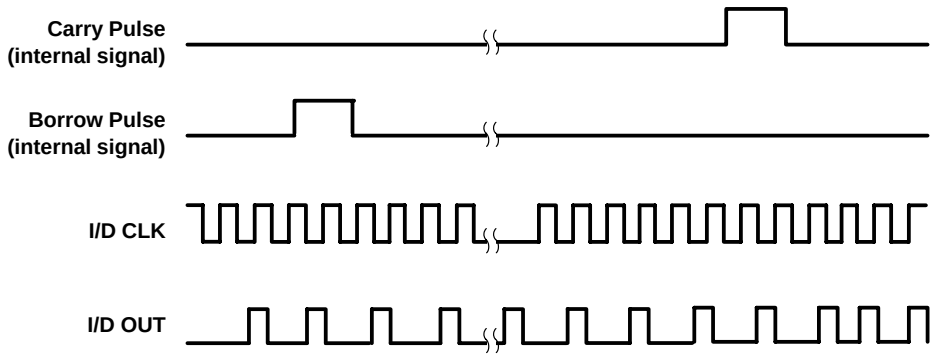


Figure 4. I/D OUT in Lock Condition

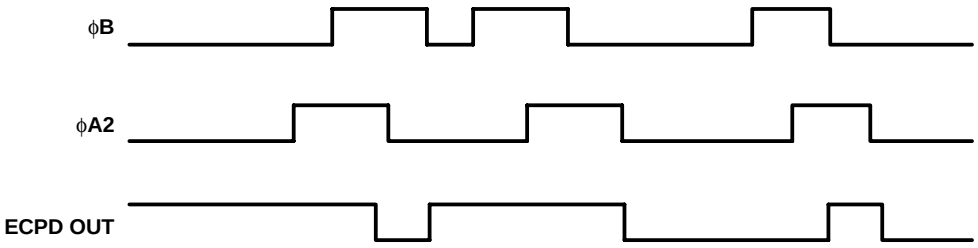


Figure 5. Edge-Controlled Phase-Comparator Waveforms

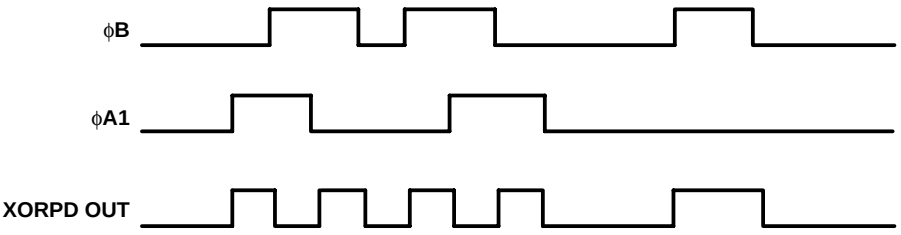


Figure 6. Exclusive-OR Phase-Detector Waveforms

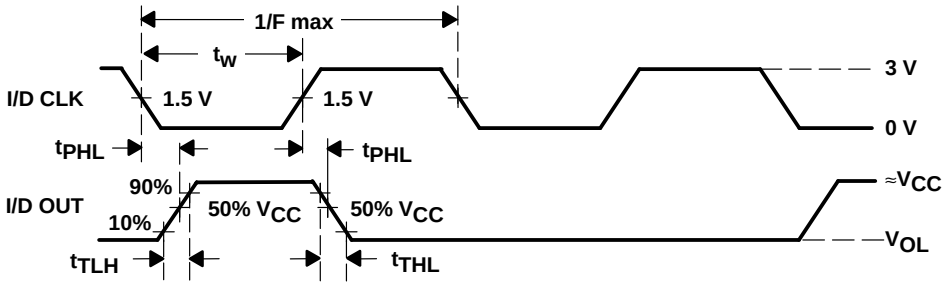


Figure 7. Clock (ID CLK) to Output (ID OUT) Propagation Delays, Clock Pulse Duration, and Maximum Clock-Pulse Frequency

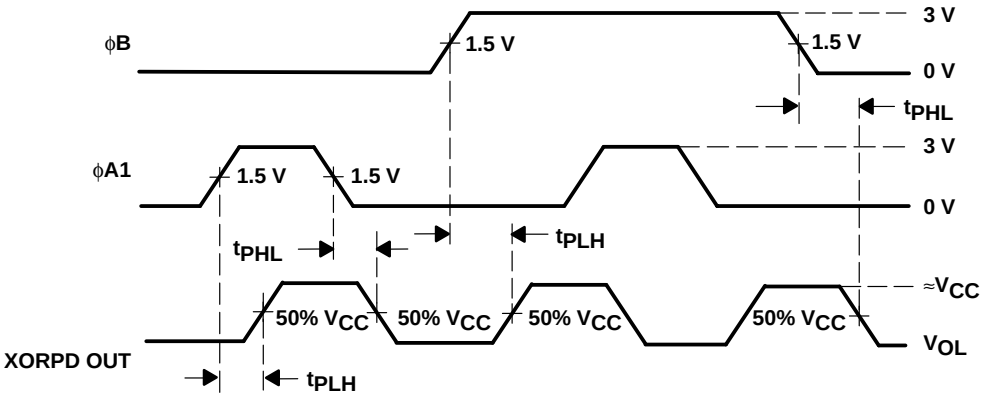


Figure 8. Phase Input (φB, φA2) to Output (XORPD OUT) Propagation Delays

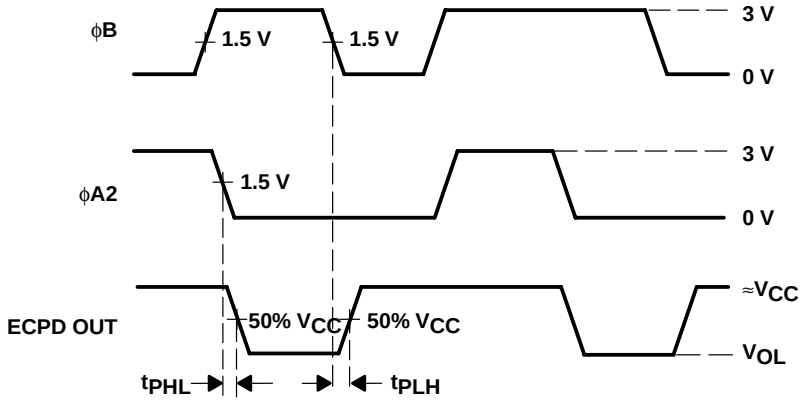
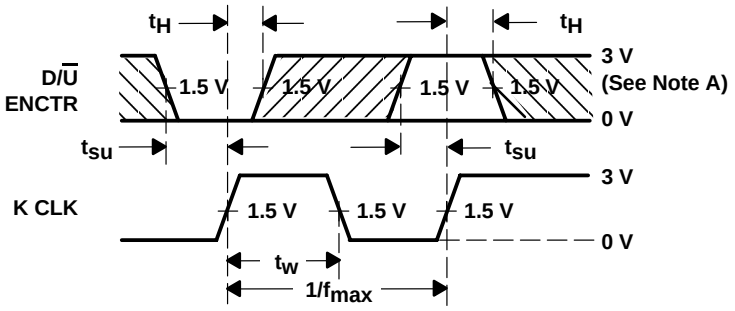


Figure 9. Phase Input (φB, φA2) to Output (ECPD OUT) Propagation Delays



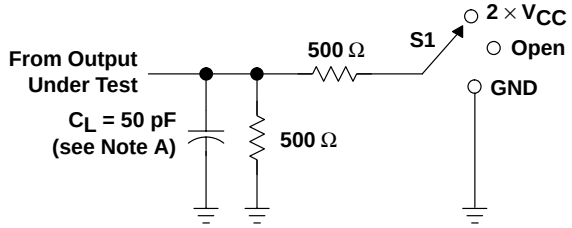
NOTE A: Shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 10. Clock (K CLK) Pulse Duration and Maximum Clock-Pulse Frequency, and Inputs (D/$\overline{U}$, ENCTR) to Clock (K CLK) Setup and Hold Times

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted)

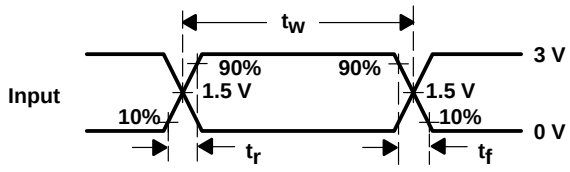
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}	K CLK	I/D OUT	55			45		MHz
	I/D CLK		40			35		
t_{PLH}	I/D CLK	I/D OUT			19		24	ns
t_{PHL}					19		24	
t_{PHL}	ϕA2	ECPD OUT			24		30	ns
t_{PLH}	ϕA1	XORPD OUT			17		22	ns
t_{PHL}					17		22	
t_{PLH}	ϕB	XORPD OUT			17		22	ns
t_{PHL}					17		22	
t_{PLH}	ϕB	ECPD OUT			24		30	ns

PARAMETER MEASUREMENT INFORMATION

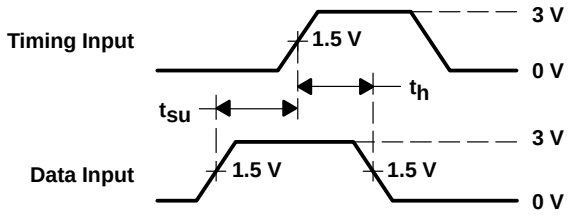


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

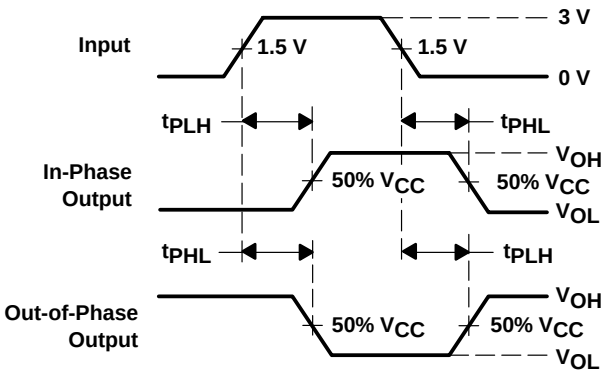
LOAD CIRCUIT



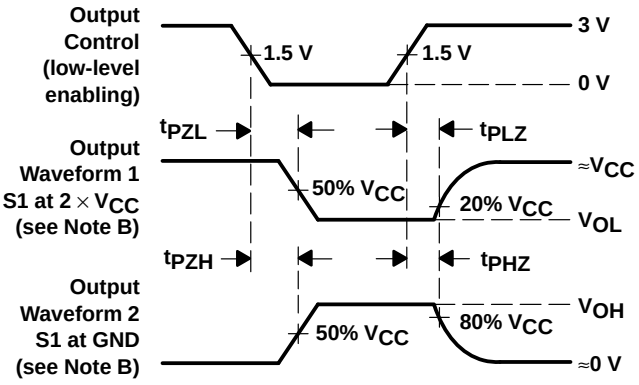
VOLTAGE WAVEFORMS
INPUT RISE AND FALL TIMES AND PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 11. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74ACT297M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT297M	Samples
CD74ACT297M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT297M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

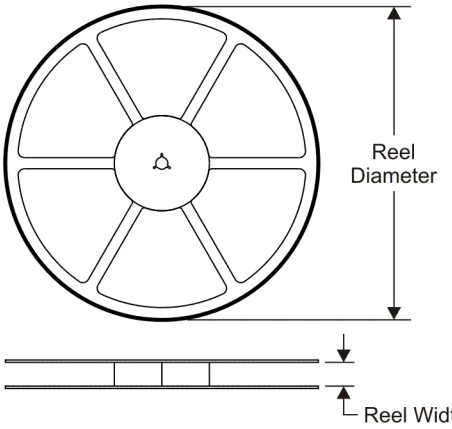
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

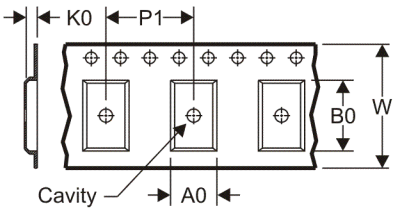
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

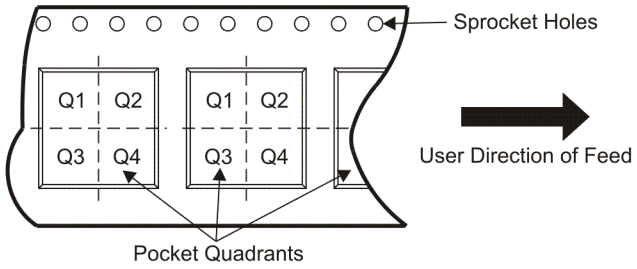


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

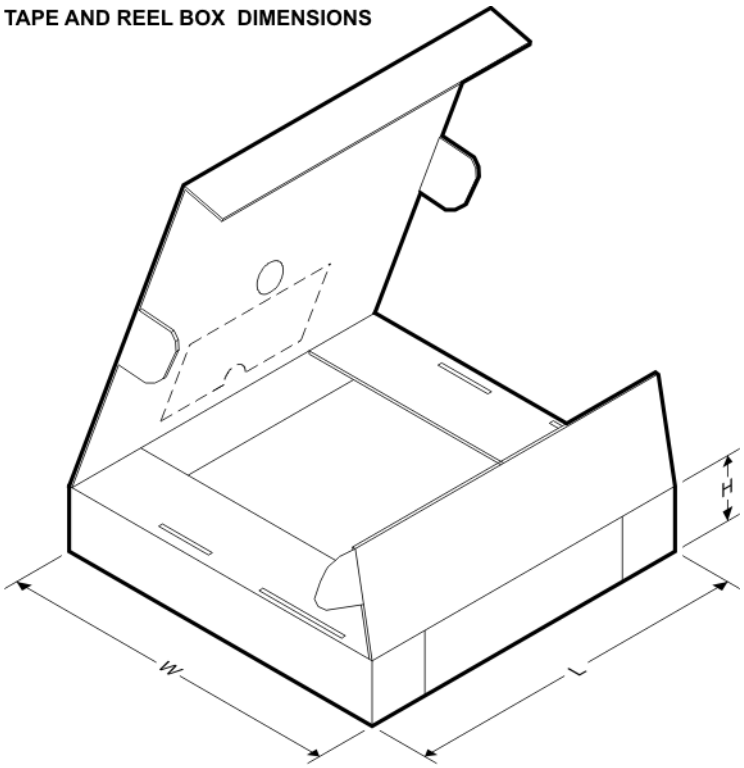
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74ACT297M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

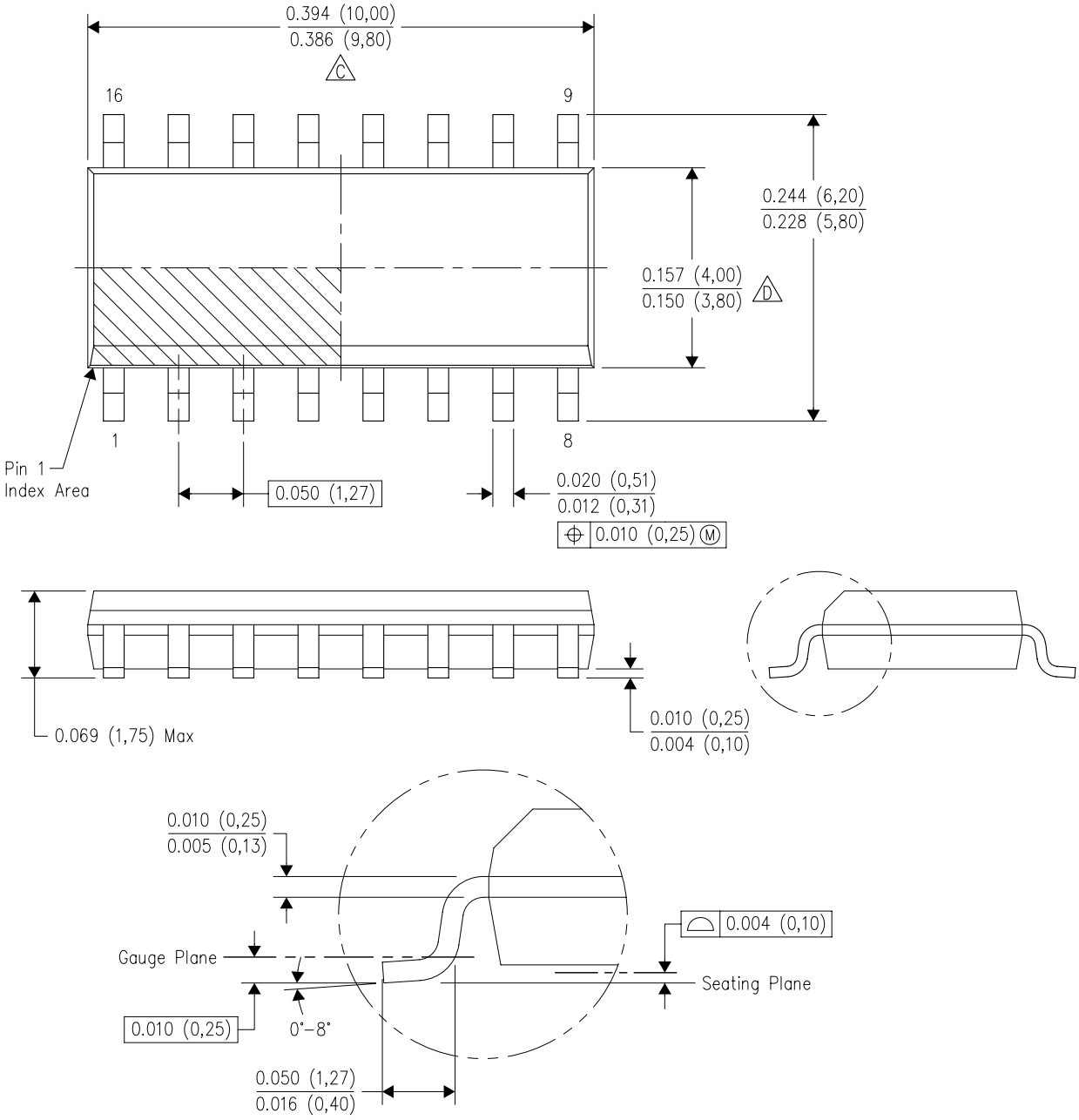
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

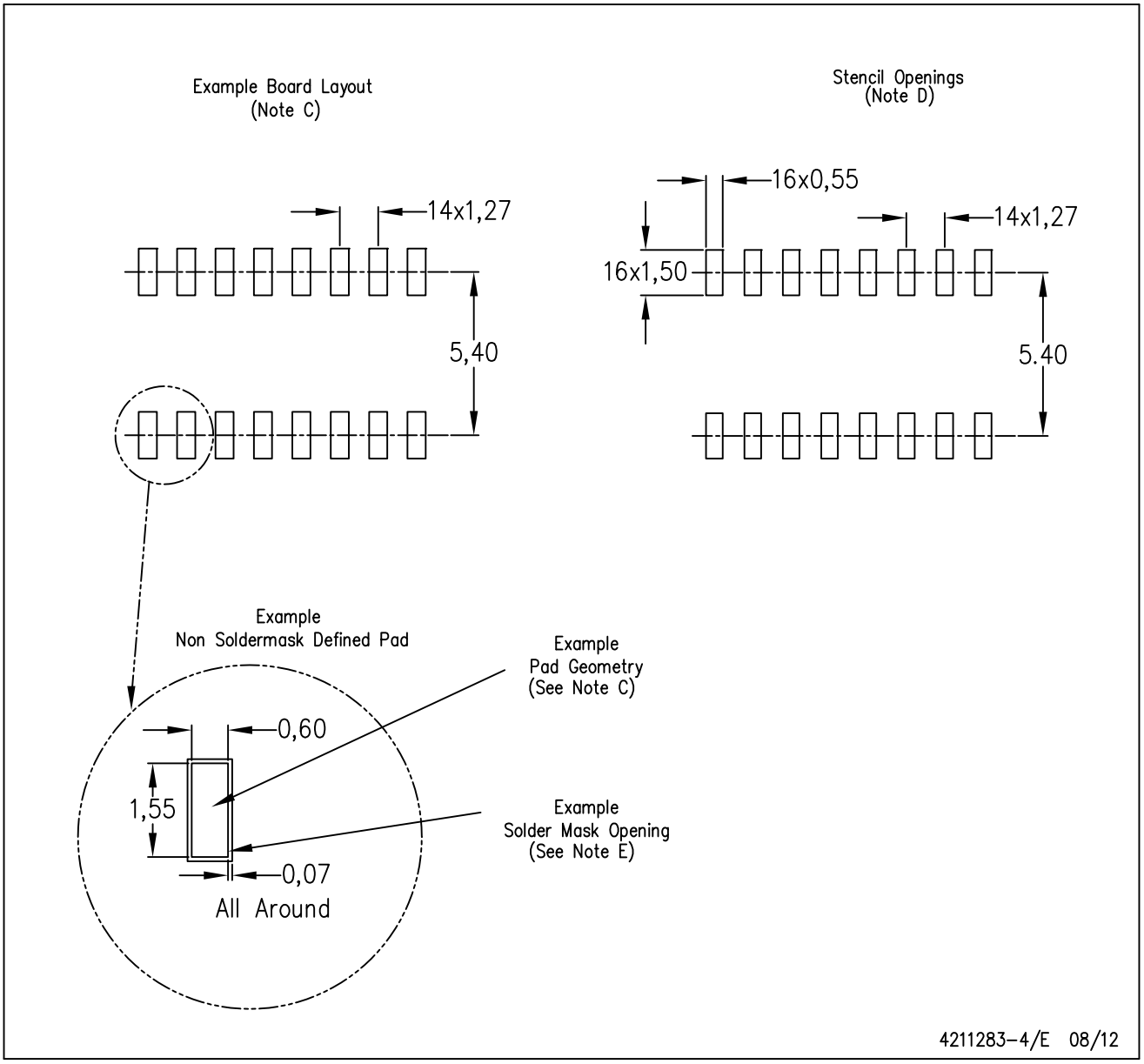
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74ACT297M96	SOIC	D	16	2500	333.2	345.9	28.6

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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