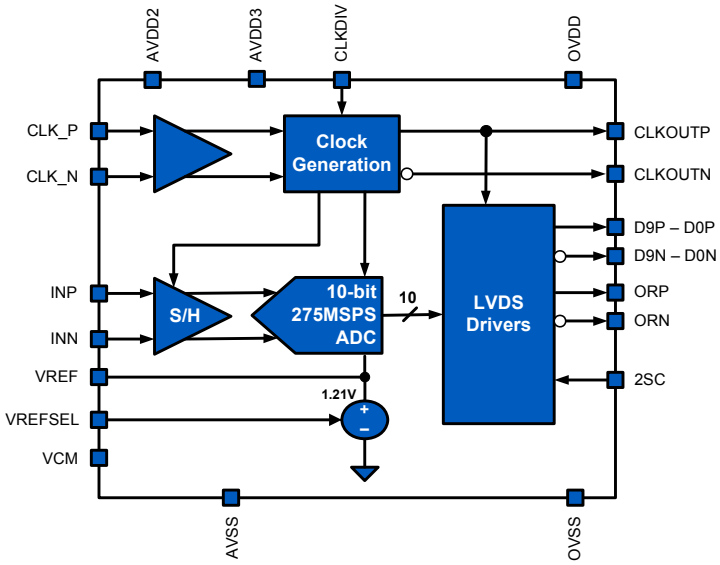
KAD2710L

10-Bit, 275/210/170/105MSPS A/D Converter

FN6818
Rev 0.00
December 5, 2008

The KAD2710L is the industry's lowest power, 10-bit, 275MSPS, high performance Analog-to-Digital converter. It is designed with Intersil's proprietary FemtoCharge™ technology on a standard CMOS process. The KAD2710L offers high dynamic performance (55.6dBFS SNR @ f_{IN} = 138MHz) while consuming less than 280mW. Features include an over-range indicator and a selectable divide-by-2 input clock divider. The KAD2710L is one member of a pin-compatible family offering 8 and 10-bit ADCs with sample rates from 105MSPS to 350MSPS and LVDS-compatible or LVCMOS outputs (Table 1). This family of products is available in 68-pin RoHS-compliant QFN packages with exposed paddle. Performance is specified over the full industrial temperature range (-40°c to +85°C).



Features

- On-Chip Reference
- Internal Sample and Hold
- 1.5V_{P-P} Differential Input Voltage
- 600MHz Analog Input Bandwidth
- Two's Complement or Binary Output
- Over-Range Indicator
- Selectable ÷2 Clock Input
- LVDS Compatible Outputs

Applications

- High-Performance Data Acquisition
- Portable Oscilloscope
- Medical Imaging
- Cable Head Ends
- Power-Amplifier Linearization
- Radar and Satellite Antenna Array Processing
- Broadband Communications
- Point-to-Point Microwave Systems
- Communications Test Equipment
- Pb-Free (RoHS Compliant)

Key Specs

- SNR = 55.6dBFS at f_S = 275MSPS, f_{IN} = 138MHz
- SFDR = 68.5dBc at f_S = 275MSPS, f_{IN} = 138MHz
- Power Consumption <280mW at f_S = 275MSPS

Pin-Compatible Family

TABLE 1. PIN-COMPATIBLE PRODUCTS

RESOLUTION, SPEED	LVDS OUTPUTS	LVCMOS OUTPUTS
8 Bits 350MSPS	KAD2708L-35	
8 Bits 275MSPS	KAD2708L-27	KAD2708C-27
8 Bits 210MSPS	KAD2708L-21	KAD2708C-21
8 Bits 170MSPS	KAD2708L-17	KAD2708C-17
8 Bits 105MSPS	KAD2708L-10	KAD2708C-10
10 Bits 275MSPS	KAD2710L-27	KAD2710C-27
10 Bits 210MSPS	KAD2710L-21	KAD2710C-21
10 Bits 170MSPS	KAD2710L-17	KAD2710C-17
10 Bits 105MSPS	KAD2710L-10	KAD2710C-10

Ordering Information

PART NUMBER (Note)	SPEED (MSPS)	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
KAD2710L-27Q68	275	-40 to +85	68 Ld QFN	L68.10x10B
KAD2710L-21Q68	210	-40 to +85	68 Ld QFN	L68.10x10B
KAD2710L-17Q68	170	-40 to +85	68 Ld QFN	L68.10x10B
KAD2710L-10Q68	105	-40 to +85	68 Ld QFN	L68.10x10B

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

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Absolute Maximum Ratings

AVDD2 to AVSS . . . . . -0.4V to 2.1V
AVDD3 to AVSS . . . . . -0.4V to 3.7V
OVDD2 to OVSS . . . . . -0.4V to 2.1V
Analog Inputs to AVSS . . . . . -0.4V to AVDD3 + 0.3V
Clock Inputs to AVSS . . . . . -0.4V to AVDD2 + 0.3V
Logic Inputs to AVSS (VREFSEL, CLKDIV) -0.4V to AVDD3 + 0.3V
Logic Inputs to OVSS (RST, 2SC) . . . . . -0.4V to OVDD2 + 0.3V
VREF to AVSS . . . . . -0.4V to AVDD3 + 0.3V
Analog Output Currents 10mA
Logic Output Currents 10mA
LVDS Output Currents 20mA

Thermal Information

Operating Temperature . . . . . -40°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . +150°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Electrical Specifications All specifications apply under the following conditions unless otherwise noted: AVDD2 = 1.8V, AVDD3 = 3.3V, OVDD = 1.8V, T_A = -40°C to +85°C (typical specifications at +25°C), f_{SAMPLE} = 275MSPS, 210MSPS, 170MSPS and 105MSPS, f_{IN} = Nyquist at -0.5dBFS.

PARAMETER	SYMBOL	CONDITIONS	KAD2710L-27			KAD2710L-21			KAD2710L-17			KAD2710L-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC SPECIFICATIONS															
Analog Input															
Full-Scale Analog Input Range	V_{FS}		1.4	1.5	1.6	1.4	1.5	1.6	1.4	1.5	1.6	1.4	1.5	1.6	V_{P-P}
Full Scale Range Temp. Drift	A_{VTC}	Full Temp		230			210			198			178		ppm/°C
Common-Mode Output Voltage	V_{CM}			860			860			860			860		mV
Power Requirements															
1.8V Analog Supply Voltage	AVDD2		1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
3.3V Analog Supply Voltage	AVDD3		3.15	3.3	3.45	3.15	3.3	3.45	3.15	3.3	3.45	3.15	3.3	3.45	V
1.8V Digital Supply Voltage	OVDD		1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
1.8V Analog Supply Current	I_{AVDD2}			44	51		38	42		35	39		29	33	mA
3.3V Analog Supply Current	I_{AVDD3}			41	45		33	37		28	32		21	24	mA
1.8V Digital Supply Current	I_{OVDD}			36	41		35	39		34	38		31	35	mA
Power Dissipation	P_D			278	314		240	268		217	244		178	202	mW
AC SPECIFICATIONS															
Maximum Conversion Rate	f_S MAX		275			210			170			105			MSPS
Minimum Conversion Rate	f_S MIN				50			50			50			50	MSPS
Differential Nonlinearity	DNL		-1.0	±0.8	1.5	-1.0	±0.8	1.5	-1.0	±0.8	1.5	-1.0	±0.8	1.5	LSB
Integral Nonlinearity	INL		-2.5	±1.0	2.0	-2.5	±1.0	1.5	-2.5	±1.0	1.5	-2.5	±1.0	1.5	LSB
Signal-to-Noise Ratio	SNR	f_{IN} = 10MHz		55.7			56.4			56.6			56.6		dBFS
		f_{IN} = Nyquist	53.5	55.6		53.5	56.2		53.5	56.5		53.5	56.5		dBFS
		f_{IN} = 430MHz		55.2			54.8			54.6			54.5		dBFS
Signal-to-Noise and Distortion	SINAD	f_{IN} = 10MHz		55.3			56.1			56.3			56.3		dBFS
		f_{IN} = Nyquist	52.5	55.2		52.5	56.0		52.5	56.2		52.5	56.2		dBFS
		f_{IN} = 430MHz		54.4			53.7			53.4			53.2		dBFS

Electrical Specifications All specifications apply under the following conditions unless otherwise noted: AVDD2 = 1.8V, AVDD3 = 3.3V, OVDD = 1.8V, T_A = -40°C to +85°C (typical specifications at +25°C), f_{SAMPLE} = 275MSPS, 210MSPS, 170MSPS and 105MSPS, f_{IN} = Nyquist at -0.5dBFS. **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	KAD2710L-27			KAD2710L-21			KAD2710L-17			KAD2710L-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Effective Number of Bits	ENOB	f_{IN} = 10MHz		8.9			9.0			9.1			9.1		Bits
		f_{IN} = Nyquist	8.4	8.9		8.4	9.0		8.4	9.0		8.4	9.0		Bits
		f_{IN} = 430MHz		8.7			8.6			8.6			8.5		Bits
Spurious-Free Dynamic Range	SFDR	f_{IN} = 10MHz		68.5			70			71			71		dBc
		f_{IN} = Nyquist	62	68.5		62	71.1		62	71		62	72		dBc
		f_{IN} = 430MHz		63.8			62.6			60.1			60.9		dBc
Two-Tone SFDR	2TSFDR	f_{IN} = 133MHz, 135MHz		68			70			70			71		dBc
Word Error Rate	WER			10^{-12}			10^{-12}			10^{-12}			10^{-12}		
Full Power Bandwidth	FPBW			600			600			600			600		MHz

Digital Specifications

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUTS						
Input Voltage High (VREFSEL)	V_{IH}		0.8*AVDD3			V
Input Voltage Low (VREFSEL)	V_{IL}				0.2*AVDD3	V
Input Current High (VREFSEL)	I_{IH}	V_{IN} = AVDD3		0	10	µA
Input Current Low (VREFSEL)	I_{IL}	V_{IN} = AVSS	-90	-65	-30	µA
Input Voltage High (CLKDIV)	V_{IH}		0.8*AVDD3			V
Input Voltage Low (CLKDIV)	V_{IL}				0.2*AVDD3	V
Input Current High (CLKDIV)	I_{IH}	V_{IN} = AVDD3	100	65	10	µA
Input Current Low (CLKDIV)	I_{IL}	V_{IN} = AVSS		0	-10	µA
Input Voltage High (RST,2SC)	V_{IH}		0.8*OVDD2			V
Input Voltage Low (RST,2SC)	V_{IL}				0.2*OVDD2	V
Input Current High (RST,2SC)	I_{IH}	VIN = OVDD		0	10	µA
Input Current Low (RST,2SC)	I_{IL}	VIN = OVSS	-50	-30	-5	µA
Input Capacitance	C_{DI}			3		pF
CLKP, CLKN P-P Differential Input Voltage	V_{CDI}		0.5		3.6	V_{P-P}
CLKP, CLKN Differential Input Resistance	R_{CDI}			10		MΩ
CLKP, CLKN Common-Mode Input Voltage	V_{CCI}			0.9		V
LVCMOS OUTPUTS						
Differential Output Voltage	V_T			210		mV
Output Offset Voltage	V_{OS}			1.15		V
Output Rise Time	t_R			500		ps
Output Fall Time	t_F			500		ps

Timing Diagram

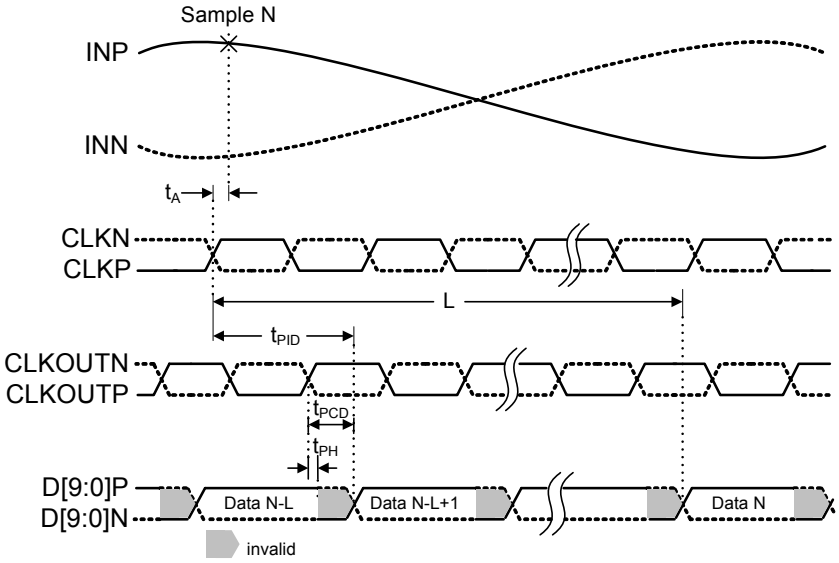


FIGURE 1. LVDS TIMING DIAGRAM

Timing Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Aperture Delay	t_A		1.7		ns
RMS Aperture Jitter	j_A		200		fs
Input Clock to Data Propagation Delay	t_{PID}	3.5	5.0	6.5	ns
Data Hold Time	t_{PH}	-300			ps
Output Clock to Data Propagation Delay	t_{PCD}		2.8	3.7	ns
Latency (Pipeline Delay)	L		28		cycles
Overvoltage Recovery	t_{OVR}		1		cycle

Thermal Impedance

PARAMETER	SYMBOL	TYP	UNIT
Junction to Paddle (Note 1)	θ_{JP}	30	°C/W

NOTE:

1. Paddle soldered to ground plane.

ESD

Electrostatic charge accumulates on humans, tools and equipment and may discharge through any metallic package contacts (pins, balls, exposed paddle, etc.) of an integrated circuit. Industry-standard protection techniques have been utilized in the design of this product. However, reasonable care must be taken in the storage and handling of ESD sensitive products. Contact Intersil for the specific ESD sensitivity rating of this product.

Pin Descriptions

PIN NUMBER	NAME	FUNCTION
1, 14, 18, 20	AVDD2	1.8V Analog Supply
2, 7, 10, 19, 21, 24	AVSS	Analog Supply Return
3	VREF	Reference Voltage Out/In
4	VREFSEL	Reference Voltage Select (0:Int 1:Ext)
5	VCM	Common-Mode Voltage Output
6, 15, 16, 25	AVDD3	3.3V Analog Supply
8, 9	INP, INN	Analog Input Positive, Negative
11-13, 29-32, 62, 63, 67	DNC	Do Not Connect
17	CLKDIV	Clock Divide by Two (Active Low)
22, 23	CLKN, CLKP	Clock Input Complement, True
26, 45, 61	OVSS	Output Supply Return
27, 41, 44, 60	OVDD2	1.8V LVDS Supply
28	RST	Power On Reset (Active Low)
33, 34	D0N, D0P	LVDS Bit 0 (LSB) Output Complement, True
35, 36	D1N, D1P	LVDS Bit 1 Output Complement, True
37, 38	D2N, D2P	LVDS Bit 2 Output Complement, True
39, 40	D3N, D3P	LVDS Bit 3 Output Complement, True
42, 43	CLKOUTN, CLKOUTP	LVDS Clock Output Complement, True
46, 47	D4N, D4P	LVDS Bit 4 Output Complement, True
48, 49	D5N, D5P	LVDS Bit 5 Output Complement, True
50, 51	D6N, D6P	LVDS Bit 6 Output Complement, True
52, 53	D7N, D7P	LVDS Bit 7 Output Complement, True
54, 55	D8N, D8P	LVDS Bit 8 Output Complement, True
56, 57	D9N, D9P	LVDS Bit 9 (MSB) Output Complement, True
58, 59	ORN, ORP	Over-Range Complement, True
64-66		Connect to OVDD2
68	2SC	Two’s Complement Select (Active Low)
Exposed Paddle	AVSS	Analog Supply Return

Pinout

KAD2710C
(68 LD QFN)
TOP VIEW

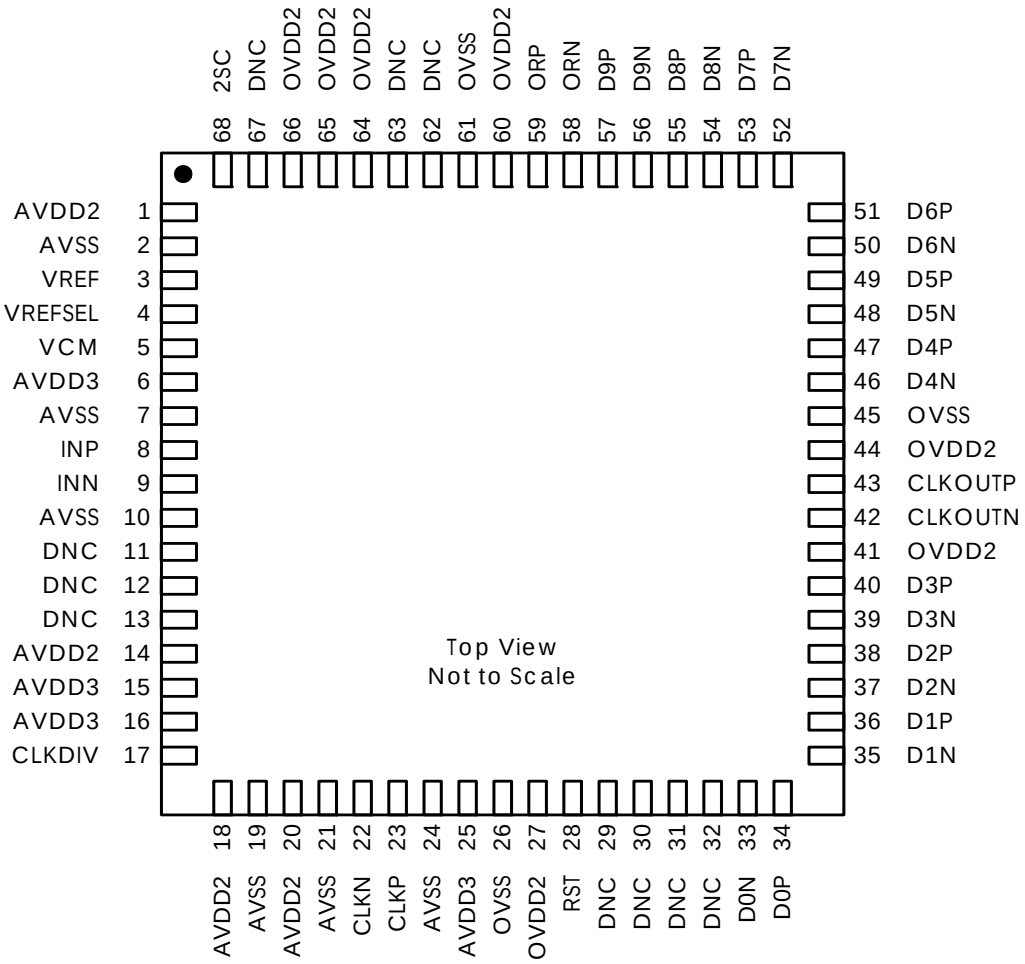


FIGURE 2. PIN CONFIGURATION

Typical Performance Curves

AVDD2 = OVDD2 = 1.8V, AVDD3 = 3.3V, T_A = +25°C, f_{SAMPLE} = 275MSPS, f_{IN} = 137MHz, A_{IN} = -0.5dBFS unless noted.

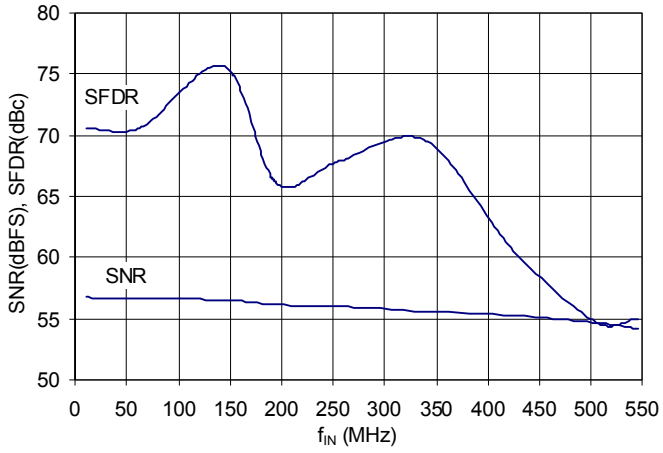


FIGURE 3. SNR AND SFDR vs f_{IN}

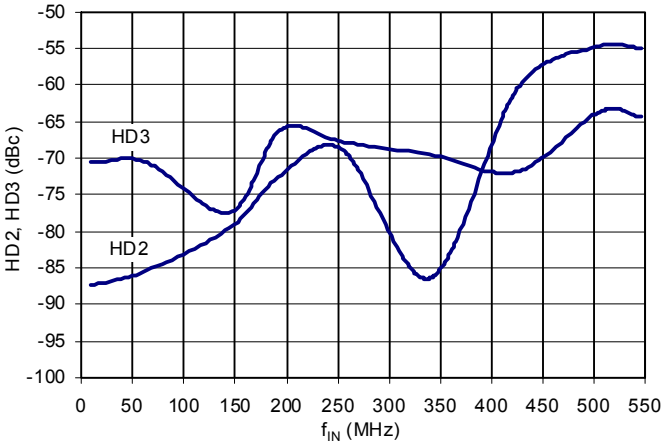


FIGURE 4. HD2 AND HD3 vs f_{IN}

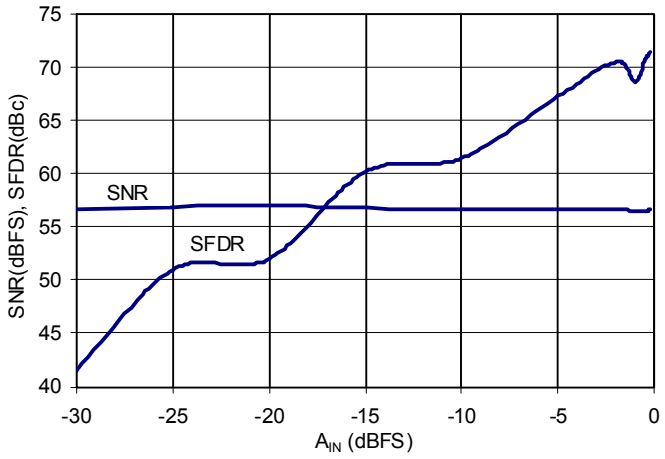


FIGURE 5. SNR AND SFDR vs A_{IN}

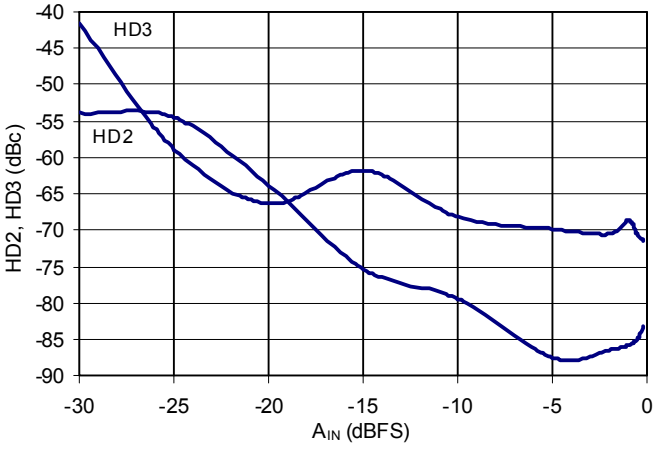


FIGURE 6. HD2 AND HD3 vs A_{IN}

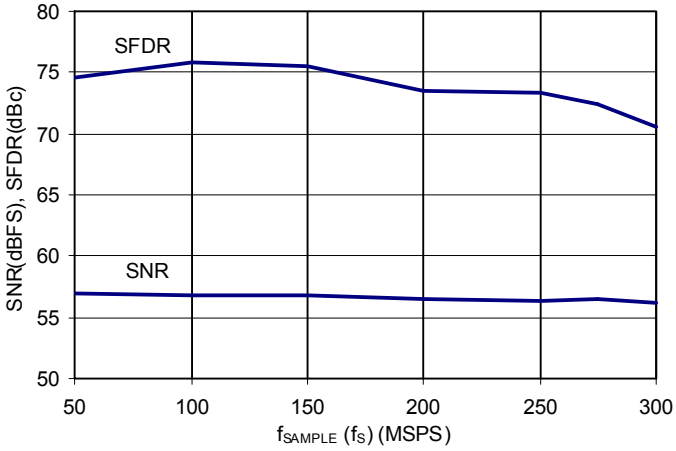


FIGURE 7. SNR AND SFDR vs f_{SAMPLE}

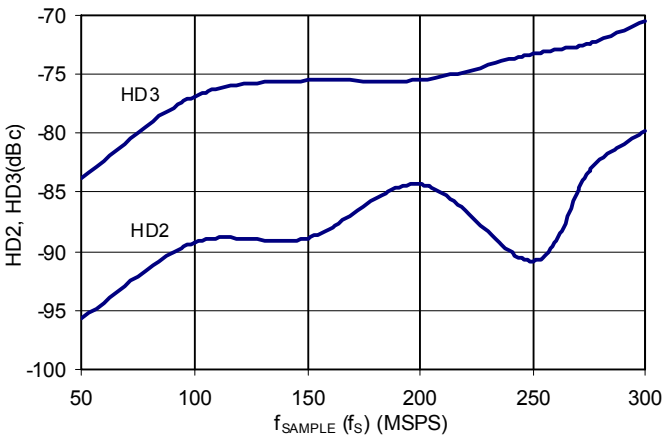


FIGURE 8. HD2 AND HD3 vs f_{SAMPLE}

Typical Performance Curves

AVDD2 = OVDD2 = 1.8V, AVDD3 = 3.3V, T_A = +25°C, f_{SAMPLE} = 275MSPS, f_{IN} = 137MHz, A_{IN} = -0.5dBFS unless noted. **(Continued)**

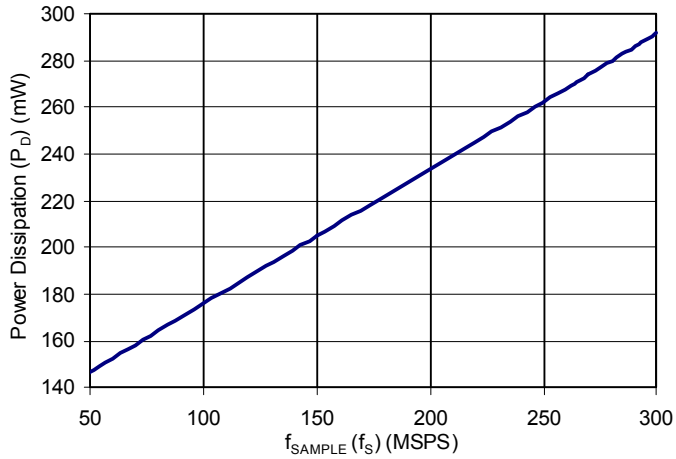


FIGURE 9. POWER DISSIPATION vs f_{SAMPLE}

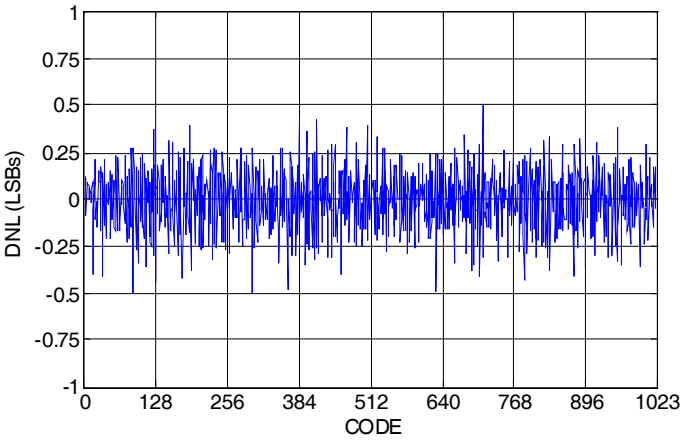


FIGURE 10. DIFFERENTIAL NONLINEARITY vs OUTPUT CODE

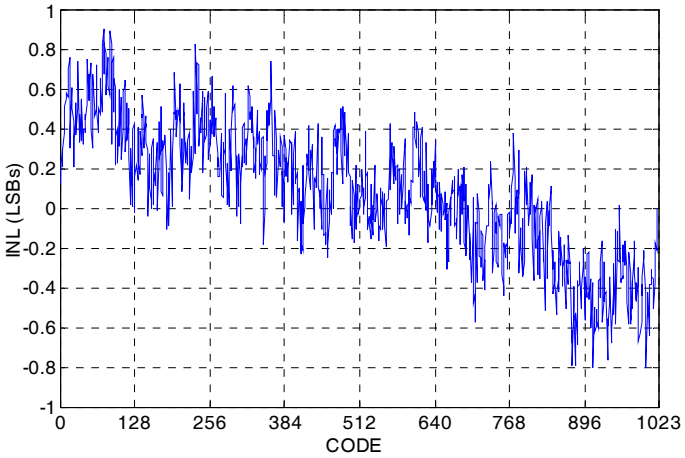


FIGURE 11. INTEGRAL NONLINEARITY vs OUTPUT CODE

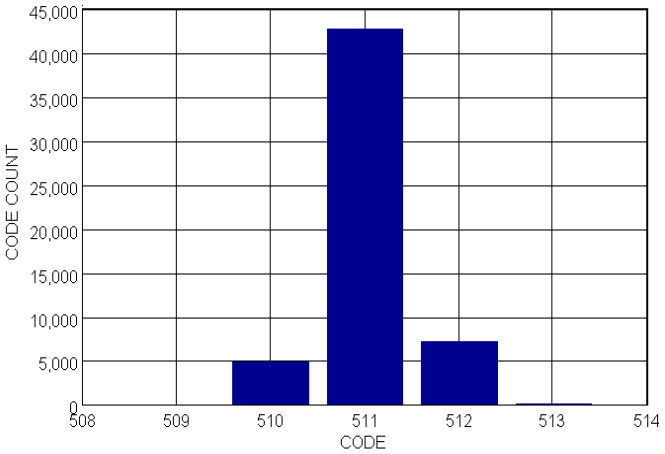


FIGURE 12. NOISE HISTOGRAM

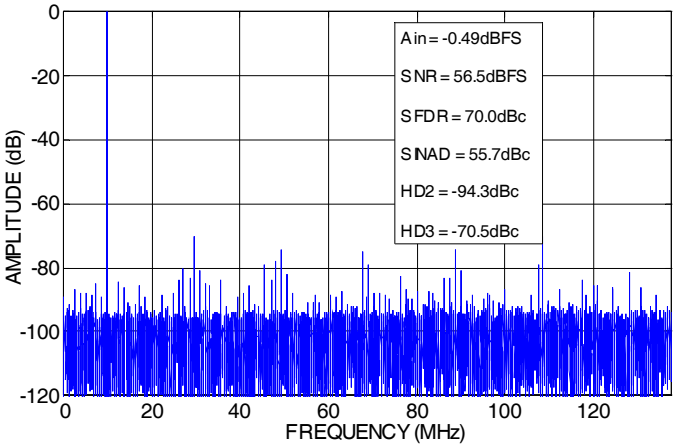


FIGURE 13. OUTPUT SPECTRUM; f_{IN} = 10MHz

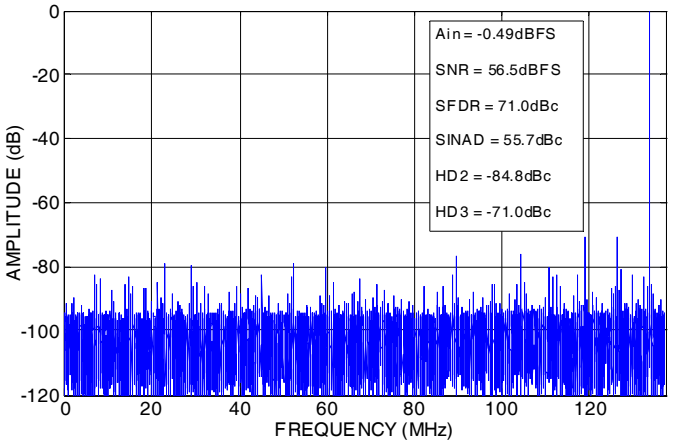


FIGURE 14. OUTPUT SPECTRUM; f_{IN} = 134MHz

Typical Performance Curves

AVDD2 = OVDD2 = 1.8V, AVDD3 = 3.3V, T_A = +25°C, f_{SAMPLE} = 275MSPS, f_{IN} = 137MHz, A_{IN} = -0.5dBFS unless noted. **(Continued)**

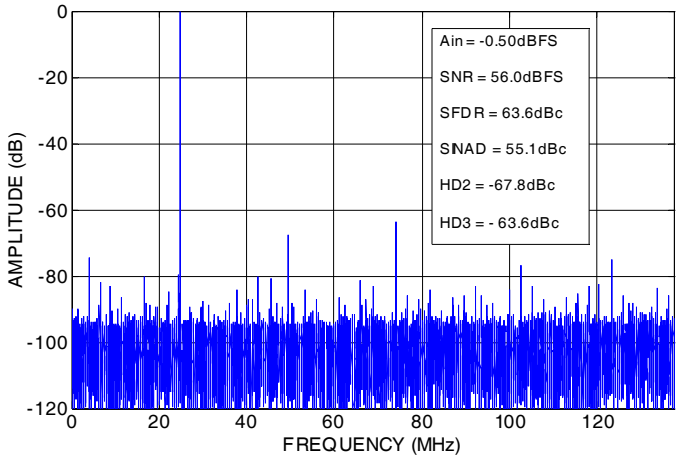


FIGURE 15. OUTPUT SPECTRUM; f_{IN} = 300MHz

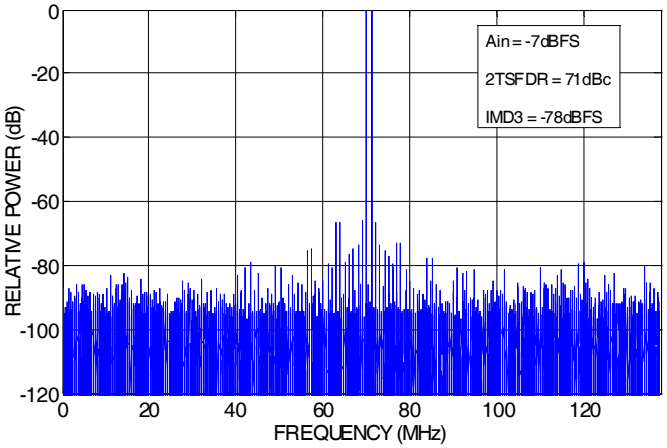


FIGURE 16. TWO-TONE SPECTRUM; f_{IN} = 69MHz, 70MHz

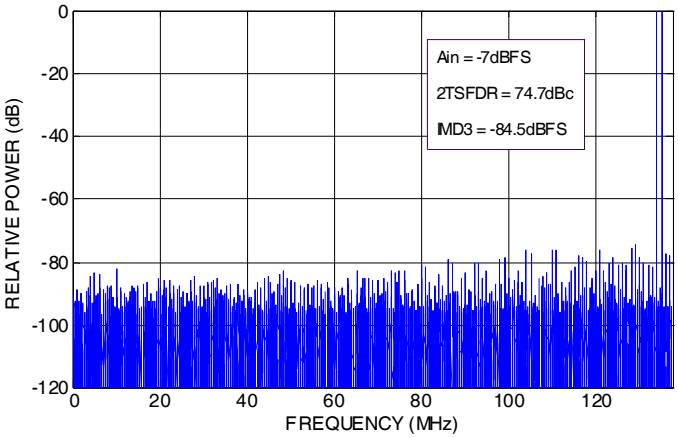


FIGURE 17. TWO-TONE SPECTRUM; f_{IN} = 140MHz, 141MHz

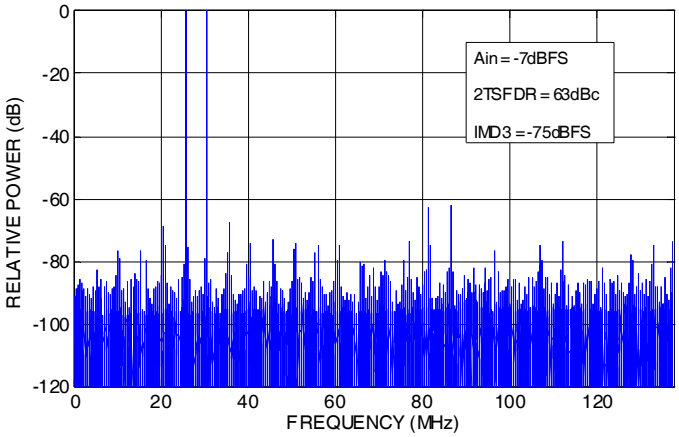


FIGURE 18. TWO-TONE SPECTRUM; f_{IN} = 300MHz, 305MHz

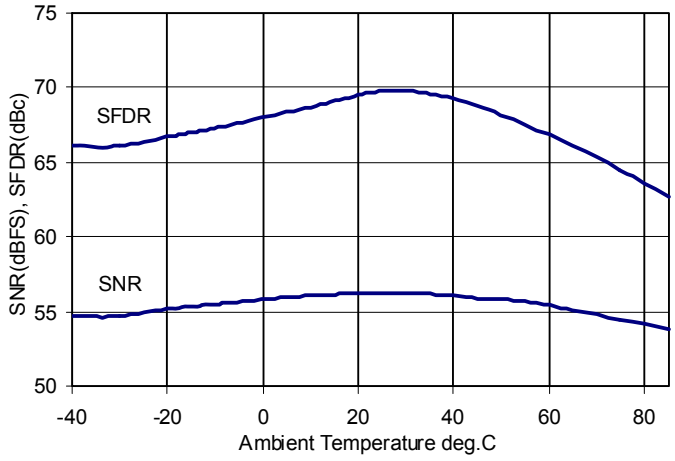


FIGURE 19. SNR vs TEMPERATURE

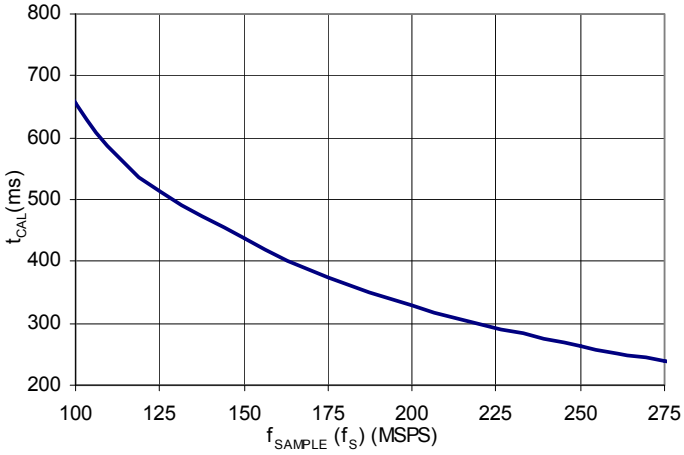


FIGURE 20. CALIBRATION TIME vs f_S

Functional Description

The KAD2710 is a ten bit, 275MSPS A/D converter in a pipelined architecture. The input voltage is captured by a sample and hold circuit and converted to a unit of charge. Proprietary charge-domain techniques are used to compare the input to a series of reference charges. These comparisons determine the digital code for each input value. The converter pipeline requires 24 sample clocks to produce a result. Digital error correction is also applied, resulting in a total latency of 28 clock cycles. This is evident to the user as a latency between the start of a conversion and the data being available on the digital outputs.

At power-up, a self-calibration is performed to minimize gain and offset errors. The reset pin (RST) is held low internally at power-up and will remain in that state until the calibration is complete. The clock frequency should remain fixed during this time.

Calibration accuracy is maintained for the sample rate at which it is performed, and therefore should be repeated if the clock frequency is changed by more than 10%. Recalibration can be initiated via the RST pin, or power cycling, at any time.

Reset

Recalibration of the ADC can be initiated at any time by driving the RST pin low for a minimum of one clock cycle. An open-drain driver is recommended.

The calibration sequence is initiated on the rising edge of RST, as shown in Figure 21. The over-range output (ORP) is set high once RST is pulled low, and remains in that state until calibration is complete. The ORP output returns to normal operation at that time, so it is important that the analog input be within the converter's full-scale range in order to observe the transition. If the input is in an over-range state the ORP pin will stay high and it will not be possible to detect the end of the calibration cycle.

While RST is low, the output clock (CLKOUTP/CLKOUTN) stops toggling and is set low. Normal operation of the output clock resumes at the next input clock edge (CLKP/CLKN) after RST is deasserted. At 275MSPS the nominal calibration time is ~240ms.

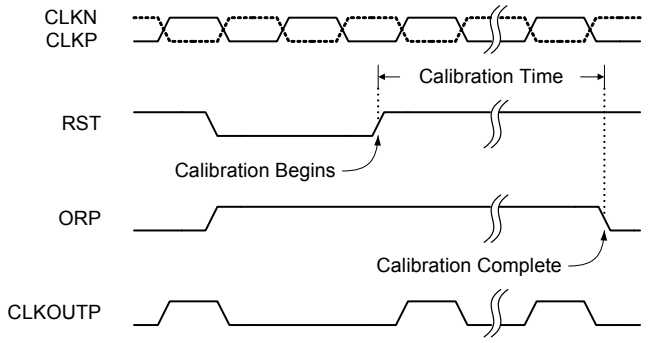


FIGURE 21. CALIBRATION TIMING

Voltage Reference

The VREF pin is the reference voltage which sets the full-scale input voltage for the chip. This pin requires a bypass capacitor of 0.1µF at a minimum. The internally generated bandgap reference voltage is provided by an on-chip voltage buffer. This buffer can sink or source up to 50µA externally.

An external voltage may be applied to this pin to provide a more accurate reference than the internally generated bandgap voltage, or to match the full-scale reference for multiple KAD2710L chips.One option in the latter configuration is to use one KAD2710L's internally generated reference as the external reference voltage for the other chips in the system. Additionally, an externally provided reference can be changed from the nominal value to adjust the full-scale input voltage within a limited range.

To select whether the full-scale reference is internally generated or externally provided, the digital input VREFSEL is set low for internal, or high for external.This pin has internal pull-up.use the internally generated reference VREFSEL can be tied directly to AVSS, and to use an external reference VREFSEL can be left unconnected.

Analog Input

The ADC core contains a fully differential input (INP/INN) to the sample and hold circuit. The ideal full-scale input voltage is 1.50V, centered at the VCM voltage of 0.86V as shown in Figure 22.

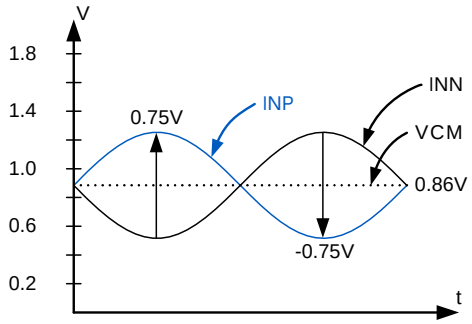


FIGURE 22. ANALOG INPUT RANGE

Best performance is obtained when the analog inputs are driven differentially. The common-mode output voltage, VCM, should be used to properly bias the inputs as shown in Figures 23 and 24. An RF transformer will give the best noise and distortion performance for wideband and/or high intermediate frequency (IF) inputs. Two different transformer input schemes are shown in Figures 23 and 24.

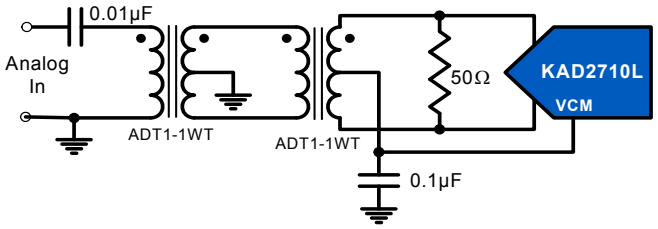


FIGURE 23. TRANSFORMER INPUT, GENERAL APPLICATION

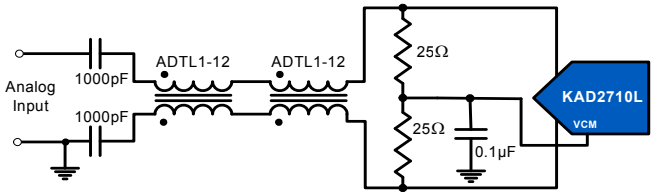


FIGURE 24. TRANSFORMER INPUT FOR HIGH IF APPLICATIONS

A back-to-back transformer scheme is used to improve common-mode rejection, which keeps the common-mode level of the input matched to V_{CM}. The value of the shunt resistor should be determined based on the desired load impedance.

The sample and hold circuit design uses a switched capacitor input stage, which creates current spikes when the sampling capacitance is reconnected to the input voltage. This creates a disturbance at the input which must settle before the next sampling point. Lower source impedance will result in faster settling and improved performance. Therefore a 1:1 transformer and low shunt resistance are recommended for optimal performance.

A differential amplifier can be used in applications that require dc coupling. In this configuration the amplifier will typically determine the achievable SNR and distortion. A typical differential amplifier circuit is shown in Figure 25.

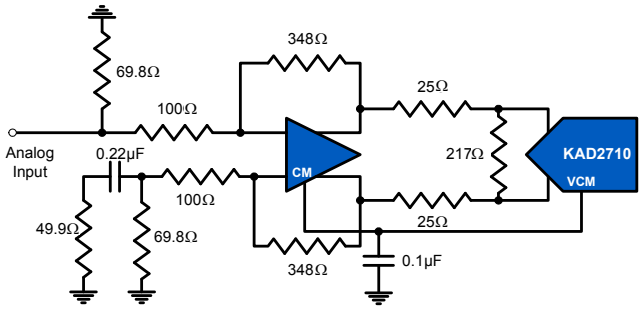


FIGURE 25. DIFFERENTIAL AMPLIFIER INPUT

Clock Input

The sample clock input circuit is a differential pair (see Figure 29). Driving these inputs with a high level (up to $1.8V_{PP}$ on each input) sine or square wave will provide the lowest jitter performance.

The recommended drive circuit is shown in Figure 26. The clock can be driven single-ended, but this will reduce the edge rate and may impact SNR performance.

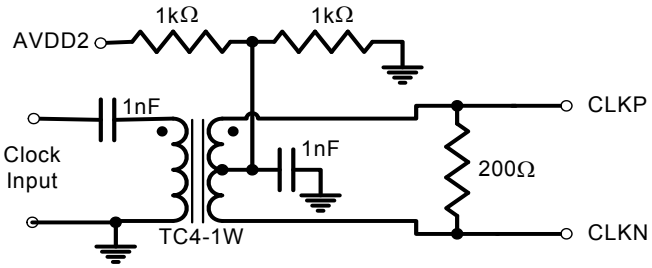


FIGURE 26. RECOMMENDED CLOCK DRIVE

Use of the clock divider is optional. The KAD2710L's ADC requires a clock with 50% duty cycle for optimum performance. If such a clock is not available, one option is to generate twice the desired sampling rate and use the KAD2710L's divide-by-2 setting. This frequency divider uses the rising edge of the clock, so 50% clock duty cycle is assured. Table 2 describes the CLKDIV connection.

TABLE 2. CLKDIV PIN SETTINGS

CLKDIV PIN	DIVIDE RATIO
AVSS	2
AVDD	1

CLKDIV is internally pulled low, so a pull-up resistor or logic driver must be connected for undivided clock.

Jitter

In a sampled data system, clock jitter directly impacts the achievable SNR performance. The theoretical relationship between clock jitter (t_J) and SNR is shown in Equation 1 and is illustrated in Figure 27.

$$SNR = 20 \log_{10}\left(\frac{1}{2\pi f_{IN} t_J}\right) \quad \text{(EQ. 1)}$$

Where t_J is the RMS uncertainty in the sampling instant.

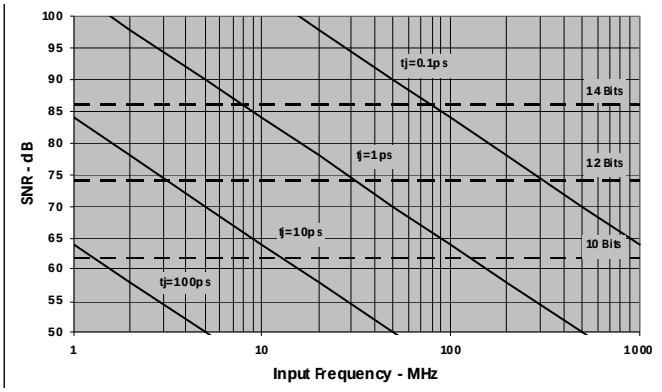


FIGURE 27. SNR vs CLOCK JITTER

This relationship shows the SNR that would be achieved if clock jitter were the only non-ideal factor. In reality, achievable SNR is limited by internal factors such as linearity, aperture jitter and thermal noise. Internal aperture jitter is the uncertainty in the sampling instant shown in Figure 1.

Any internal aperture jitter combines with the input clock jitter in a root-sum-square fashion, since they are not statistically correlated, and this determines the total jitter in the system. The total jitter, combined with other noise sources, then determines the achievable SNR.

Digital Outputs

Data is output on a parallel bus with LVDS-compatible drivers.

The output format (Binary or Two's Complement) is selected via the 2SC pin as shown in Table 3.

TABLE 3. 2SC PIN SETTINGS

2SC PIN	MODE
AVSS	Two's Complement
AVDD (or unconnected)	Binary

Equivalent Circuits

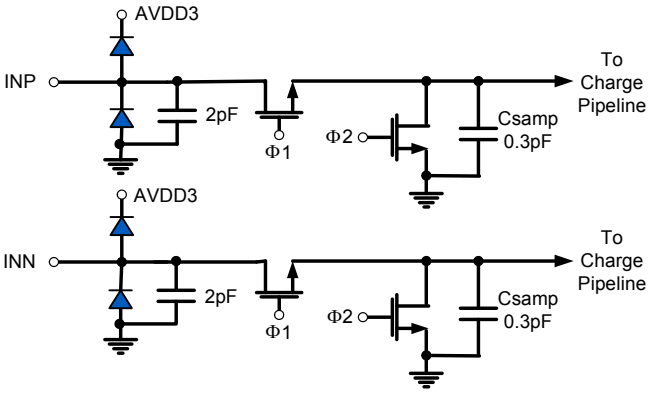


FIGURE 28. ANALOG INPUTS

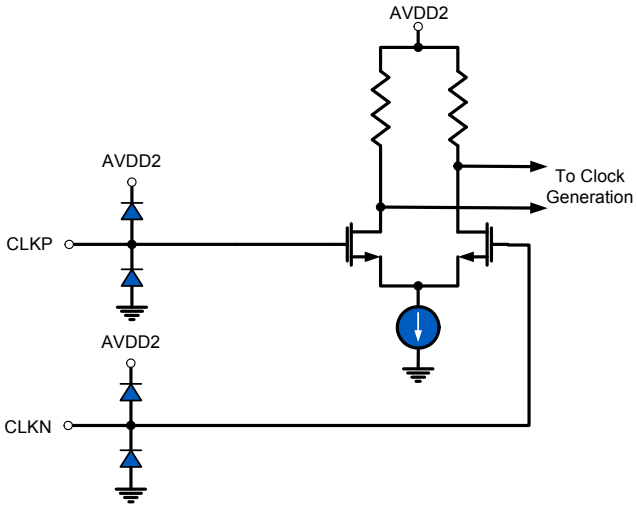


FIGURE 29. CLOCK INPUTS

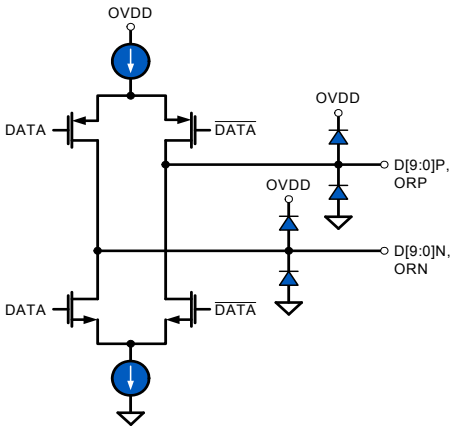


FIGURE 30. LVDS OUTPUTS

Layout Considerations

Split Ground and Power Planes

Data converters operating at high sampling frequencies require extra care in PC board layout. If analog and digital ground planes are separate, analog supply and ground planes should be laid out under signal and clock inputs and digital planes under outputs and logic pins. Grounds should be joined under the chip.

Clock Input Considerations

Use matched transmission lines to the inputs for the analog input and clock signals. Locate transformers, drivers and terminations as close to the chip as possible.

Bypass and Filtering

Bulk capacitors should have low equivalent series resistance. Tantalum is recommended. Keep ceramic bypass capacitors very close to device pins. Longer traces will increase inductance, resulting in diminished dynamic performance and accuracy. Make sure that connections to ground are direct, and low impedance.

LVDS Outputs

Output traces and connections must be designed for 50Ω (100Ω differential) characteristic impedance. Keep trace lengths equal, and minimize bends where possible. Avoid crossing ground and power-plane breaks with signal traces.

Unused Inputs

The RST and 2SC inputs are internally pulled up, and can be left open-circuit if not used.

CLKDIV is internally pulled low, which divides the input clock by two.

VREFSEL is internally pulled up. It must be held low for internal reference, but can be left open for external reference.

Definitions

Analog Input Bandwidth is the analog input frequency at which the spectral output power at the fundamental frequency (as determined by FFT analysis) is reduced by 3dB from its full-scale low-frequency value. This is also referred to as Full Power Bandwidth.

Aperture Delay or Sampling Delay is the time required after the rise of the clock input for the sampling switch to open, at which time the signal is held for conversion.

Aperture Jitter is the RMS variation in aperture delay for a set of samples.

Clock Duty Cycle is the ratio of the time the clock wave is at logic high to the total time of one clock period.

Differential Non-Linearity (DNL) is the deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB) is an alternate method of specifying Signal to Noise-and-Distortion Ratio (SINAD). In dB, it is calculated as: ENOB = (SINAD - 1.76)/6.02

Gain Error is the ratio of the difference between the voltages that cause the lowest and highest code transitions to the full-scale voltage (less 2 LSB). It is typically expressed in percent.

Integral Non-Linearity (INL) is the deviation of each individual code from a line drawn from negative full-scale (1/2 LSB below the first code transition) through positive full-scale (1/2 LSB above the last code transition). The deviation of any given code from this line is measured from the center of that code.

Least Significant Bit (LSB) is the bit that has the smallest value or weight in a digital word. Its value in terms of input voltage is $V_{FS}/(2^N-1)$ where N is the resolution in bits.

Missing Codes are output codes that are skipped and will never appear at the ADC output. These codes cannot be reached with any input value.

Most Significant Bit (MSB) is the bit that has the largest value or weight.

Pipeline Delay, or latency, is the number of clock cycles between the initiation of a conversion and the appearance at the output pins of the data.

Power Supply Rejection Ratio (PSRR) is the ratio of a change in input voltage necessary to correct a change in output code that results from a change in power supply voltage.

Signal to Noise-and-Distortion (SINAD) is the ratio of the RMS signal amplitude to the RMS sum of all other spectral components below one half the clock frequency, including harmonics but excluding DC.

Signal-to-Noise Ratio (SNR) (without Harmonics) is the ratio of the RMS signal amplitude to the RMS sum of all other spectral components below one-half the sampling frequency, excluding harmonics and DC.

SNR and SINAD are either given in units of dBc when the power level of the fundamental is used as the reference, or dBFS (dB to full scale) when the converter's full-scale input power is used as the reference.

Spurious-Free-Dynamic Range (SFDR) is the ratio of the RMS signal amplitude to the RMS value of the peak spurious spectral component. The peak spurious spectral component may or may not be a harmonic.

Two-Tone SFDR is the ratio of the RMS value of the lowest power input tone to the RMS value of the peak spurious component, which may or may not be an IMD product.

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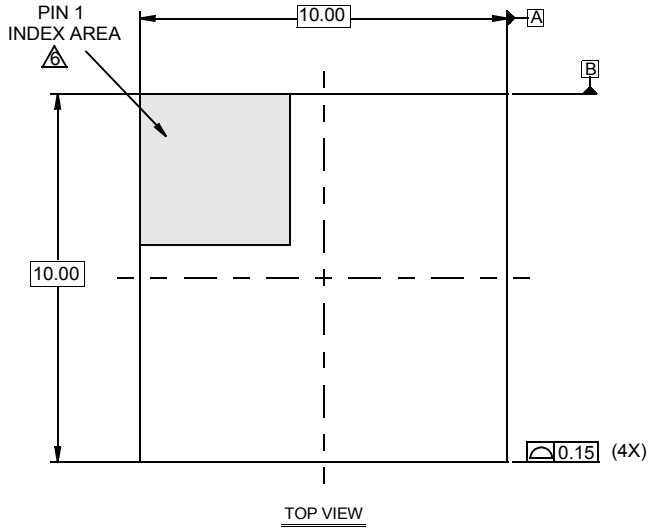
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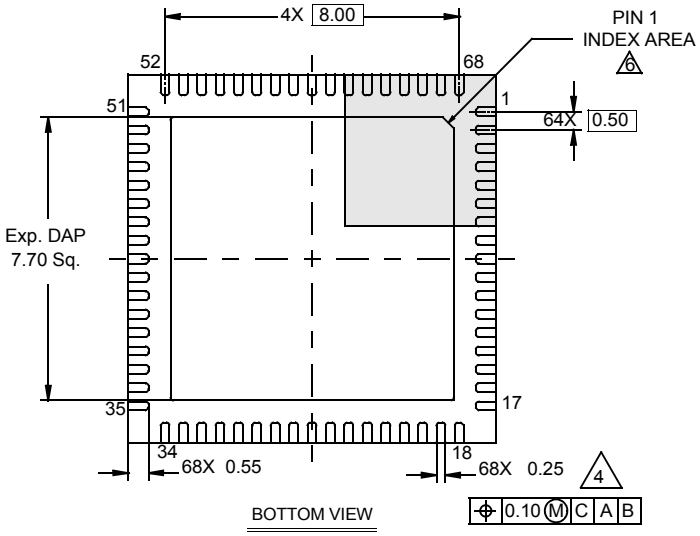
Package Outline Drawing

L68.10x10B

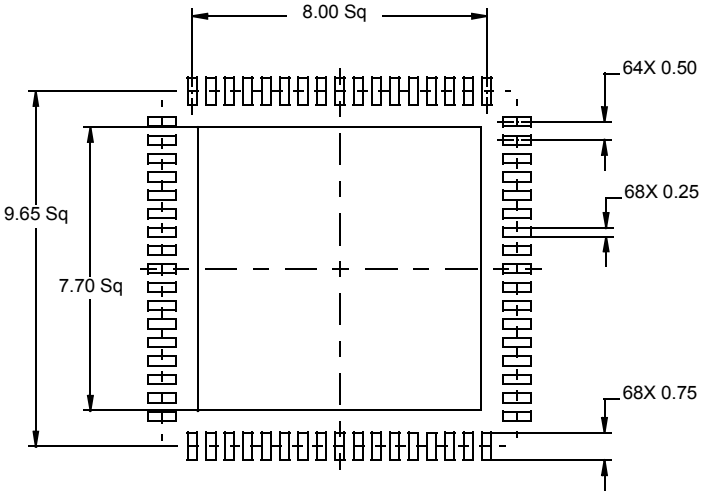
68 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 11/08



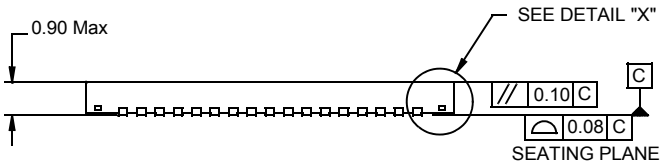
TOP VIEW



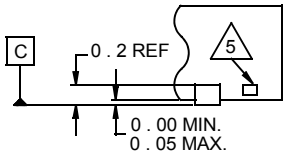
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.