LMC6041 CMOS Single Micropower Operational Amplifier

Check for Samples: LMC6041

FEATURES

- **Low Supply Current: 14 µA (Typ)**
- **Operates from 4.5V to 15.5V Single Supply**
- **Ultra Low Input Current: 2 fA (Typ)**
- **Rail-to-Rail Output Swing**
- **Input Common-Mode Range Includes Ground**

APPLICATIONS

- **Battery Monitoring and Power Conditioning**
- **Photodiode and Infrared Detector Preamplifier**
- **Silicon Based Transducer Systems**
- **Hand-Held Analytic Instruments**
- **pH Probe Buffer Amplifier**
- **Fire and Smoke Detection Systems**
- **Charge Amplifier for Piezoelectric Transducers**

DESCRIPTION

Ultra-low power consumption and low input-leakage current are the hallmarks of the LMC6041. Providing input currents of only 2 fA typical, the LMC6041 can operate from a single supply, has output swing extending to each supply rail, and an input voltage range that includes ground.

The LMC6041 is ideal for use in systems requiring ultra-low power consumption. In addition, the insensitivity to latch-up, high output drive, and output swing to ground without requiring external pull-down resistors make it ideal for single-supply battery-powered systems.

Other applications for the LMC6041 include bar code reader amplifiers, magnetic and electric field detectors, and hand-held electrometers.

This device is built with TI's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6042 for a dual, and the LMC6044 for a quad amplifier with these features.

Connection Diagrams

Top View

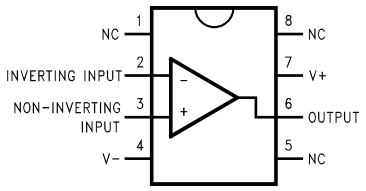


Figure 1. 8-Pin SOIC or PDIP Package
See Package Number D0008A or P0008E

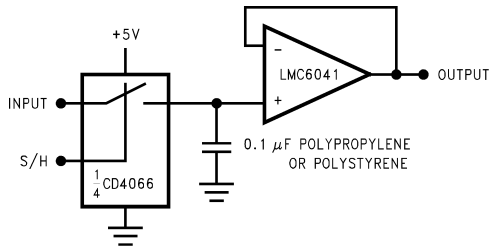


Figure 2. Low-Leakage Sample and Hold

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^-	See(3)
Output Short Circuit to V^+	See(4)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	110°C
ESD Tolerance(5)	500V
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Voltage at Input/Output Pin	(V^+) + 0.3V, (V^-) − 0.3V
Power Dissipation	See(6)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 110°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(4) Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.
(5) Human body model, 1.5 kΩ in series with 100 pF.
(6) The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Operating Ratings

Temperature Range	LMC6041AI, LMC6041I	$-40°C \le T_J \le +85°C$
Supply Voltage		$4.5V \le V^+ \le 15.5V$
Power Dissipation		See(1)
Thermal Resistance (θ_{JA})(2)	8-Pin PDIP package	101°C/W
	8-Pin SOIC package	165°C/W

(1) For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.
(2) All numbers apply for packages soldered directly into a PC board.

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Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Parameter		Test Conditions		Typical (1)	LMC6041AI Limit (2)	LMC6041I Limit (2)	Units (Limit)
V_{OS}	Input Offset Voltage			1	3	6	mV
					3.3	**6.3**	max
TCV_{OS}	Input Offset Voltage Average Drift			1.3			µV/°C
I_B	Input Bias Current			0.002	**4**	**4**	pA max
I_{OS}	Input Offset Current			0.001	**2**	**2**	pA max
R_{IN}	Input Resistance			>10			TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$		75	68	62	dB
					66	**60**	min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		75	68	62	dB
					66	**60**	min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$ $V_O = 2.5V$		94	84	74	dB
					83	**73**	min
CMR	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 50 dB		−0.4	−0.1	−0.1	V
					0	**0**	max
				$V^+ - 1.9V$	$V^+ - 2.3V$	$V^+ - 2.3V$	V
					$V^+ - 2.5V$	**$V^+ - 2.4V$**	min
A_V	Large Signal Voltage Gain	$R_L = 100 k\Omega$ (3)	Sourcing	1000	400	300	V/mV
					300	**200**	min
			Sinking	500	180	90	V/mV
					120	**70**	min
		$R_L = 25 k\Omega$ (3)	Sourcing	1000	200	100	V/mV
					160	**80**	min
			Sinking	250	100	50	V/mV
					60	**40**	min
V_O	Output Swing	$V^+ = 5V$ $R_L = 100 k\Omega$ to $V^+/2$		4.987	4.970	4.940	V
					4.950	**4.910**	min
				0.004	0.030	0.060	V
					0.050	**0.090**	max
		$V^+ = 5V$ $R_L = 25 k\Omega$ to $V^+/2$		4.980	4.920	4.870	V
					4.870	**4.820**	min
				0.010	0.080	0.130	V
					0.130	**0.180**	max
		$V^+ = 15V$ $R_L = 100 k\Omega$ to $V^+/2$		14.970	14.920	14.880	V
					14.880	**14.820**	min
				0.007	0.030	0.060	V
					0.050	**0.090**	max
		$V^+ = 15V$ $R_L = 25 k\Omega$ to $V^+/2$		14.950	14.900	14.850	V
					14.850	**14.800**	min
				0.022	0.100	0.150	V
					0.150	**0.200**	max

(1) Typical Values represent the most likely parametric norm.
(2) All limits are ensured at room temperature (standard type face) or at operating temperature extremes (bold face type).
(3) $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

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Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Parameter		Test Conditions	Typical (1)	LMC6041AI Limit (2)	LMC6041I Limit (2)	Units (Limit)
I_{SC}	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16	13	mA
				10	**8**	min
		Sinking, $V_O = 5V$	21	16	13	mA
				8	**8**	min
I_{SC}	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	15	15	mA
				10	**10**	min
		Sinking, $V_O = 13V$ (4)	39	24	21	mA
				8	**8**	min
I_S	Supply Current	$V_O = 1.5V$	14	20	26	µA
				24	**30**	max
		$V^+ = 15V$	18	26	34	µA
				31	**39**	max

(4) Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

AC Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Parameter		Test Conditions	Typ (1)	LMC6041AI	LMC6041I	Units (Limit)
				Limit (2)	Limit (2)	
SR	Slew Rate	See (3)	0.02	0.015	0.010	V/µs
				0.010	**0.007**	min
GBW	Gain-Bandwidth Product		75			kHz
φ_m	Phase Margin		60			Deg
e_n	Input-Referred Voltage Noise	F = 1 kHz	83			nV/√Hz
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002			pA/√Hz
THD	Total Harmonic Distortion	F = 1 kHz, $A_V = -5$ $R_L = 100\ k\Omega$, $V_O = 2\ V_{pp}$ ±5V Supply	0.01			%

(1) Typical Values represent the most likely parametric norm.
(2) All limits are ensured at room temperature (standard type face) or at operating temperature extremes (bold face type).
(3) $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified in the slower of the positive and negative slew rates.

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Typical Performance Characteristics

V_S = ± 7.5V, T_A = 25°C unless otherwise specified

Supply Current vs Supply Voltage

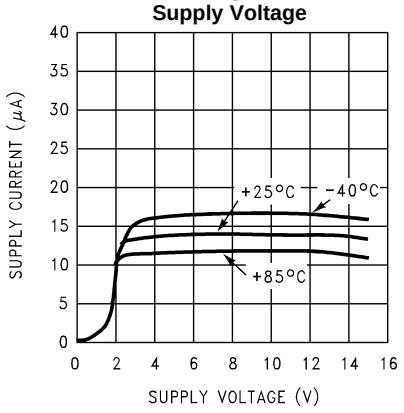


Figure 3.

Offset Voltage vs Temperature of Five Representative Units

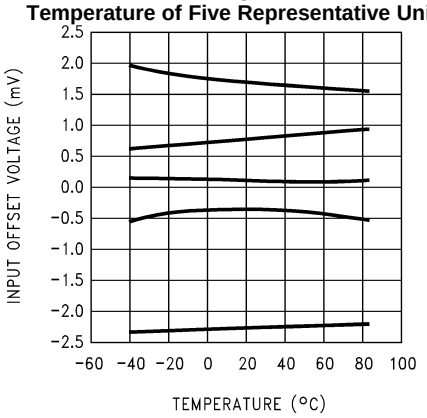


Figure 4.

Input Bias Current vs Temperature

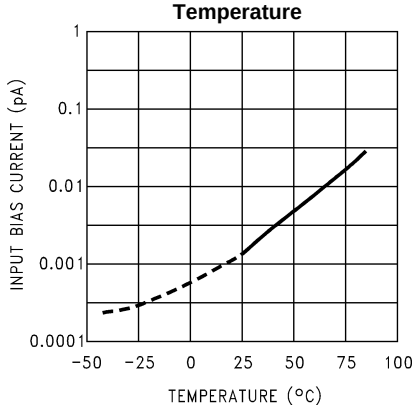


Figure 5.

Input Bias Current vs Input Common-Mode Voltage

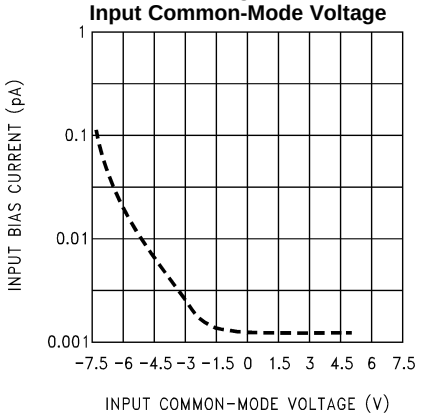


Figure 6.

Input Common-Mode Voltage Range vs Temperature

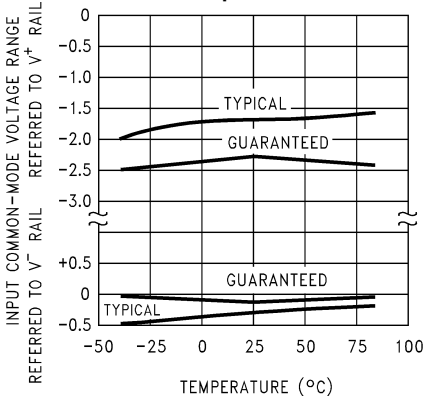


Figure 7.

Output Characteristics Current Sinking

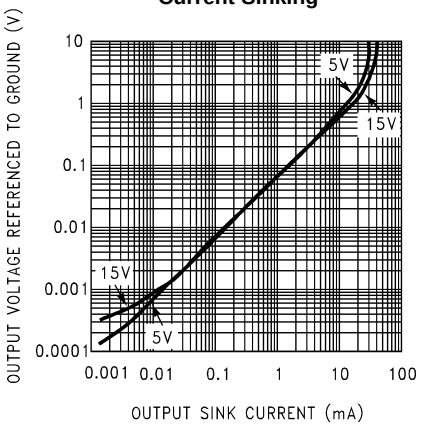


Figure 8.

Typical Performance Characteristics (continued)

V_S = ± 7.5V, T_A = 25°C unless otherwise specified

Output Characteristics Current Sourcing

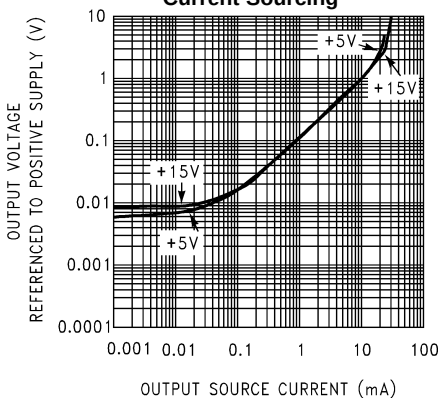


Figure 9.

Input Voltage Noise vs Frequency

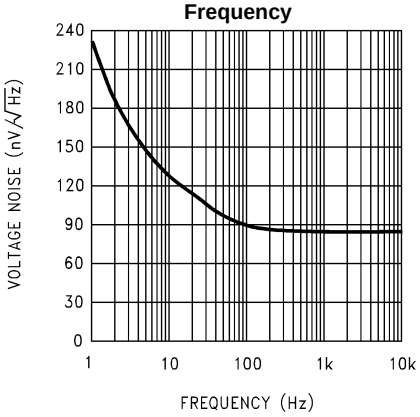


Figure 10.

Power Supply Rejection Ratio vs Frequency

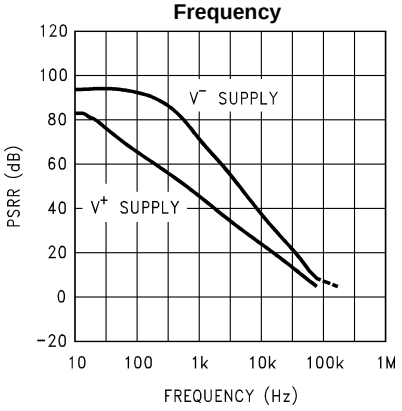


Figure 11.

CMRR vs Frequency

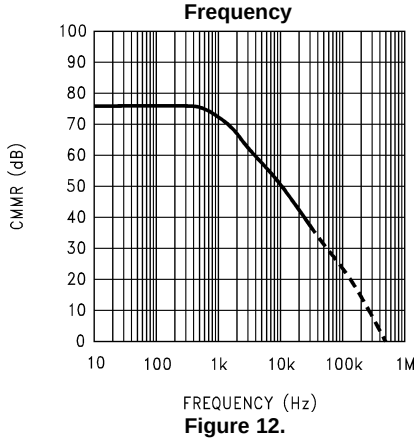


Figure 12.

CMRR vs Temperature

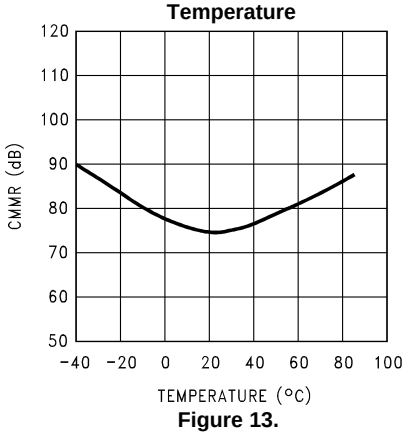


Figure 13.

Open-Loop Voltage Gain vs Temperature

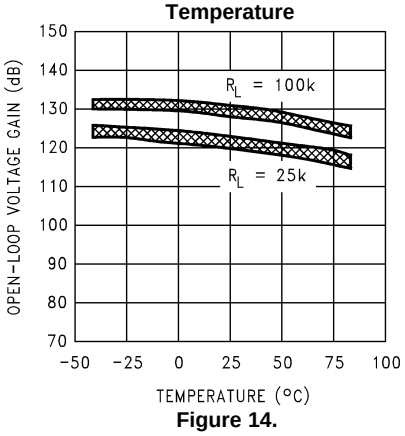


Figure 14.

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Typical Performance Characteristics (continued)

V_S = ± 7.5V, T_A = 25°C unless otherwise specified

Open-Loop Frequency Response

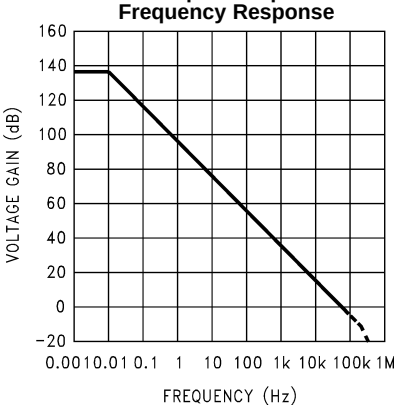


Figure 15.

Gain and Phase Responses vs Load Capacitance

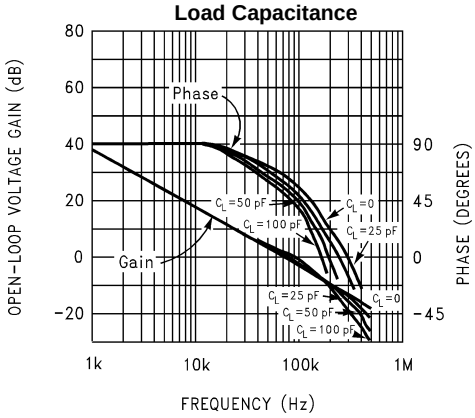


Figure 16.

Gain and Phase Responses vs Temperature

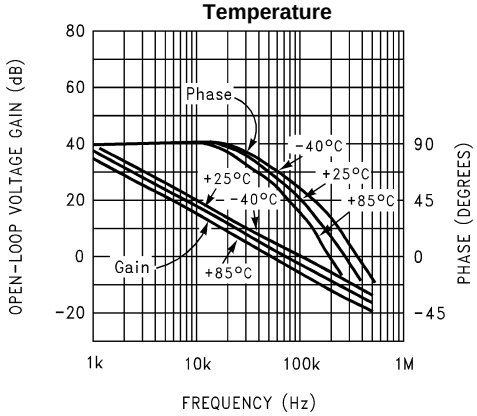


Figure 17.

Gain Error (V_{OS} vs V_{OUT})

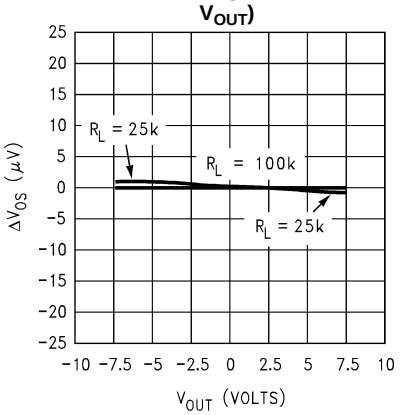


Figure 18.

Common-Mode Error vs Common-Mode Voltage of Three Representative Units

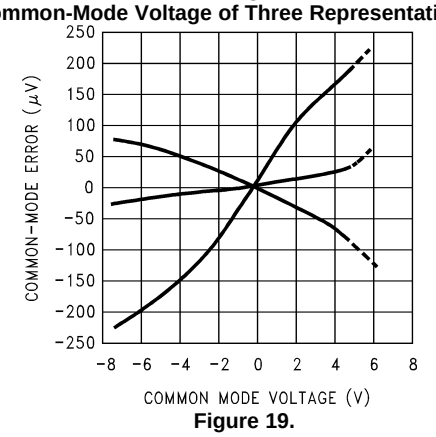


Figure 19.

Non-Inverting Slew Rate vs Temperature

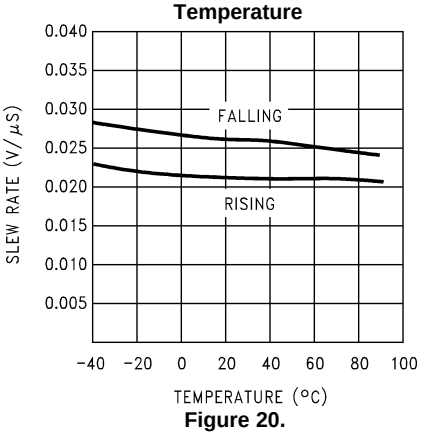


Figure 20.

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Typical Performance Characteristics (continued)

V_S = ± 7.5V, T_A = 25°C unless otherwise specified

Inverting Slew Rate vs Temperature

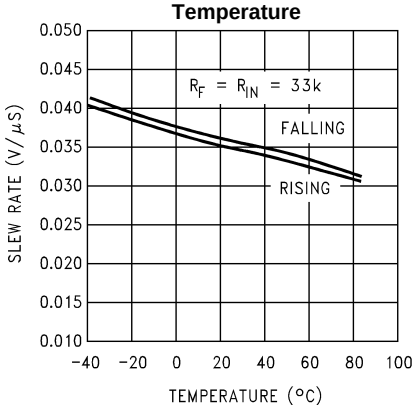


Figure 21.

Non-Inverting Large Signal Pulse Response (A_V = +1)

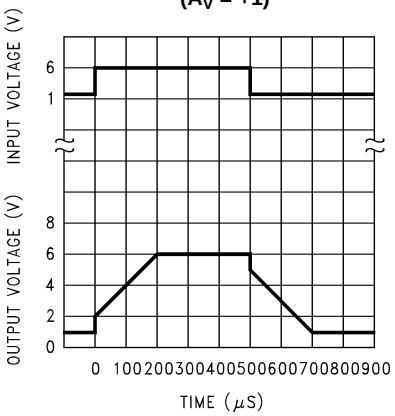


Figure 22.

Non-Inverting Small Signal Pulse Response

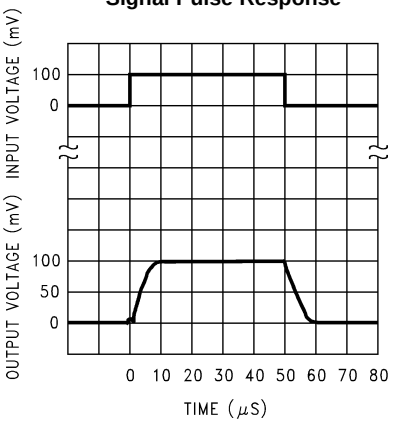


Figure 23.

Inverting Large-Signal Pulse Response

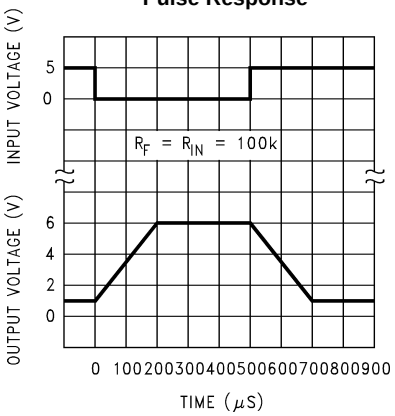


Figure 24.

Inverting Small Signal Pulse Response

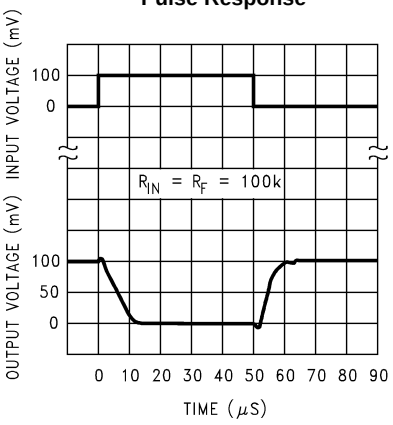


Figure 25.

Stability vs Capacitive Load (A_V = +1)

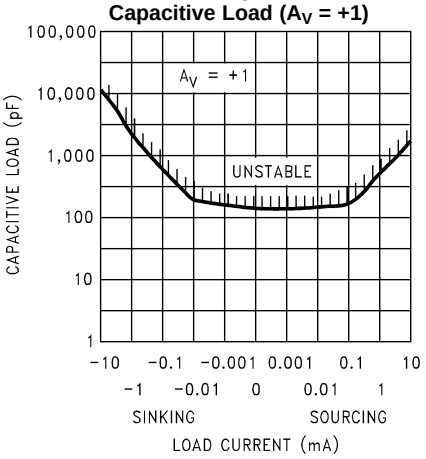


Figure 26.

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Typical Performance Characteristics (continued)

V_S = ± 7.5V, T_A = 25°C unless otherwise specified

Stability vs Capacitive Load (A_V = ±10)

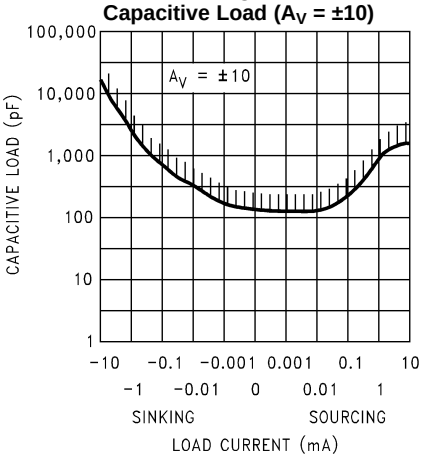


Figure 27.

APPLICATIONS HINTS

AMPLIFIER TOPOLOGY

The LMC6041 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6041 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance with amplifiers with ultra-low input current, like the LMC6041.

Although the LMC6041 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuits board parasitics, reduce phase margins.

When high input impedance are demanded, guarding of the LMC6041 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See Printed-Circuit-Board Layout for High Impedance Work.)

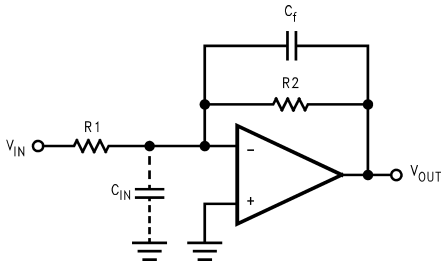


Figure 28. Cancelling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a capacitor. Adding a capacitor, C_f, around the feedback resistor (as in Figure 28) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (1)$$

or

$$R_1 C_{IN} \leq R_2 C_f \quad (2)$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

CAPACITIVE LOAD TOLERANCE

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in Figure 29.

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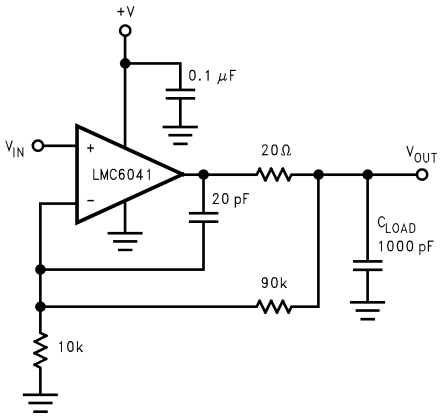


Figure 29. LMC6041 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of Figure 29, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 30). Typically a pull up resistor conducting 10 µA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

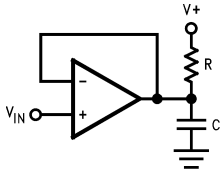


Figure 30. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6041, typically less than 2fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6041's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 31. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifer inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6041's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figure 34 for typical connections of guard rings for standard op-amp configurations.

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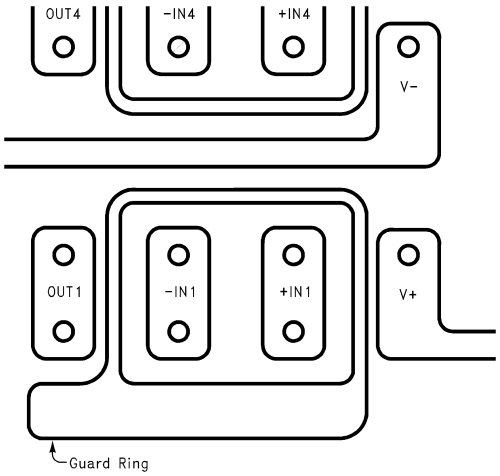


Figure 31. Example of Guard Ring in P.C. Board Layout

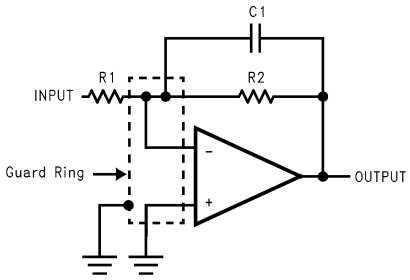


Figure 32. Inverting Amplifier

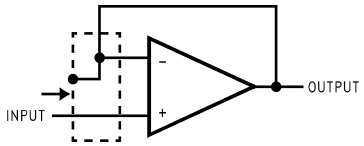
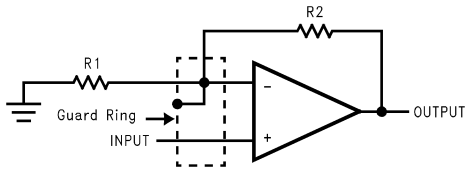


Figure 33. Follower

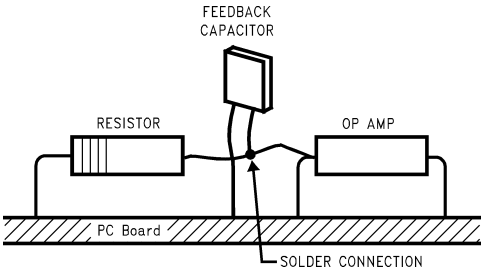


Non-Inverting Amplifier

Figure 34. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 35.

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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

Figure 35. Air Wiring

Typical Single-Supply Applications

(V^+ = 5.0 V_{DC})

The extremely high input impedance, and low power consumption, of the LMC6041 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these type of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

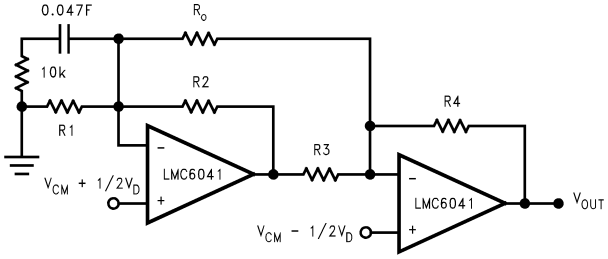


Figure 36. Two Op-Amp Instrumentation Amplifier

The circuit in Figure 36 is recommended for applications where the common-mode input range is relatively low and the differential gain will be in the range of 10 to 1000. This two op-amp instrumentation amplifier features an independent adjustment of the gain and common-mode rejection trim, and a total quiescent supply current of less than 28 µA. To maintain ultra-high input impedance, it is advisable to use ground rings and consider PC board layout an important part of the overall system design (see Printed-Circuit-Board Layout for High Impedance Work). Referring to Figure 36, the input voltages are represented as a common-mode input V_{CM} plus a differential input V_D.

Rejection of the common-mode component of the input is accomplished by making the ratio of R1/R2 equal to R3/R4. So that where,

$$\frac{R3}{R4} = \frac{R2}{R1}$$

$$V_{OUT} = \frac{R4}{R3}\left(1 + \frac{R3}{R4} + \frac{R2 + R3}{R_O}\right) V_D \quad (3)$$

A suggested design guideline is to minimize the difference of value between R1 through R4. This will often result in improved resistor tempco, amplifier gain, and CMRR over temperature. If RN = R1 = R2 = R3 = R4 then the gain equation can be simplified:

$$V_{OUT} = 2\left(1 + \frac{RN}{R_O}\right) V_D \quad (4)$$

Due to the “zero-in, zero-out” performance of the LMC6041, and output swing rail-rail, the dynamic range is only limited to the input common-mode range of 0V to V_S–2.3V, worst case at room temperature. This feature of the LMC6041 makes it an ideal choice for low-power instrumentation systems.

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A complete instrumentation amplifier designed for a gain of 100 is shown in Figure 37. Provisions have been made for low sensitivity trimming of CMRR and gain.

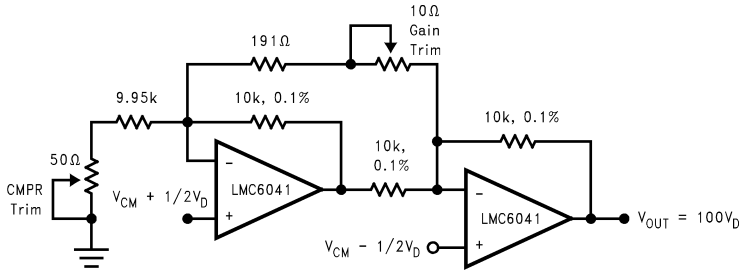


Figure 37. Low-Power Two-Op-Amp Instrumentation Amplifier

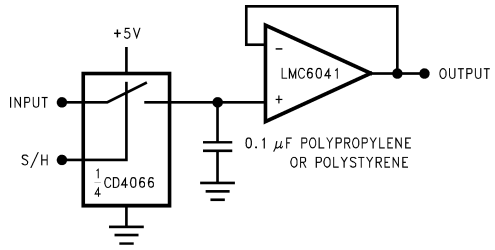


Figure 38. Low-Leakage Sample and Hold

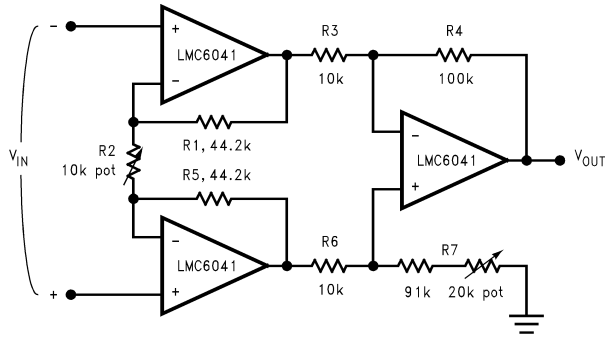


Figure 39. Instrumentation Amplifier

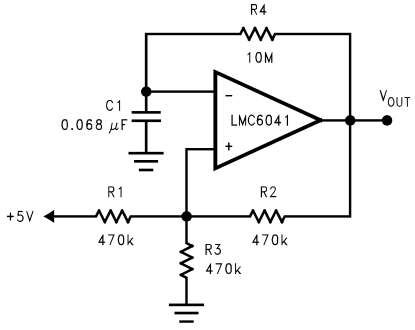


Figure 40. 1 Hz Square-Wave Oscillator

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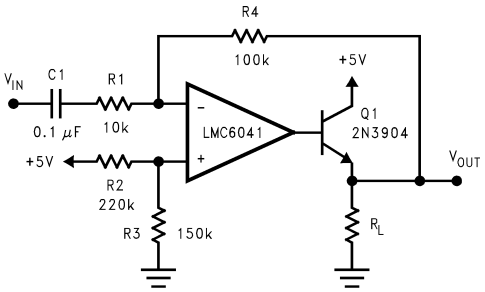


Figure 41. AC Coupled Power Amplifier

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	15

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6041AIM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMC60 41AIM	
LMC6041AIM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC60 41AIM	Samples
LMC6041AIMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC60 41AIM	Samples
LMC6041IM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMC60 41IM	
LMC6041IM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC60 41IM	Samples
LMC6041IMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 85	LMC60 41IM	Samples
LMC6041IN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-NA-UNLIM	-40 to 85	LMC60 41IN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

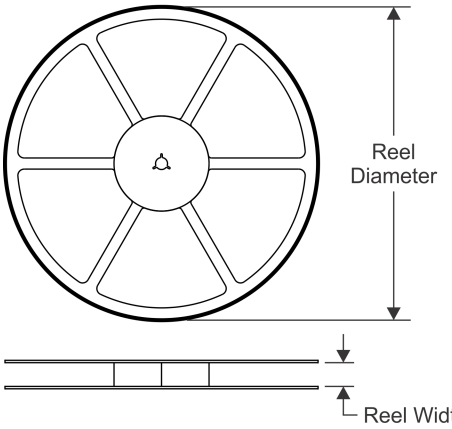
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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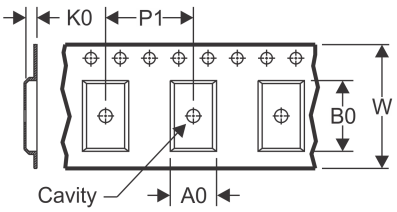
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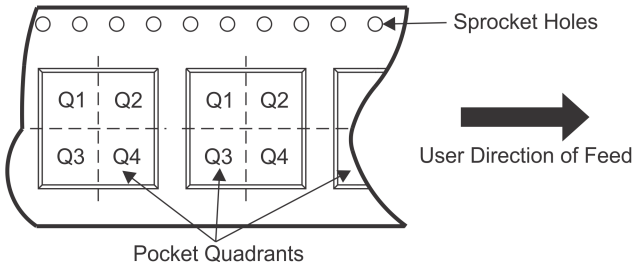


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

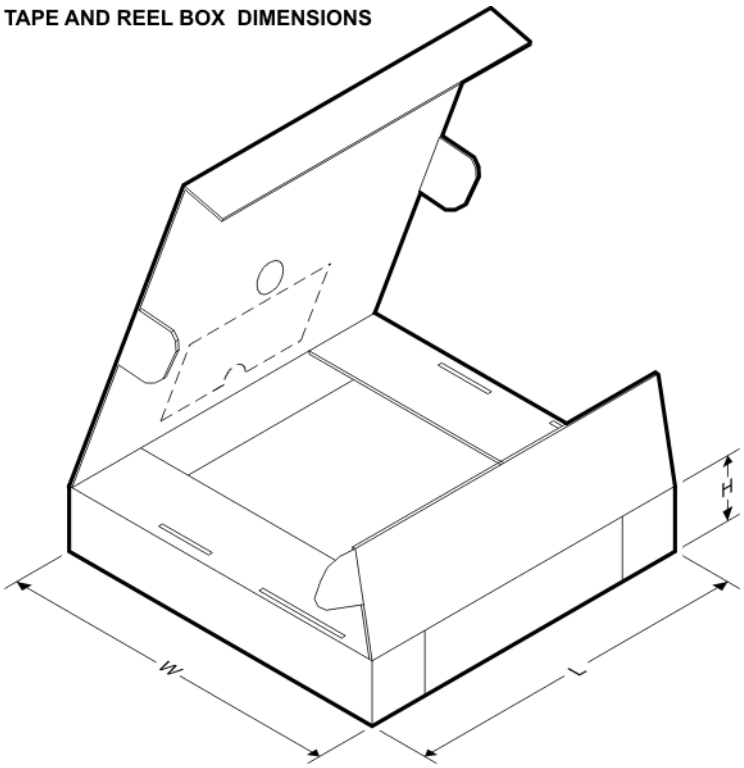
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6041AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6041IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

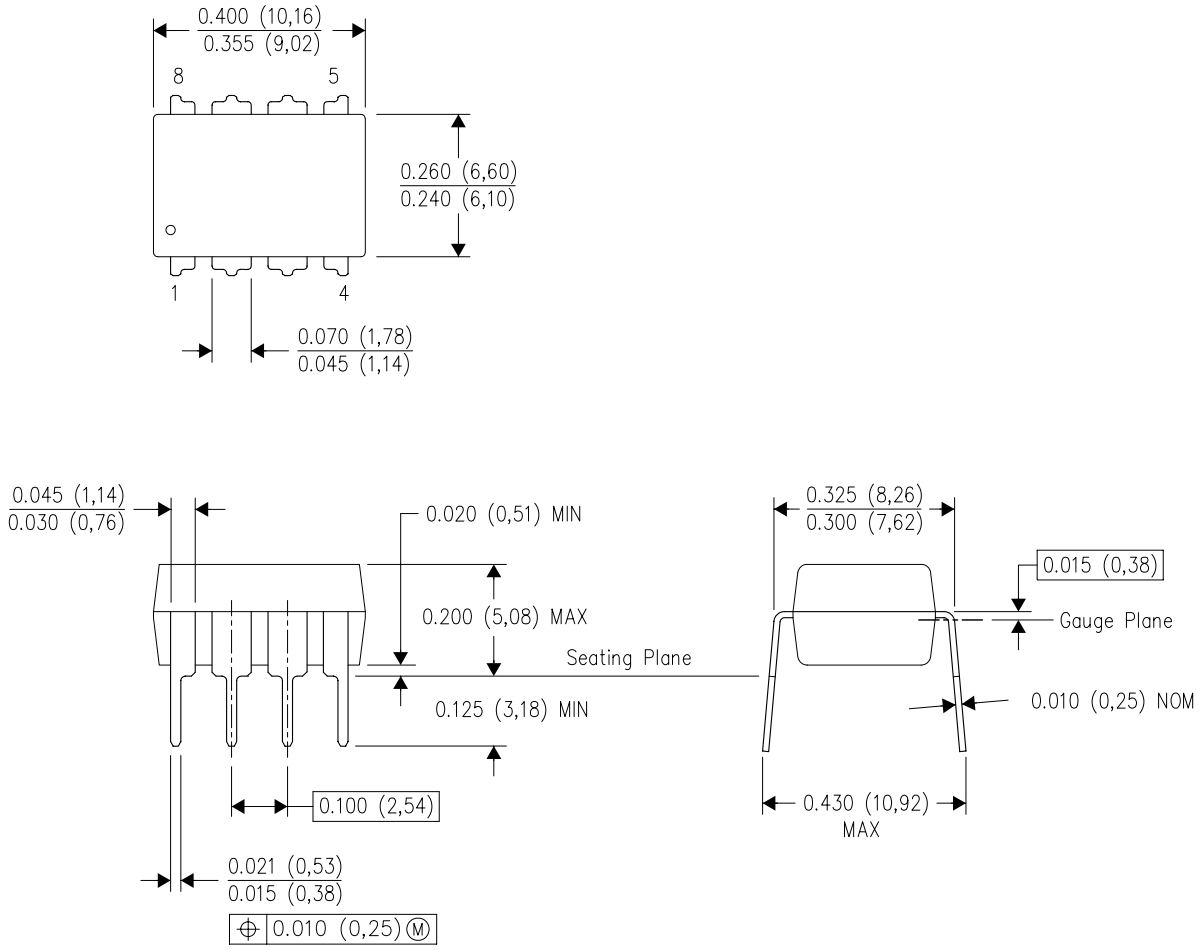
TAPE AND REEL BOX DIMENSIONS



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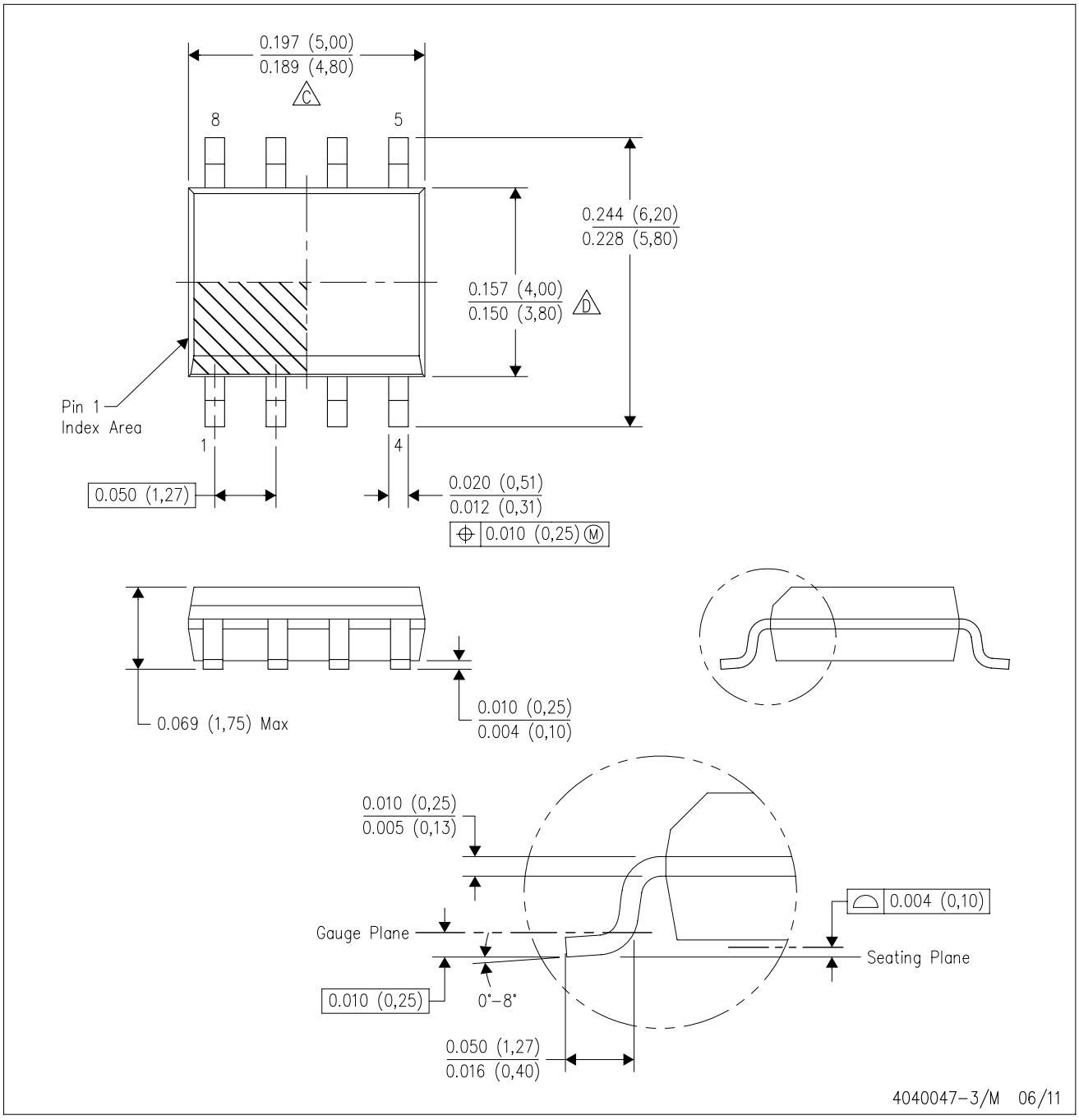
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6041AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6041IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

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NOTES:
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B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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NOTES:
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D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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