

LMK60XX High-Performance Low Jitter Oscillator

1 Features

- Low Noise, High Performance
 - Jitter: 150 fs RMS typical Fout > 100 MHz
 - PSRR: –60 dBc, Robust Supply Noise Immunity
- Supported Output Format
 - LVPECL and LVDS up to 800 MHz
 - HCSL up to 400 MHz
- Total Frequency Tolerance of ± 50 ppm (LMK60X2) and ± 25 ppm (LMK60X0)
- 3.3 V Operating Voltage
- Industrial Temperature Range (-40°C to $+85^{\circ}\text{C}$)
- 7 mm x 5 mm 6-pin Package that is Pin-compatible with Industry Standard 7050 XO Package

2 Applications

- High-Performance Replacement for Crystal-, SAW-, or Silicon-based Oscillators
- Switches, Routers, Network Line Cards, Base Band Units (BBU), Servers, Storage/SAN
- Test and Measurement
- Medical Imaging
- FPGA, Processor Attach

3 Description

The LMK60XX is a low jitter oscillator that generates a commonly used reference clock. The device is pre-programmed in factory to support any reference clock frequency; supported output formats are LVPECL and LVDS up to 800 MHz, and HCSL up to 400 MHz. Internal power conditioning provide excellent power supply ripple rejection (PSRR), reducing the cost and complexity of the power delivery network. The device operates from a single $3.3\text{ V} \pm 5\%$ supply.

Device Information⁽¹⁾

PART NUMBER	OUTPUT FREQ (MHz) AND FORMAT	TOTAL FREQ STABILITY (ppm)	PACKAGE	BODY SIZE (NOM)
LMK60E2-150M00	150 LVPECL	± 50	6-pin QFM	7.0 mm x 5.0 mm
LMK60E2-156M25	156.25 LVPECL	± 50		
LMK60E0-156257	156.257 LVPECL	± 25		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Pinout

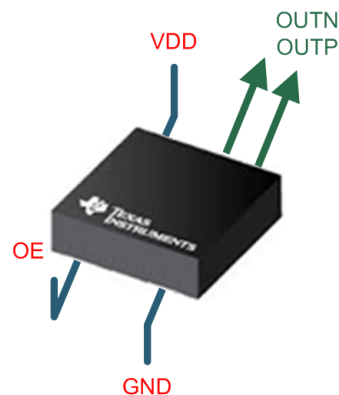
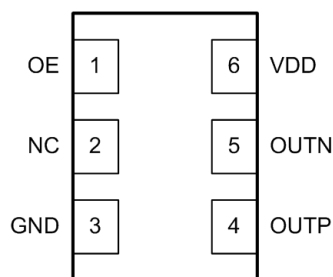


Table of Contents

1 Features	1	6.12 PSRR Characteristics	7
2 Applications	1	6.13 PLL Clock Output Jitter Characteristics	7
3 Description	1	6.14 Additional Reliability and Qualification	7
4 Revision History	2	6.15 Typical Performance Characteristics	8
5 Pin Configuration and Functions	3	7 Parameter Measurement Information	9
6 Specifications	4	7.1 Device Output Configurations	9
6.1 Absolute Maximum Ratings	4	8 Power Supply Recommendations	11
6.2 ESD Ratings	4	9 Layout	12
6.3 Recommended Operating Conditions.....	4	9.1 Layout Guidelines	12
6.4 Thermal Information	4	10 Device and Documentation Support	14
6.5 Electrical Characteristics - Power Supply	5	10.1 Related Links	14
6.6 LVPECL Output Characteristics.....	5	10.2 Receiving Notification of Documentation Updates	14
6.7 LVDS Output Characteristics	5	10.3 Community Resources.....	14
6.8 HCSL Output Characteristics.....	5	10.4 Trademarks	14
6.9 OE Input Characteristics	6	10.5 Electrostatic Discharge Caution.....	14
6.10 Frequency Tolerance Characteristics	6	10.6 Glossary	14
6.11 Power-On/Reset Characteristics (VDD).....	6	11 Mechanical, Packaging, and Orderable Information	14

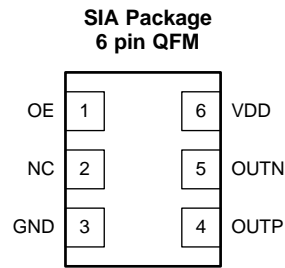
4 Revision History

Changes from Original (June 2016) to Revision A

Page

• New release of LMK60E0-156257.....	1
--------------------------------------	----------

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
POWER			
GND	3	Ground	Device Ground.
VDD	6	Analog	3.3 V Power Supply.
OUTPUT BLOCK			
OUTP, OUTN	4, 5	Universal	Differential Output Pair (LVPECL, LVDS or HCSL).
DIGITAL CONTROL / INTERFACES			
NC	2	N/A	No Connect.
OE	1	LVC MOS	Output Enable (internal pullup). When set to low, output pair is disabled and set at high impedance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
VDD	Device Supply Voltage	-0.3	3.6	V
V _{IN}	Output Voltage Range for Logic Inputs	-0.3	VDD + 0.3	V
V _{OUT}	Output Voltage Range for Clock Outputs	-0.3	VDD + 0.3	V
T _J	Junction Temperature		150	°C
T _{STG}	Storage Temperature	-40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Device Supply Voltage	3.135	3.3	3.465	V
T _A	Ambient Temperature	-40	25	85	°C
T _J	Junction Temperature			120	°C
t _{RAMP}	VDD Power-Up Ramp Time	0.1		100	ms

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	LMK60XX ^{(2) (3) (4)}			UNIT	
	QFM (SIA)				
	6 PINS				
	Airflow (LFM) 0	Airflow (LFM) 200	Airflow (LFM) 400		
R _{θJA}	Junction-to-ambient thermal resistance	55.2	46.4	43.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	34.6	n/a	n/a	
R _{θJB}	Junction-to-board thermal resistance	37.7	n/a	n/a	
ψ _{JT}	Junction-to-top characterization parameter	11.3	17.6	22.5	
ψ _{JB}	Junction-to-board characterization parameter	37.7	41.5	40.1	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) The package thermal resistance is calculated on a 4 layer JEDEC board.

(3) Connected to GND with 3 thermal vias (0.3-mm diameter).

(4) ψ_{JB} (junction to board) is used when the main heat flow is from the junction to the GND pad. Please refer to Thermal Considerations section for more information on ensuring good system reliability and quality.

6.5 Electrical Characteristics - Power Supply⁽¹⁾

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD	Device Current Consumption	LVPECL ⁽²⁾		162	208	mA
		LVDS		152	196	
		HCSL		155	196	
IDD-PD	Device Current Consumption when output is disabled	OE = GND		136		

(1) Refer to Parameter Measurement Information for relevant test conditions.

(2) On-chip power dissipation should exclude 40 mW, dissipated in the 150 Ω termination resistors, from total power dissipation.

6.6 LVPECL Output Characteristics⁽¹⁾

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{OUT}	Output Frequency ⁽²⁾		10		800	MHz
V _{OD}	Output Voltage Swing (V _{OH} - V _{OL}) ⁽²⁾		700	800	1200	mV
V _{OUT, DIFF, PP}	Differential Output Peak-to-Peak Swing			2 x V _{OD}		V
V _{OS}	Output Common Mode Voltage			VDD - 1.55		V
t _R / t _F	Output Rise/Fall Time (20% to 80%) ⁽³⁾			150	250	ps
ODC	Output Duty Cycle ⁽³⁾		45%		55%	

(1) Refer to Parameter Measurement Information for relevant test conditions.

(2) An output frequency over f_{OUT} max spec is possible, but output swing may be less than V_{OD} min spec.

(3) Ensured by characterization.

6.7 LVDS Output Characteristics⁽¹⁾

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{OUT}	Output Frequency ⁽¹⁾		10		800	MHz
V _{OD}	Output Voltage Swing (V _{OH} - V _{OL}) ⁽¹⁾		300	390	480	mV
V _{OUT, DIFF, PP}	Differential Output Peak-to-Peak Swing			2 x V _{OD}		V
V _{OS}	Output Common Mode Voltage			1.2		V
t _R / t _F	Output Rise/Fall Time (20% to 80%) ⁽²⁾			150	250	ps
ODC	Output Duty Cycle ⁽²⁾		45%		55%	
R _{OUT}	Differential Output Impedance			125		Ω

(1) An output frequency over f_{OUT} max spec is possible, but output swing may be less than V_{OD} min spec.

(2) Ensured by characterization.

6.8 HCSL Output Characteristics⁽¹⁾

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{OUT}	Output Frequency		10		400	MHz
V _{OH}	Output High Voltage		600		850	mV
V _{OL}	Output Low Voltage		-100		100	mV

(1) Refer to Parameter Measurement Information for relevant test conditions.

HCSL Output Characteristics⁽¹⁾ (continued)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{CROSS}	Absolute Crossing Voltage ⁽²⁾⁽³⁾	250		475	mV
V _{CROSS-DELTA}	Variation of V _{CROSS} ⁽²⁾⁽³⁾	0		140	mV
dV/dt	Slew Rate ⁽⁴⁾	0.8		2	V/ns
ODC	Output Duty Cycle ⁽⁴⁾	45%		55%	

(2) Measured from -150 mV to +150 mV on the differential waveform with the 300 mVpp measurement window centered on the differential zero crossing.

(3) Ensured by design.

(4) Ensured by characterization.

6.9 OE Input Characteristics

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IH}	Input High Voltage	1.4			V
V _{IL}	Input Low Voltage			0.6	V
I _{IH}	Input High Current	V _{IH} = VDD		40	μA
I _{IL}	Input Low Current	V _{IL} = GND		40	μA
C _{IN}	Input Capacitance		2		pF

6.10 Frequency Tolerance Characteristics⁽¹⁾

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
f _T	Total Frequency Tolerance	LMK60X2: All output formats, frequency bands and device junction temperature up to 120°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow and 5-year aging at 25°C	-50		50	ppm
		LMK60X0: All output formats, frequency bands and device junction temperature up to 120°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow and 5-year aging at 25°C	-25		25	ppm

(1) Ensured by characterization.

6.11 Power-On/Reset Characteristics (VDD)

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{THRESH}	Threshold Voltage ⁽¹⁾	2.72		2.95	V
V _{DROOP}	Allowable Voltage Droop ⁽²⁾			0.1	V
t _{STARTUP}	Startup Time ⁽¹⁾	Time elapsed from VDD at 3.135 V to output enabled		10	ms
t _{OE-EN}	Output enable time ⁽²⁾	Time elapsed from OE at V _{IH} to output enabled		50	μs
t _{OE-DIS}	Output disable time ⁽²⁾	Time elapsed from OE at V _{IL} to output disabled		50	μs

(1) Ensured by characterization.

(2) Ensured by design.

6.12 PSRR Characteristics⁽¹⁾

VDD = 3.3 V, T_A = 25°C, FS[1:0] = NC, NC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Spurs Induced by 50 mV Power Supply Ripple ⁽²⁾⁽³⁾ at 156.25 MHz output, all output types	Sine wave at 50 kHz		-60		dBc
		Sine wave at 100 kHz		-60		
		Sine wave at 500 kHz		-60		
		Sine wave at 1 MHz		-60		

(1) Refer to Parameter Measurement Information for relevant test conditions.

(2) Measured max spur level with 50 mVpp sinusoidal signal between 50 kHz and 1 MHz applied on VDD pin

(3) $DJ_{SPUR} (ps, pk-pk) = [2 \cdot 10(SPUR/20) / (\pi \cdot f_{OUT})] \cdot 1e6$, where PSRR or SPUR in dBc and f_{OUT} in MHz.

6.13 PLL Clock Output Jitter Characteristics⁽¹⁾⁽²⁾

VDD = 3.3 V ± 5%, T_A = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RJ	RMS Phase Jitter ⁽³⁾ (12 kHz – 20 MHz)	$f_{OUT} \geq 100$ MHz, All output types		150	250	fs RMS

(1) Refer to Parameter Measurement Information for relevant test conditions.

(2) Phase jitter measured with Agilent E5052 signal source analyzer using a differential-to-single ended converter (balun or buffer).

(3) Ensured by characterization.

6.14 Additional Reliability and Qualification

PARAMETER	CONDITION / TEST METHOD
Mechanical Shock	MIL-STD-202, Method 213
Mechanical Vibration	MIL-STD-202, Method 204
Moisture Sensitivity Level	J-STD-020, MSL3

6.15 Typical Performance Characteristics

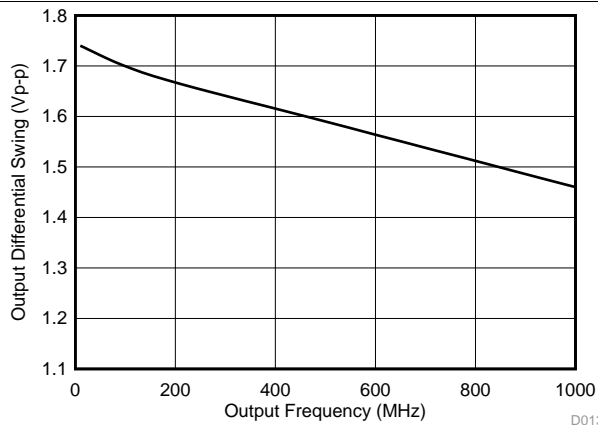


Figure 1. LVPECL Differential Output Swing vs Frequency

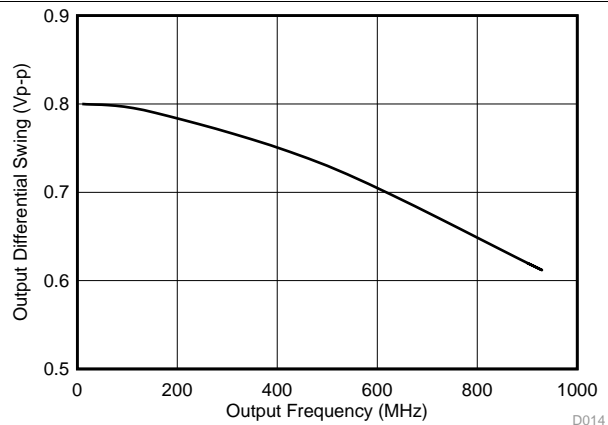


Figure 2. LVDS Differential Output Swing vs Frequency

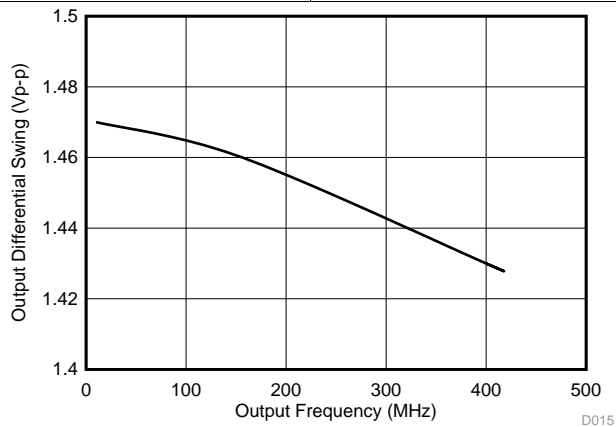


Figure 3. HCSL Differential Output Swing vs Frequency

7 Parameter Measurement Information

7.1 Device Output Configurations

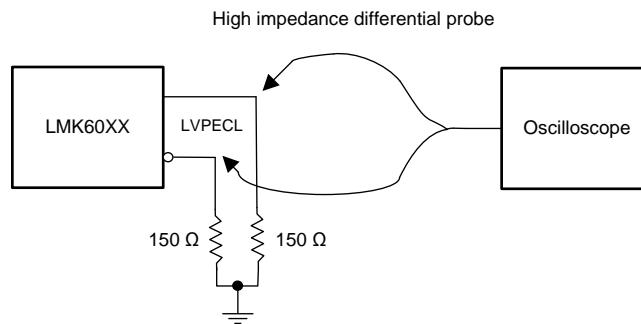


Figure 4. LVPECL Output DC Configuration During Device Test

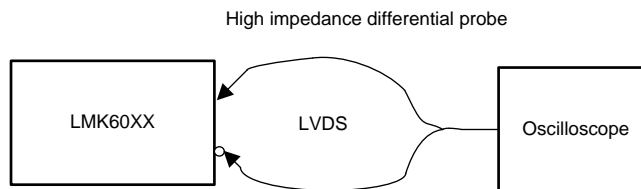


Figure 5. LVDS Output DC Configuration During Device Test

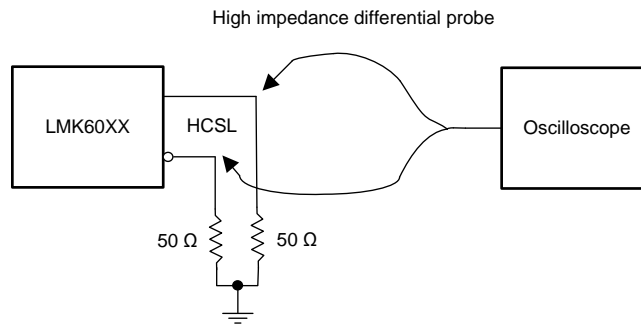


Figure 6. HCSL Output DC Configuration During Device Test

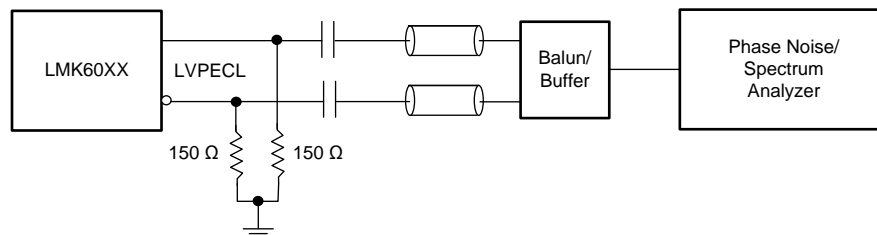


Figure 7. LVPECL Output AC Configuration During Device Test

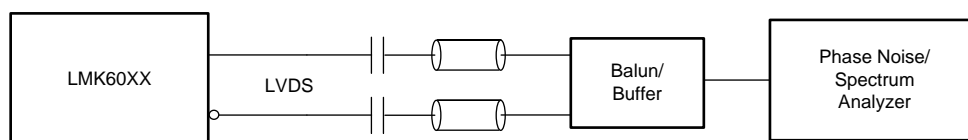


Figure 8. LVDS Output AC Configuration During Device Test

Device Output Configurations (continued)

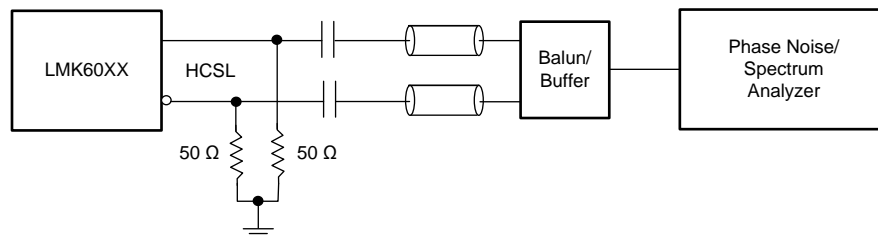


Figure 9. HCSL Output AC Configuration During Device Test

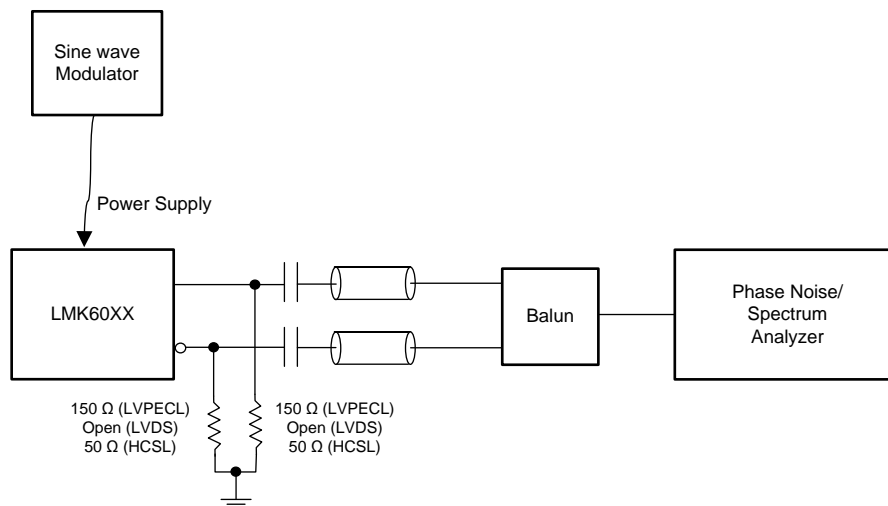


Figure 10. PSRR Test Setup

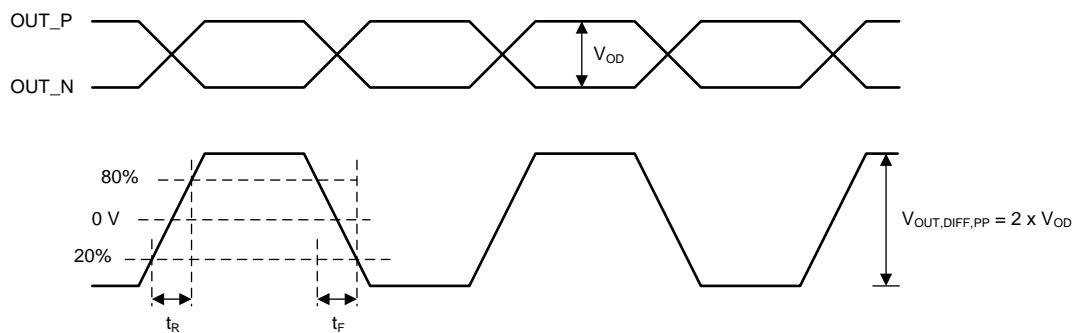


Figure 11. Differential Output Voltage and Rise/Fall Time

8 Power Supply Recommendations

For best electrical performance of LMK60XX, it is preferred to utilize a combination of 10 μF , 1 μF and 0.1 μF on its power supply bypass network. It is also recommended to utilize component side mounting of the power supply bypass capacitors and it is best to use 0201 or 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane. [Figure 12](#) shows the layout recommendation for power supply decoupling of LMK60XX.

9 Layout

9.1 Layout Guidelines

The following sections provides recommendations for board layout, solder reflow profile and power supply bypassing when using LMK60XX to ensure good thermal / electrical performance and overall signal integrity of entire system.

9.1.1 Ensuring Thermal Reliability

The LMK60XX is a high performance device. Therefore careful attention must be paid to device configuration and printed circuit board (PCB) layout with respect to power consumption. The ground pin needs to be connected to the ground plane of the PCB through three vias or more, as shown in [Figure 12](#), to maximize thermal dissipation out of the package.

[Equation 1](#) describes the relationship between the PCB temperature around the LMK60XX and its junction temperature.

$$T_B = T_J - \Psi_{JB} * P$$

where

- T_B : PCB temperature around the LMK60XX
- T_J : Junction temperature of LMK60XX
- Ψ_{JB} : Junction-to-board thermal resistance parameter of LMK60XX (37.7°C/W without airflow)
- P : On-chip power dissipation of LMK60XX

(1)

In order to ensure that the maximum junction temperature of LMK60XX is below 120°C, it can be calculated that the maximum PCB temperature without airflow should be at 90°C or below when the device is optimized for best performance resulting in maximum on-chip power dissipation of 0.68 W.

9.1.2 Best Practices for Signal Integrity

For best electrical performance and signal integrity of entire system with LMK60XX, it is recommended to route vias into decoupling capacitors and then into the LMK60XX. It is also recommended to increase the via count and width of the traces wherever possible. These steps ensure lowest impedance and shortest path for high frequency current flow. [Figure 12](#) shows the layout recommendation for LMK60XX.

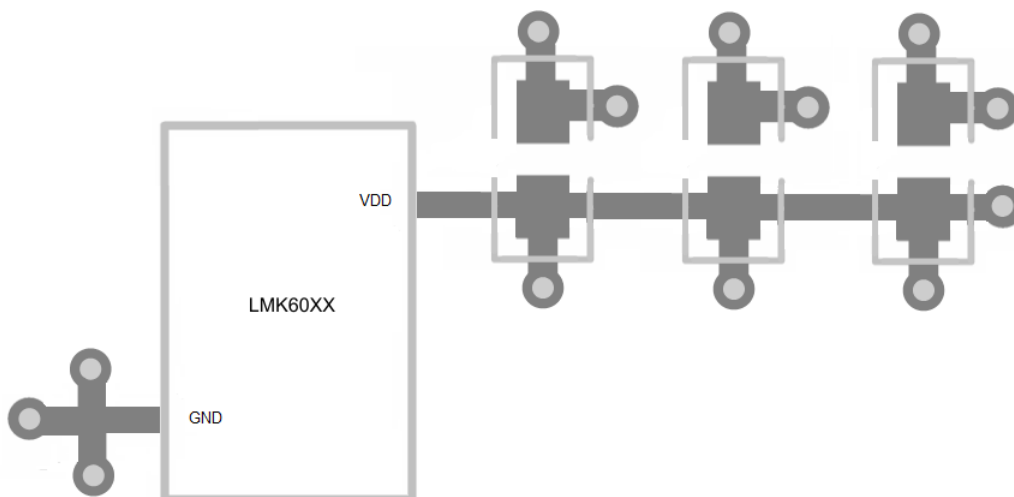


Figure 12. LMK60XX Layout Recommendation for Power Supply and Ground

Layout Guidelines (continued)

9.1.3 Recommended Solder Reflow Profile

It is recommended to follow the solder paste supplier's recommendations to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. It is preferable for the LMK60XX to be processed with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label. The exact temperature profile would depend on several factors including maximum peak temperature for the component as rated on the MSL label, Board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, as well solder manufactures recommended profile, and capability of the reflow equipment to as confirmed by the SMT assembly operation.

10 Device and Documentation Support

10.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMK60E2-150M00	Click here	Click here	Click here	Click here	Click here
LMK60E2-156M25	Click here	Click here	Click here	Click here	Click here
LMK60E0-156257	Click here	Click here	Click here	Click here	Click here

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

10.4 Trademarks

E2E is a trademark of Texas Instruments.
 All other trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK60E2-150M00SIAR	ACTIVE	QFM	SIA	6	2500	Green (RoHS & no Sb/Br)	Call TI NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 150M00	Samples
LMK60E2-150M00SIAT	ACTIVE	QFM	SIA	6	250	Green (RoHS & no Sb/Br)	Call TI NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 150M00	Samples
LMK60E2-156M25SIAR	PREVIEW	QFM	SIA	6	2500	Green (RoHS & no Sb/Br)	Call TI NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 156M25	
LMK60E2-156M25SIAT	PREVIEW	QFM	SIA	6	250	Green (RoHS & no Sb/Br)	Call TI NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 156M25	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

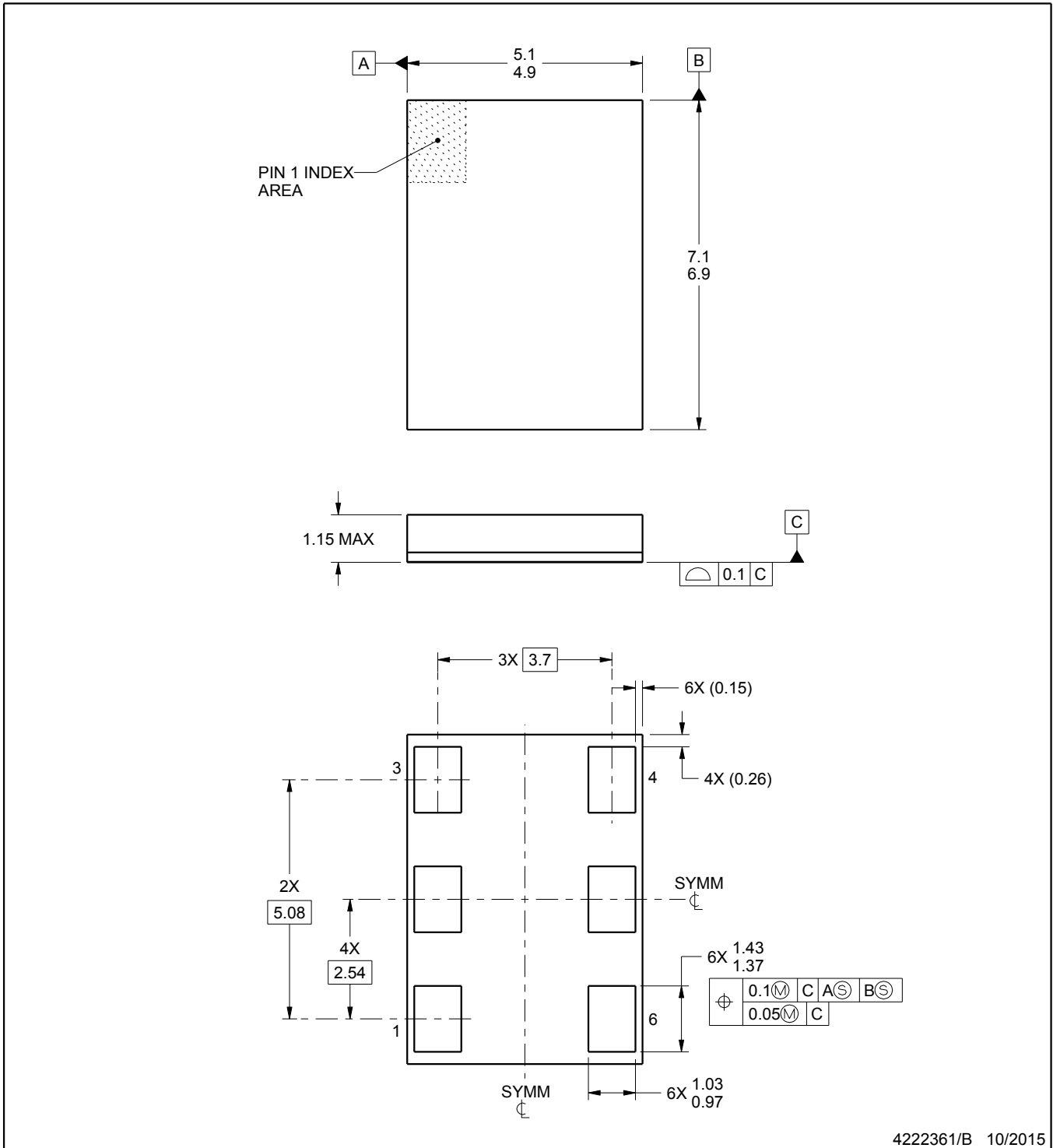
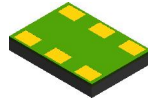

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK60E2-150M00SIAR	QFM	SIA	6	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60E2-150M00SIAT	QFM	SIA	6	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK60E2-150M00SIAR	QFM	SIA	6	2500	367.0	367.0	38.0
LMK60E2-150M00SIAT	QFM	SIA	6	250	213.0	191.0	55.0



4222361/B 10/2015

NOTES:

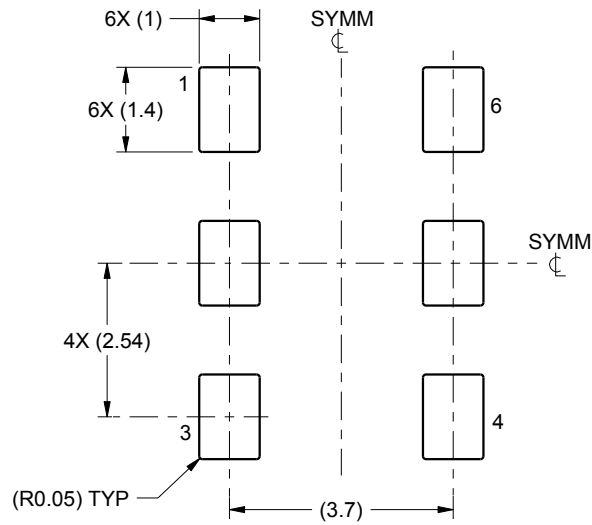
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

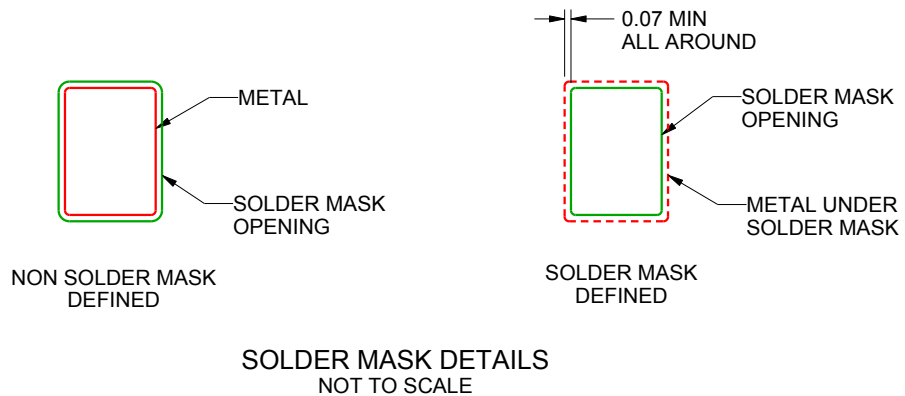
SIA0006A

QFM - 1.15 mm max height

QUAD FLAT MODULE



LAND PATTERN EXAMPLE
1:1 RATIO WITH PACKAGE SOLDER PADS
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

4222361/B 10/2015

NOTES: (continued)

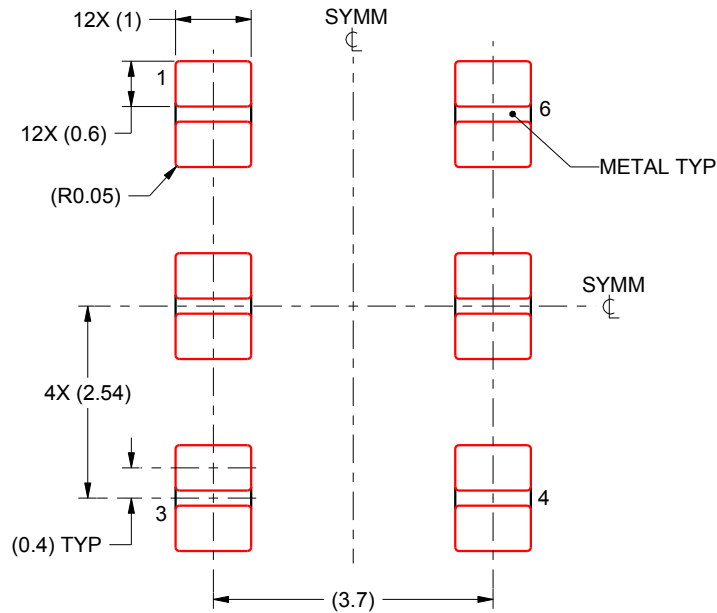
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

SIA0006A

QFM - 1.15 mm max height

QUAD FLAT MODULE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
PRINTED SOLDER COVERAGE BY AREA
ALL PADS: 86%
SCALE:10X

4222361/B 10/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com