



UT2N10

Power MOSFET

2 Amps, 100 Volts N-CHANNEL POWER MOSFET

DESCRIPTION

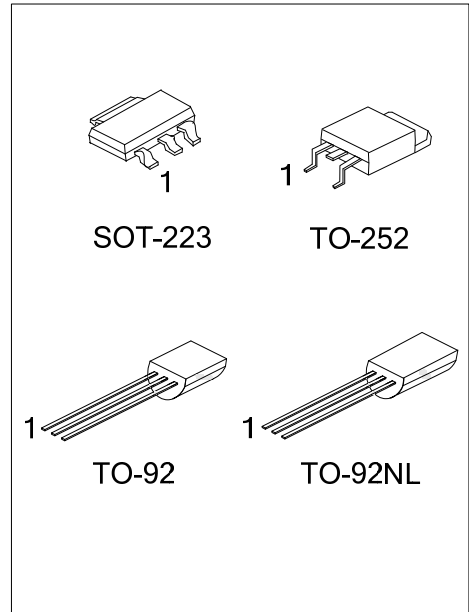
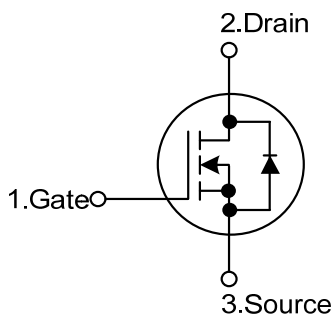
The UTC **UT2N10** is N-Channel enhancement mode silicon gate power FET. It uses a special gate oxide designed to provide full rated conductance at gate biases through 3V ~ 5V and facilitate true on-off power control directly from logic circuit supply voltages.

The UTC **UT2N10** is universally applied in logic level (5V) driving sources, such as automotive switching, solenoid drivers and programmable controllers.

FEATURES

- * $R_{DS(ON)} < 1.050\Omega @ V_{GS}=5V, I_D=2A$
- * Design Optimized for 5V Gate Drives
- * Can be Driven Directly from QMOS, NMOS, TTL Circuits
- * Compatible with Automotive Drive Requirements
- * SOA is Power Dissipation Limited
- * Nanosecond Switching Speeds
- * Linear Transfer Characteristics
- * High Input Impedance
- * Majority Carrier Device

SYMBOL



ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
-	UT2N10G-AA3-R	SOT-223	G	D	S	Tape Reel
UT2N10L-TN3-R	UT2N10G-TN3-R	TO-252	G	D	S	Tape Reel
UT2N10L-T92-B	UT2N10G-T92-B	TO-92	G	D	S	Tape Box
UT2N10L-T92-K	UT2N10G-T92-K	TO-92	G	D	S	Bulk
UT2N10L-T9N-B	UT2N10G-T9N-B	TO-92NL	G	D	S	Tape Box
UT2N10L-T9N-K	UT2N10G-T9N-K	TO-92NL	G	D	S	Bulk
UT2N10L-T9N-A-B	UT2N10G-T9N-A-B	TO-92NL	S	D	G	Tape Box
UT2N10L-T9N-A-K	UT2N10G-T9N-A-K	TO-92NL	S	D	G	Bulk

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UT2N10L-T9N-A-B</p> <p>(1) Packing Type (2) Pin Assignment (3) Package Type (4) Green Package</p>	<p>(1) R: Tape Reel, B: Tape Box, K: Bulk (2) refer to Pin Assignment (for TO-92NL) (3) AA3: SOT-223, TN3: TO-252, T92: TO-92 T9N: TO-92NL (4) L: Lead Free, G: Halogen Free and Lead Free</p>
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MARKING

SOT-223	TO-252
TO-92	TO-92NL

■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage (Note 1)	V_{DSS}	100	V
Gate-Source Voltage	V_{GSS}	± 10	V
Drain-Gate Voltage ($R_{GS}=1M\Omega$) (Note 1)	V_{DGR}	100	V
Drain Current	Continuous	I_D	2
	Pulsed (Note 3)	I_{DM}	5
Power Dissipation	SOT-223	P_D	1
	TO-252		25
	TO-92/ TO-92NL		3
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55~+150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$, unless otherwise specified)

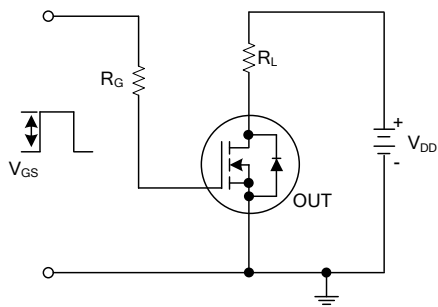
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	100			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}$, $V_{GS} = 0\text{V}$			1.0	μA
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$			25	
Gate- Source Leakage Current	I_{GSS}	Forward $V_{GS}=+10\text{V}$, $V_{DS}=0\text{V}$			+100	nA
		Reverse $V_{GS}=-10\text{V}$, $V_{DS}=0\text{V}$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.0		2.5	V
Drain-Source On Voltage (Note 2)	$V_{DS(ON)}$	$V_{GS}=5\text{V}$, $I_D=2\text{A}$			2.1	V
Static Drain-Source On-State Resistance (Note 2)	$R_{DS(ON)}$	$V_{GS}=5\text{V}$, $I_D=2\text{A}$			1.050	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$			200	pF
Output Capacitance	C_{OSS}				80	pF
Reverse Transfer Capacitance	C_{RSS}				35	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$				5	$^\circ\text{C/W}$
SWITCHING PARAMETERS						
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=50\text{V}$, $I_D=2\text{A}$, $R_G=6.25\Omega$, $R_L=25\Omega$, $V_{GS}=5\text{V}$		10	25	ns
Rise Time	t_R			15	45	ns
Turn-OFF Delay Time	$t_{D(OFF)}$			25	45	ns
Fall-Time	t_F			20	25	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Drain-Source Diode Forward Voltage (Note 2)	V_{SD}	$I_{SD}=2\text{A}$			1.4	V
Body Diode Reverse Recovery Time	t_{RR}	$I_{SD}=2\text{A}$, $dI_{SD}/dt=50\text{A}/\mu\text{s}$		100		ns

Notes: 1. $T_J = 25^\circ\text{C} \sim 125^\circ\text{C}$

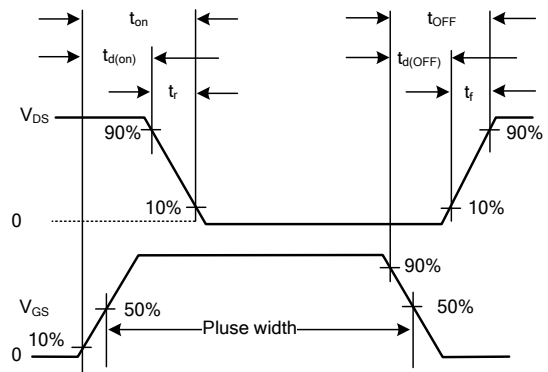
2. Pulse test: pulse width $\leq 300\text{ms}$, duty cycle $\leq 2\%$.

3. Repetitive rating: pulse width limited by maximum junction temperature

■ TEST CIRCUITS AND WAVEFORMS



Switching Time Test Circuit



Resistive Switching Waveforms

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