ISL68201

Single-Phase R4 Digital Hybrid PWM Controller with PMBus/SMBus/I^{2}C and PFM

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The ISL68201 is a single-phase, synchronous buck PWM controller featuring Intersil's proprietary R4™ Technology. It supports a wide 4.5V to 24V input voltage range and a wide 0.5V to 5.5V output range. Integrated LDOs provide controller bias voltage, allowing for single supply operation. The ISL68201 includes a PMBus/SMBus/I^{2}C interface for device configuration and telemetry (V_{IN}, V_{OUT}, I_{OUT}, and temperature) and fault reporting.

Intersil's proprietary R4 control scheme has extremely fast transient performance, accurately regulated frequency control and all internal compensation. An efficiency enhancing PFM mode can be enabled to greatly improve light-load efficiency. The ISL68201's serial bus allows for easy R4 loop optimization, resulting in fast transient performance over a wide range of applications, including all ceramic output filters.

The ISL68201 has four 8-bit configuration pins, which provide very flexible configuration options (frequency, V_{OUT}, R4 gain, etc.) without the need for built-in NVM memory. This results in a design flow that closely matches traditional analog controllers, while still offering the design flexibility and feature set of a digital PMBus/SMBus/I^{2}C interface. The ISL68201 also features remote voltage sensing and completely eliminates any potential difference between remote and local grounds. This improves regulation and protection accuracy. A precision enable input is available to coordinate the start-up of the ISL68201 with other voltage rails, especially useful for power sequencing.

Applications

- High efficiency and high density POL digital power
- FPGA, ASIC, and memory supplies
- Data center: servers, storage systems
- Wired infrastructure: routers, switches, and optical networking
- Wireless infrastructure: base station

Related Literature

- ISL68201 product page

Features

- Intersil's proprietary R4 Technology
  - Linear control loop for optimal transient response
  - Variable frequency and duty cycle control during load transient for fastest possible response
  - Inherent voltage feed-forward for wide range input
- Input voltage range: 4.5V to 24V
- Output voltage range: 0.5V to 5.5V
- ±0.5% DAC accuracy with remote sense
- Support all ceramic solutions
- Integrated LDOs for single input rail solution
- SMBus/PMBus/I^{2}C compatible, up to 1.25MHz
- 256 boot-up voltage levels with a configuration pin
- Eight switching frequency options from 300kHz to 1.5MHz
- PFM operation option, compatible with ISL99140 for improved light-load efficiency
- Start-up into precharged load
- Precision enable input to set higher input UVLO and power sequence as well as fault reset
- Power-good monitor for soft-start and fault detection
- Comprehensive fault protection for high system reliability
  - Over-temperature protection
  - Output overcurrent and short-circuit protection
  - Output overvoltage and undervoltage protection
  - Open remote sense protection
- Compatible with 5V or 3.3V PWM input DrMOS or Smart Power Stage (SPS)
- Compatible with Intersil's PowerNavigator software

TABLE 1. SINGLE-PHASE R4 DIGITAL HYBRID PWM CONTROLLER OPTIONS

PART NUMBER	INTEGRATED DRIVER	PWM OUTPUT	PMBus/SMBus/I^{2}C INTERFACE	COMPATIBLE DEVICES
ISL68200	Yes	No	Yes	Discrete MOSFETs or Dual Channel MOSFETs
ISL68201	No	Yes	Yes	Intersil Power Stages: ISL99140, ISL99227, ISL99125B, ISL99135B Intersil Drivers: ISL6596, ISL6609, ISL6627, ISL6622, ISL6208

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Typical Applications Circuits

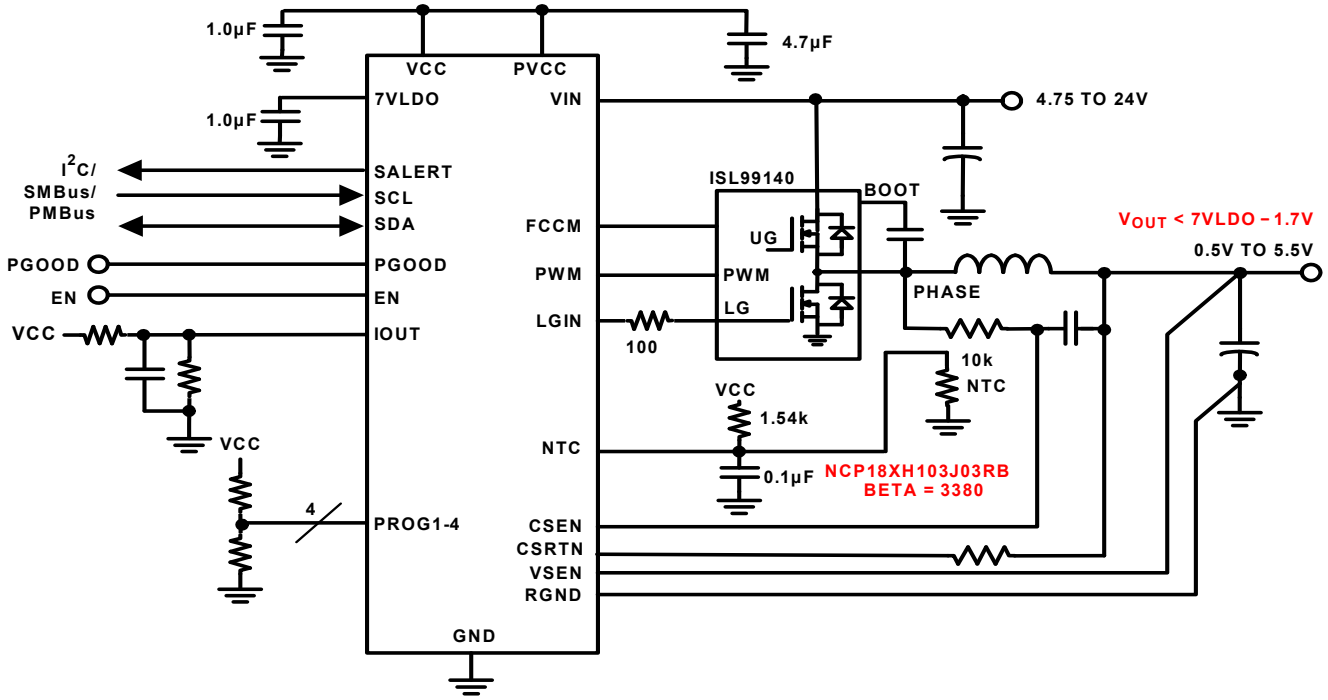


FIGURE 1. WIDE RANGE INPUT AND OUTPUT APPLICATIONS

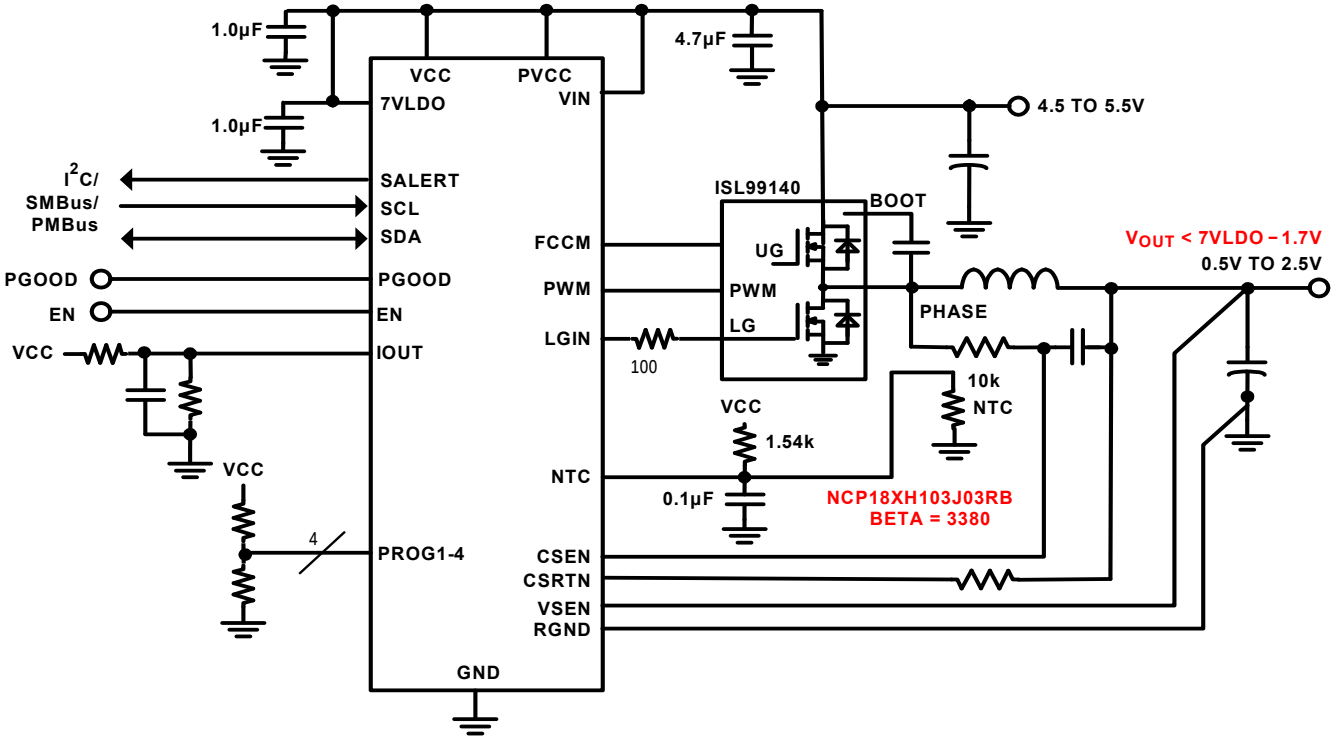


FIGURE 2. 5V INPUT APPLICATION

Block Diagram

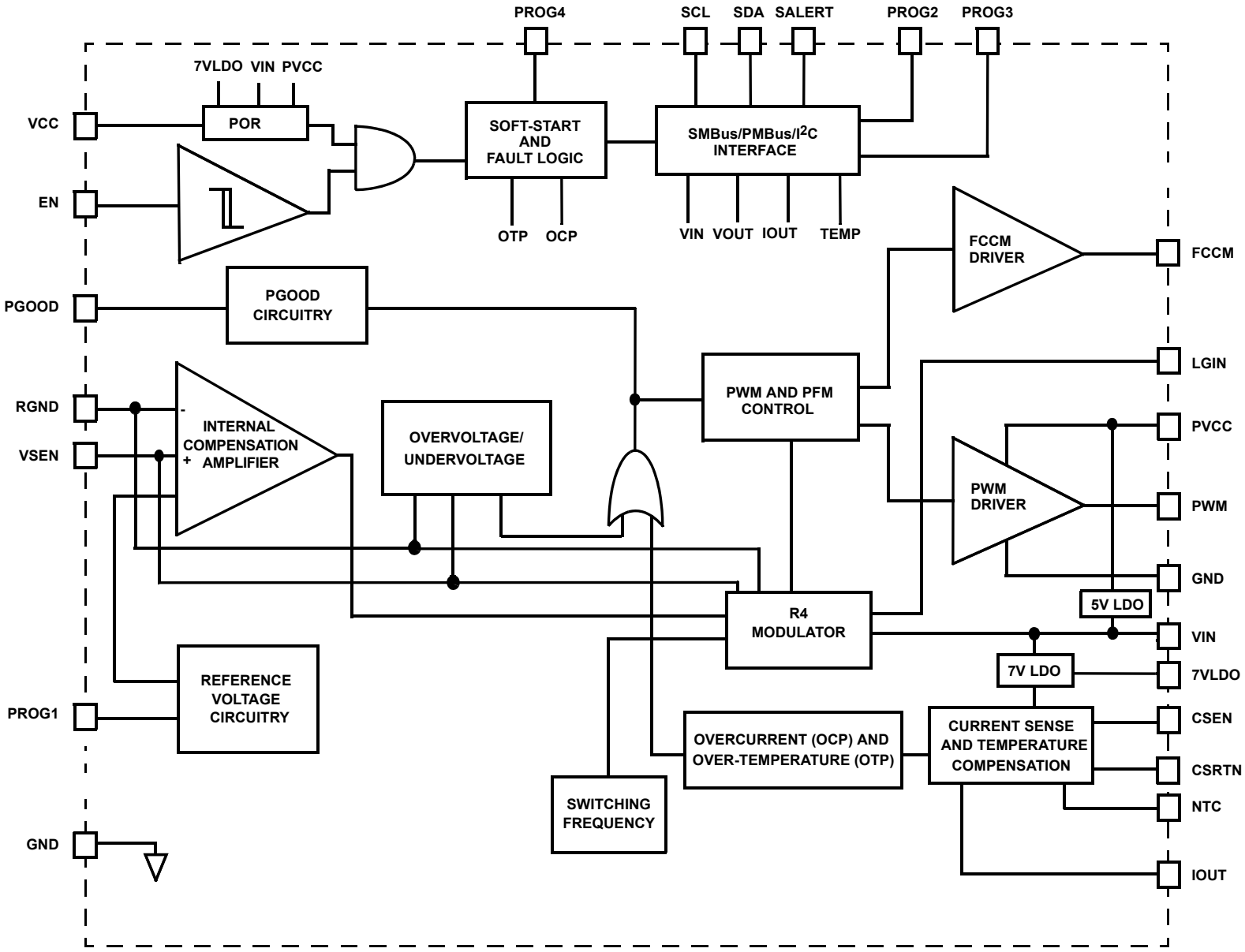


FIGURE 3. ISL68201 SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

Ordering Information

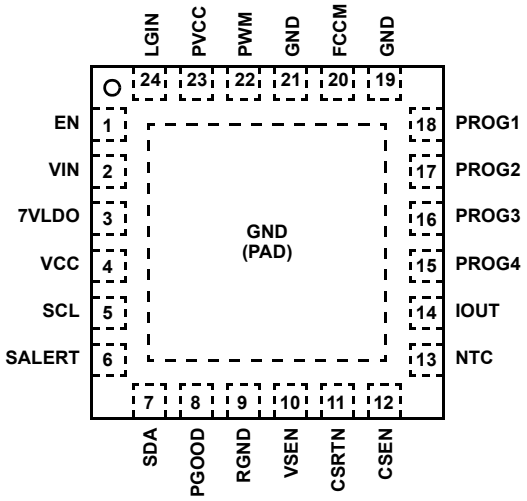
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL68201IRZ	ISL 68201I	-40 to +85	24 Ld 4x4 QFN	L24.4x4C
ISL68201-99125DEM01Z	16A Demo Board with On-Board Transient			
ISL68201-99135DEM01Z	20A Demo Board with On-Board Transient			
ISL68201-99140DEM01Z	35A Demo Board with On-Board Transient			

NOTES:

1. Add “-T” suffix for 6k unit, “-T7A” suffix for 250 unit or “-TK” for 1k unit for tape and reel options. Refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the product information page for ISL68201. For more information on MSL, see TB363.

Pin Configuration

ISL68201
(24 LD 4X4 QFN)
TOP VIEW



Functional Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	EN	Precision enable input. Pulling EN above the rising threshold voltage initiates the soft-start sequence, while pulling EN below the failing threshold voltage suspends the Voltage Regulator (VR) operation.
2	VIN	Input voltage pin for R4 loop and LDOs (5V and 7V). Place a high quality low ESR ceramic capacitor (1.0µF, X7R) in close proximity to the pin. External series resistor is not advised.
3	7VLDO	7V LDO from VIN is used to bias current sensing amplifier. Place a high quality low ESR ceramic capacitor (1.0µF, X7R, 10V+) in close proximity to the pin.
4	VCC	Logic bias supply that should be connected to PVCC rail externally. Place a high quality low ESR ceramic capacitor (1µF, X7R) from this pin to GND.
5	SCL	Synchronous clock signal input of SMBus/PMBus/I^2C.
6	SALERT	Output pin for transferring the active low signal driven asynchronously from the VR controller to SMBus/PMBus.
7	SDA	I/O pin for transferring data signals between SMBus/PMBus/I^2C host and VR controller.
8	PGOOD	Power-good open-drain indicator output.
9	RGND	This pin monitors the negative rail of regulator output. Connect to ground at point of regulation.

Functional Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
10	VSEN	This pin monitors the positive rail of regulator output. Connect to point of regulation.
11	CSRTN	This pin monitors the negative flow of output current with a series resistor and for overcurrent protection and telemetry. The series resistor sets the current gain and should be within 40Ω and 3.5kΩ.
12	CSEN	This pin monitors the positive flow of output current for overcurrent protection and telemetry.
13	NTC	Input pin for the temperature measurement. Connect this pin through an NTC thermistor (10kΩ, β ~ 3380) and a decoupling capacitor (~0.1µF) to GND and a resistor (1.54kΩ) to VCC of the controller. The voltage at this pin is inversely proportional to the VR temperature.
14	IOUT	Output current monitor pin. An external resistor sets the gain and an external capacitor provides the averaging function; an external pull-up resistor to VCC is recommended to calibrate the no load offset. See "I_{OUT} Calibration" on page 19.
15	PROG4	Programming pin for Modulator (R4) RR impedance and output slew rate during Soft-Start (SS) and Dynamic VID (DVID). It also sets AV gain multiplier to 1x or 2x and determines the AV gain on PROG3.
16	PROG3	Programming pin for ultrasonic PFM operation, fault behavior, switching frequency, and R4 (AV) control loop gain.
17	PROG2	Programming pin for PWM/PFM mode, temperature compensation, and serial bus (SMBus/PMBus/I^2C) address.
18	PROG1	Programming pin for boot-up voltage.
19, 21	GND	Ground pin, connect directly to system ground plane.
20	FCCM	Output signal low to work with DrMOS ISL99140 for diode emulation in PFM mode; signal high for PWM mode.
22	PWM	PWM output and is compatible with 3.3V or 5V PWM input external driver, DrMOS, or Smart Power Stage.
23	PVCC	Output of the 5V LDO and input for the LGATE and UGATE MOSFET driver circuits. Place a high quality low ESR ceramic capacitors (4.7µF or higher, X7R) in close proximity to the pin.
24	LGIN	Low-side gate signal input to complete the internal FLL loop. A 100Ω series impedance from low-side gate drive signal to this pin is required.
PAD	GND	Return of logic bias supply VCC. Connect directly to system ground plane with at least four vias.

Absolute Maximum Ratings

VCC, PVCC, VSEN. . . . . -0.3V to +7.0V
Input Voltage, VIN . . . . . +27V
7VLDO . . . . . -0.3V to GND, 7.75V
All Other Pins . . . . . -0.3V to GND, VCC + 0.3V
ESD Rating
Human Body Model (Tested per JS-001-2010). 2.5kV
Machine Model (Tested per JESD22-A115C) 200V
Charge Device Model (Tested per JS-002-2014) 1kV
Latch-Up (Tested per JESD78D, Class 2, Level A). . . . ±100mA at +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld QFN (Notes 4, 5)	39	2.5

Junction Temperature Range . . . . . -55°C to +150°C
Storage Temperature . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to +85°C
Wide Range Input Voltage, V_{IN}, Figure 1. . . . . 4.75V to 24V
5V Application Input Voltage, V_{IN}, V_{CC}, PVCC, Figure 2 . . . . . 4.5V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

All typical specifications T_A = +25°C, V_{CC} = 5V. **Boldface limits apply across the operating temperature range, -40°C to +85°C, unless otherwise stated.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
VCC AND PVCC						
VCC Input Bias Current	I_{VCC}	EN = 5V, V_{CC} = 5V, f_{SW} = 500kHz, DAC = 1V		14	**16.5**	mA
		EN = 0V, V_{CC} = 5V		14	**16.5**	mA
PVCC Input Bias Current	I_{PVCC}	EN = 5V, V_{CC} = 5V, f_{SW} = 500kHz, DAC = 1V		2		mA
		EN = 0V, V_{CC} = 5V			**1.0**	mA
VCC AND VIN POR THRESHOLD						
VCC, PVCC Rising POR Threshold Voltage				4.2	**4.35**	V
VCC, PVCC Falling POR Threshold Voltage			**3.80**	3.95	**4.15**	V
V_{IN}, 7VLDO Rising POR Threshold Voltage				4.2	**4.35**	V
V_{IN}, 7VLDO Falling POR Threshold Voltage			**3.80**	3.95	**4.15**	V
ENABLE INPUT						
EN High Threshold Voltage	V_{ENTHR}		**0.81**	0.84	**0.87**	V
EN Low Threshold Voltage	V_{ENTHF}		**0.71**	0.76	**0.81**	V
DAC ACCURACY						
DAC Accuracy (T_A = 0°C to +85°C)		2.5V < DAC ≤ 5.5V	**-0.5**		**0.5**	%
		1.6V < DAC ≤ 2.5V	**-0.75**		**0.75**	%
		1.2V < DAC ≤ 1.6V	**-10**		**10**	mV
		0.5V ≤ DAC ≤ 1.2V	**-8**		**8**	mV
DAC Accuracy (T_A = -45°C to +85°C)		2.5V < DAC ≤ 5.5V	**-0.75**		**0.75**	%
		1.6V < DAC ≤ 2.5V	**-1.0**		**1.0**	%
		1.2V < DAC ≤ 1.6V	**-11**		**11**	mV
		0.5V ≤ DAC ≤ 1.2V	**-9**		**9**	mV
CHANNEL FREQUENCY						
300kHz Configuration		PWM mode	**260**	300	**335**	kHz
400kHz Configuration		PWM mode	**345**	400	**450**	kHz

Electrical Specifications All typical specifications T_A = +25°C, V_{CC} = 5V. **Boldface limits apply across the operating temperature range, -40°C to +85°C, unless otherwise stated. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
500kHz Configuration		PWM mode	**435**	500	**562**	kHz
600kHz Configuration		PWM mode	**510**	600	**670**	kHz
700kHz Configuration		PWM mode	**610**	700	**790**	kHz
850kHz Configuration		PWM mode	**730**	850	**950**	kHz
1000kHz Configuration		PWM mode	**865**	1000	**1120**	kHz
1500kHz Configuration		PWM mode	**1320**	1500	**1660**	kHz
SOFT-START AND DYNAMIC VID						
Soft-Start and DVID Slew Rate			**0.0616**	0.078	**0.096**	mV/µs
			0.13	0.157	**0.18**	mV/µs
			0.25	0.315	**0.37**	mV/µs
			0.53	0.625	**0.70**	mV/µs
			1.05	1.25	**1.40**	mV/µs
			2.10	2.50	**2.80**	mV/µs
			4.20	5.00	**5.60**	mV/µs
			8.60	10.0	**10.9**	mV/µs
Soft-Start Delay from Enable High		Excluding 5.5ms POR timeout. See Figures 21 and 22	**140**	200	**260**	µs
REMOTE SENSE						
Bias Current of VSEN and RGND Pins					**250**	µA
Maximum Differential Input Voltage			**6.0**			V
POWER-GOOD						
PGOOD Pull-Down Impedance	R_{PG}	PGOOD = 5mA sink		10	**50**	Ω
PGOOD Leakage Current	I_{PG}	PGOOD = 5V			**1.0**	µA
LDOs						
5V LDO Regulation		V_{IN} = 12V, load = 50mA	**4.85**	5.00	**5.15**	V
5V Dropout		V_{IN} = 4.75V, load = 50mA	**4.45**			V
5V LDO Current Capability			**125**			mA
7V LDO Regulation		250µA load	**7.2**	7.4	**7.5**	V
7V Dropout		V_{IN} = 4.75V, 250µA load	**4.50**			V
7V LDO Current Capability		Not recommended for external use	**2**			mA
CURRENT SENSE						
Average OCP Trip Level	I_{OC_TRIP}		**82**	100	**123**	µA
Short-Circuit Protection Threshold				130		% I_{OCP}
Sensed Current Tolerance			**74**	78	**83**	µA
Sensed Current Tolerance			**35**	38	**42**	µA
Maximum Common-Mode Input Voltage		7VLDO = 7.4V	**5.7**			V
		VCC = PVCC = 7VLDO = 4.5V	**2.8**			V

Electrical Specifications All typical specifications T_A = +25°C, V_{CC} = 5V. **Boldface limits apply across the operating temperature range, -40°C to +85°C, unless otherwise stated. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
FAULT PROTECTION						
UVP Threshold Voltage		Latch	**68**	74	**80**	% DAC
Start-Up OVP Threshold Voltage		0V ≤ V_{BOOT} ≤ 1.08V	**1.10**	1.15	**1.25**	V
		1.08V < V_{BOOT} ≤ 1.55V	**1.58**	1.65	**1.75**	V
		1.55V < V_{BOOT} ≤ 1.85V	**1.88**	1.95	**2.05**	V
		1.85V < V_{BOOT} ≤ 2.08V	**2.09**	2.15	**2.25**	V
		2.08V < V_{BOOT} ≤ 2.53V	**2.56**	2.65	**2.75**	V
		2.53V < V_{BOOT} ≤ 3.33V	**3.36**	3.45	**3.6**	V
		3.33V < V_{BOOT} ≤ 5.5V	**5.52**	5.65	**5.85**	V
Start-Up OVP Hysteresis				100		mV
OVP Rising Threshold Voltage	V_{OVRTH}	0.5 ≤ DAC ≤ 5.5	**114**	120	**127**	% DAC
OVP Falling Threshold Voltage	V_{OVFTH}	0.5 ≤ DAC ≤ 5.5	**96**	100	**108**	% DAC
Over-Temperature Shutdown Threshold		READ_TEMP = 72h	**20**	22.31	**26**	% VCC
Over-Temperature Shutdown Reset Threshold		READ_TEMP = 8Eh	**25**	27.79	**30**	% VCC
SMBus/PMBus/I^2C						
Signal Input Low Voltage					**1**	V
Signal Input High Voltage			**1.6**			V
Signal Output Low Voltage		4mA pull-up current			**0.4**	V
DATE, ALERT # Pull-Down Impedance				11	**50**	Ω
CLOCK Maximum Speed			**1.25**			MHz
CLOCK Minimum Speed					**0.05**	MHz
Telemetry Update Rate				108		µs
Timeout			**25**	30	**35**	ms
PMBus Accessible Timeout from All Rails' POR		See Figure 21		5.5	**6.5**	ms

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Operation

The following sections provide a detailed description of the ISL68201 operation.

IC Supplies

The ISL68201 has four bias pins: VIN, 7VLDO, PVCC, and VCC. The PVCC and 7VLDO voltage rails are 5V LDO and 7.4V LDO supplied by VIN, respectively, while the VCC pin needs to connect to the PVCC rail externally to be biased. For 5V input applications, all these pins should be tied together and biased by a 5V supply. Because the VIN pin voltage information is used by the R4 Modulator loop, the user CANNOT bias VIN with a series resistor. In addition, the VIN pin CANNOT be biased independently from other rails.

Enable and Disable

The IC is disabled until the 7VLDO, PVCC, VCC, VIN, and EN pins increase above their respective rising threshold voltages and the typical 5.5ms timeout (worst case = 6.5ms) expires, as shown in Figures 21 and 22 on page 22. The controller will become disabled when the 7VLDO, PVCC, VCC, VIN, or EN pins drop below their respective falling POR threshold voltages.

The precision threshold EN pin allows the user to set a precision input UVLO level with an external resistor divider, as shown in Figure 4. For 5V input applications or wide range input applications, the EN pin can directly connect to VCC, as shown in Figure 5. If an external enable control signal is available and is an open-drain signal, a pull-up impedance (100k or higher) can be used.

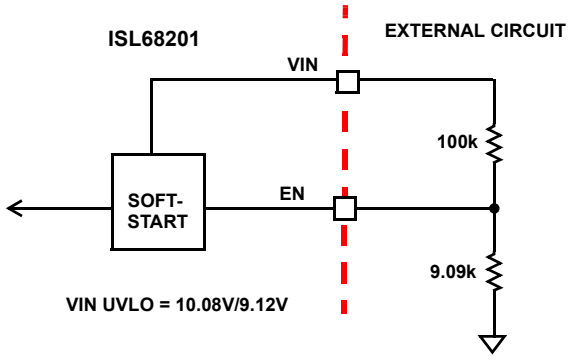


FIGURE 4. INPUT UVP CONFIGURATION

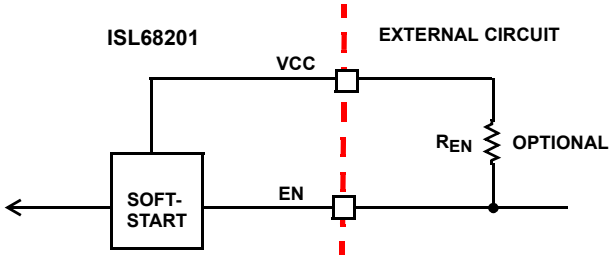


FIGURE 5. 5V INPUT OR WIDE RANGE INPUT CONFIGURATION

In addition, based on the ON_OFF_CONFIG [02h] setting, the IC can be enabled or disabled by the serial bus command "OPERATION [01h]" and/or EN pin. See Table 11 on page 25 for more details.

Resistor Reader (Patented)

The ISL68201 offers four programming pins to customize their regulator specifications. The details of these pins are summarized in Table 2, followed by the detailed description of resistor reader operation.

TABLE 2. DEFINITION OF PROG PINS

PIN	BIT	NAME	DESCRIPTION
PROG1	[7:0]	BOOT-UP VOLTAGE	Set output boot-up voltage, 256 different options: 0, 0.5V to 5.5V (see Table 7)
PROG2	[7:7]	PWM/PFM	Enables PFM mode or forced PWM.
	[6:5]	Temperature Compensation	Adjust NTC temperature compensation: OFF, +5, +15, +30°C.
	[4:0]	ADDR	Set serial bus 32 different addresses (see Table 10).
PROG3	[7:7]	USPFM	Ultrasonic (25kHz Clamp) PFM enable
	[6:6]	Fault Behavior	OCP fault behavior: Latch, Infinite 9ms retry
	[5:3]	f_{SW}	Set switching frequency (f_{SW}).
	[2:0]	R4 Gain	Set error amplifier gain (AV).
PROG4	[7:5]	RAMP_RATE	Set soft-start and DVID ramp rate.
	[4:3]	RR	Select RR impedance for R4 loop.
	[2:2]	AVMLTI	Select AV gain multiplier (1x or 2x)
	[1:0]	Not Used	

Intersil has developed a high resolution ADC using a patented technique with a simple 1%, 100ppm/K or better temperature coefficient resistor divider. The same type of resistors are preferred so that it has similar change over temperature. In addition, the divider is compared to the internal divider off V_{CC} and GND nodes and therefore must refer to VCC and GND pins, not through any RC decoupling network.

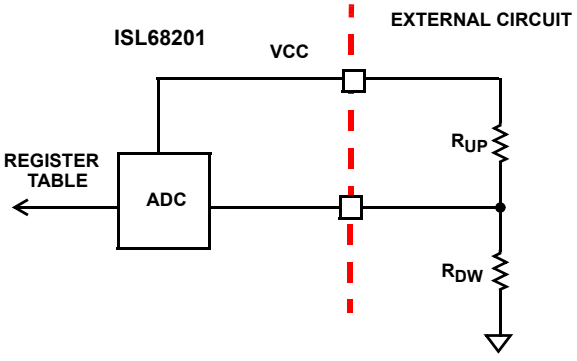


FIGURE 6. SIMPLIFIED RESISTOR DIVIDER ADC

The R_{UP} and R_{DW} values for a particular parameter set can be found using the Power Navigator GUI. Data for corresponding registers can be read out using the serial PMBus command (DC to DF). **Note**: The case of 10kΩ R_{UP} or R_{DW} is the same as 0kΩ R_{UP} or R_{DW}.

TABLE 3. PROG 1 RESISTOR READER EXAMPLE

PROG1 (DC)	R_{UP} (kΩ)	R_{DW} (kΩ)	V_{OUT} (V)
00h	Open	0	0.797
20h	Open	21.5	0.852
40h	Open	34.8	0.898
60h	Open	52.3	0.953
80h	Open	75	1.000
A0h	Open	105	1.047
C0h	Open	147	1.102
E0h	Open	499	1.203
1Fh	0	Open	1.352
3Fh	21.5	Open	1.500
5Fh	34.8	Open	1.797
7Fh	52.3	Open	2.500
9Fh	75	Open	3.000
BFh	105	Open	3.297
DFh	147	Open	5.000
FFh	499	Open	0.000

TABLE 4. PROG 2 RESISTOR READER EXAMPLE

PROG2 (DD)	R_{UP} (kΩ)	R_{DW} (kΩ)	PWM/PFM	TEMP COMP	PM_ADDR (7-BIT)
00h	Open	0	Enabled	30	60h
20h	Open	21.5	Enabled	15	60h
40h	Open	34.8	Enabled	5	60h
60h	Open	52.3	Enabled	OFF	60h
80h	Open	75	Disabled	30	60h
A0h	Open	105	Disabled	15	60h
C0h	Open	147	Disabled	5	60h
E0h	Open	499	Disabled	OFF	60h
1Fh	0	Open	Enabled	30	7F
3Fh	21.5	Open	Enabled	15	7F
5Fh	34.8	Open	Enabled	5	7F
7Fh	52.3	Open	Enabled	OFF	7F
9Fh	75	Open	Disabled	30	7F
BFh	105	Open	Disabled	15	7F
DFh	147	Open	Disabled	5	7F
FFh	499	Open	Disabled	OFF	7F

TABLE 5. PROG 3 RESISTOR READER EXAMPLE

PROG3 (DE)	R_{UP} (kΩ)	R_{DW} (kΩ)	ULTRASONIC PFM	FAULT BEHAVIOR	f_{SW} (kHz)	R4 GAIN	
						1x	2x
00h	Open	0	Disabled	Retry	300	42	84
20h	Open	21.5	Disabled	Retry	700	42	84
40h	Open	34.8	Disabled	Latch	300	42	84
60h	Open	52.3	Disabled	Latch	700	42	84
80h	Open	75	Enabled	Retry	300	42	84
A0h	Open	105	Enabled	Retry	700	42	84
C0h	Open	147	Enabled	Latch	300	42	84
E0h	Open	499	Enabled	Latch	700	42	84
1Fh	0	Open	Disabled	Retry	600	1	2
3Fh	21.5	Open	Disabled	Retry	1500	1	2
5Fh	34.8	Open	Disabled	Latch	600	1	2
7Fh	52.3	Open	Disabled	Latch	1500	1	2
9Fh	75	Open	Enabled	Retry	600	1	2
BFh	105	Open	Enabled	Retry	1500	1	2
DFh	147	Open	Enabled	Latch	600	1	2
FFh	499	Open	Enabled	Latch	1500	1	2

TABLE 6. PROG 4 RESISTOR READER EXAMPLE

PROG4 (DF	R_{UP} (kΩ)	R_{DW} (kΩ)	SS RATE (mV/µs)	RR (kΩ)	AVMLTI
00h	Open	0	1.25	200	1x
20h	Open	21.5	2.5	200	1x
40h	Open	34.8	5	200	1x
60h	Open	52.3	10	200	1x
80h	Open	75	0.078	200	1x
A0h	Open	105	0.157	200	1x
C0h	Open	147	0.315	200	1x
E0h	Open	499	0.625	200	1x
1Fh	0	Open	1.25	800	2x
3Fh	21.5	Open	2.5	800	2x
5Fh	34.8	Open	5	800	2x
7Fh	52.3	Open	10	800	2x
9Fh	75	Open	0.078	800	2x
BFh	105	Open	0.157	800	2x
DFh	147	Open	0.315	800	2x
FFh	499	Open	0.625	800	2x

Soft-Start

The ISL68201-based regulator has four periods during soft-start, as shown in Figure 7 on page 12. After a 5.5ms timeout (worst case = 6.5ms) of bias supplies, as shown in Figures 21 and 22 on page 22, when the EN pin reaches above its enable threshold, the controller begins the first soft-start ramp after a fixed soft-start delay period t_{D1}. The output voltage reaches the boot-up voltage (V_{BOOT}) at a fixed slew rate in period t_{D2}. Then, the controller will regulate the output voltage at V_{BOOT} for another period t_{D3} until SMBus/PMBus/ I^2C sends a new V_{OUT} command. If the V_{OUT} command is valid, the ISL68201 will initiate the ramp until the voltage reaches the new VOUT_COMMAND voltage in period t_{D4}. The soft-start time is the sum of the four periods, as shown in Equation 1.

$$t_{SS} = t_{D1} + t_{D2} + t_{D3} + t_{D4} \quad \text{(EQ. 1)}$$

t_{D1} is a fixed delay with the typical value as 200µs. t_{D3} is determined by the time to obtain a new valid VOUT_COMMAND voltage from SMBus/PMBus/I^2C bus. If the VOUT_COMMAND is valid before the output reaches the boot-up voltage, the output will turn around to respond to the new VOUT_COMMAND code.

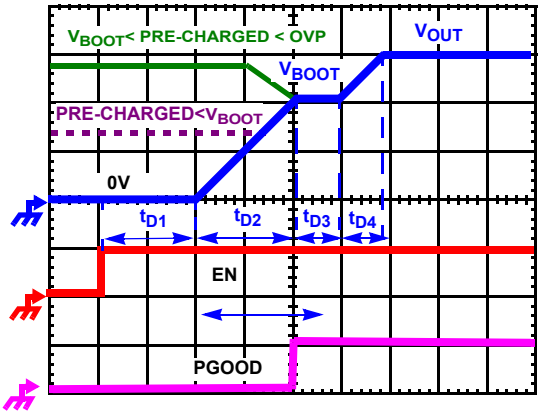


FIGURE 7. SOFT-START WAVEFORMS

During t_{D2} and t_{D4}, the ISL68201 digitally controls the DAC voltage change. The ramp time t_{D2} and t_{D4} can be calculated based on Equations 2 and 3, after the slew rate is set by the PROG4 pin.

$$t_{D2} = \frac{V_{BOOT}}{RAMP_RATE}(\mu s) \quad \text{(EQ. 2)}$$

$$t_{D4} = \frac{V_{OUT} - V_{BOOT}}{RAMP_RATE}(\mu s) \quad \text{(EQ. 3)}$$

The ISL68201 supports precharged start-up, which initiates the first PWM pulse until the internal reference (DAC) reaches the precharged level at RAMP_RATE, programmed by PROG4 or D5[2:0]. When the precharged level is below V_{BOOT}, the output walks up to the V_{BOOT} at RAMP_RATE and releases PGOOD at $t_{D1} + t_{D2}$. When the precharged output is above V_{BOOT} but below OVP, it walks down to V_{BOOT} at RAMP_RATE and then releases PGOOD at $t_{D1} + t_{D2}$, in which t_{D2} is defined in Equation 4 and longer than a normal start-up.

The ISL68201 supports precharged load start-up to the maximum V_{OUT} of 5.5V with sufficient boot capacitor charge. For

$$t_{D2} = \frac{V_{PRECHARGED}}{RAMP_RATE} + \frac{V_{PRECHARGED} - V_{BOOT}}{RAMP_RATE}(\mu s) \quad \text{(EQ. 4)}$$

an extended precharged load, the boot capacitor will be discharged to "PVCC - V_{OUT} - V_D" by the high-side drive circuits' standby current. For instance, an extended 4V precharged load, the boot capacitor will reduce to a less-than-1V boot capacitor voltage, which is insufficient to power up the VR; in this case, it is recommended to let the output drop below 2.5V with an external bleed resistor before issuing another soft-start command.

Boot-Up Voltage Programming

An 8-bit pin PROG1 is dedicated for the boot-up voltage programmability, which offers 256 options 0V and 0.5V to 5.5V, as in Table 7. The most popular boot-up voltage levels are placed on the tie-low spots (0h, 20h, 40h, 60h, 80h, A0h, C0h, E0h) and the tie-high spots (1Fh, 3Fh, 5Fh, 7Fh, 9Fh, BFh, DFh, FFh) for easy programming, as summarized in Table 3. 0V boot-up voltage is considered as "OFF," the driver will be in tri-state and the internal DAC will set to 0V.

In addition, if the VOUT_COMMAND (21h) is executed successfully 5.5ms (typically, worst 6.5ms) after VCC POR and before Enable, it will override the boot-up voltage set by the PROG1 pin.

TABLE 7. PROG1 8-BIT (BOOT-UP VOLTAGE)

BINARY CODE	HEX CODE	V_{BOOT} (V)	VOUT COMMAND CODE (HEX)	DELTA FROM PREVIOUS CODE (mV)
00000000	0	0.7969	66	
00000001	1	0.5000	40	
00000010	2	0.5078	41	7.8125
00000011	3	0.5156	42	7.8125
00000100	4	0.5234	43	7.8125
00000101	5	0.5313	44	7.8125
00000110	6	0.5391	45	7.8125
00000111	7	0.5469	46	7.8125
00001000	8	0.5547	47	7.8125
00001001	9	0.5625	48	7.8125
00001010	A	0.5703	49	7.8125
00001011	B	0.5781	4A	7.8125
00001100	C	0.5859	4B	7.8125
00001101	D	0.5938	4C	7.8125
00001110	E	0.6016	4D	7.8125
00001111	F	0.6094	4E	7.8125
00010000	10	0.6172	4F	7.8125
00010001	11	0.6250	50	7.8125
00010010	12	0.6328	51	7.8125
00010011	13	0.6406	52	7.8125
00010100	14	0.6484	53	7.8125

TABLE 7. PROG1 8-BIT (BOOT-UP VOLTAGE) (Continued)

BINARY CODE	HEX CODE	V_{BOOT} (V)	VOUT COMMAND CODE (HEX)	DELTA FROM PREVIOUS CODE (mV)
00010101	15	0.6563	54	7.8125
00010110	16	0.6641	55	7.8125
00010111	17	0.6719	56	7.8125
00011000	18	0.6797	57	7.8125
00011001	19	0.6875	58	7.8125
00011010	1A	0.6953	59	7.8125
00011011	1B	0.7031	5A	7.8125
00011100	1C	0.7109	5B	7.8125
00011101	1D	0.7188	5C	7.8125
00011110	1E	0.7266	5D	7.8125
00011111	1F	1.3516	AD	
00100000	20	0.8516	6D	
00100001	21	0.7344	5E	7.8125
00100010	22	0.7422	5F	7.8125
00100011	23	0.7500	60	7.8125
00100100	24	0.7578	61	7.8125
00100101	25	0.7656	62	7.8125
00100110	26	0.7734	63	7.8125
00100111	27	0.7813	64	7.8125
00101000	28	0.7891	65	7.8125
00101001	29	0.7969	66	7.8125
00101010	2A	0.8047	67	7.8125
00101011	2B	0.8125	68	7.8125
00101100	2C	0.8203	69	7.8125
00101101	2D	0.8281	6A	7.8125
00101110	2E	0.8359	6B	7.8125
00101111	2F	0.8438	6C	7.8125
00110000	30	0.8516	6D	7.8125
00110001	31	0.8594	6E	7.8125
00110010	32	0.8672	6F	7.8125
00110011	33	0.8750	70	7.8125
00110100	34	0.8828	71	7.8125
00110101	35	0.8906	72	7.8125
00110110	36	0.8984	73	7.8125
00110111	37	0.9063	74	7.8125
00111000	38	0.9141	75	7.8125
00111001	39	0.9219	76	7.8125
00111010	3A	0.9297	77	7.8125
00111011	3B	0.9375	78	7.8125

TABLE 7. PROG1 8-BIT (BOOT-UP VOLTAGE) (Continued)

BINARY CODE	HEX CODE	V_{BOOT} (V)	VOUT COMMAND CODE (HEX)	DELTA FROM PREVIOUS CODE (mV)
00111100	3C	0.9453	79	7.8125
00111101	3D	0.9531	7A	7.8125
00111110	3E	0.9609	7B	7.8125
00111111	3F	1.5000	C0	
01000000	40	0.8984	73	
01000001	41	0.9688	7C	7.8125
01000010	42	0.9766	7D	7.8125
01000011	43	0.9844	7E	7.8125
01000100	44	0.9922	7F	7.8125
01000101	45	1.0000	80	7.8125
01000110	46	1.0078	81	7.8125
01000111	47	1.0156	82	7.8125
01001000	48	1.0234	83	7.8125
01001001	49	1.0313	84	7.8125
01001010	4A	1.0391	85	7.8125
01001011	4B	1.0469	86	7.8125
01001100	4C	1.0547	87	7.8125
01001101	4D	1.0625	88	7.8125
01001110	4E	1.0703	89	7.8125
01001111	4F	1.0781	8A	7.8125
01010000	50	1.0859	8B	7.8125
01010001	51	1.0938	8C	7.8125
01010010	52	1.1016	8D	7.8125
01010011	53	1.1094	8E	7.8125
01010100	54	1.1172	8F	7.8125
01010101	55	1.1250	90	7.8125
01010110	56	1.1328	91	7.8125
01010111	57	1.1406	92	7.8125
01011000	58	1.1484	93	7.8125
01011001	59	1.1563	94	7.8125
01011010	5A	1.1641	95	7.8125
01011011	5B	1.1719	96	7.8125
01011100	5C	1.1797	97	7.8125
01011101	5D	1.1875	98	7.8125
01011110	5E	1.1953	99	7.8125
01011111	5F	1.7969	E6	
01100000	60	0.9531	7A	
01100001	61	1.2031	9A	7.8125
01100010	62	1.2109	9B	7.8125

TABLE 7. PROG1 8-BIT (BOOT-UP VOLTAGE) (Continued)

BINARY CODE	HEX CODE	V_{BOOT} (V)	VOUT COMMAND CODE (HEX)	DELTA FROM PREVIOUS CODE (mV)
01100011	63	1.2188	9C	7.8125
01100100	64	1.2266	9D	7.8125
01100101	65	1.2344	9E	7.8125
01100110	66	1.2422	9F	7.8125
01100111	67	1.2500	A0	7.8125
01101000	68	1.2578	A1	7.8125
01101001	69	1.2656	A2	7.8125
01101010	6A	1.2734	A3	7.8125
01101011	6B	1.2813	A4	7.8125
01101100	6C	1.2891	A5	7.8125
01101101	6D	1.2969	A6	7.8125
01101110	6E	1.3047	A7	7.8125
01101111	6F	1.3125	A8	7.8125
01110000	70	1.3203	A9	7.8125
01110001	71	1.3281	AA	7.8125
01110010	72	1.3359	AB	7.8125
01110011	73	1.3438	AC	7.8125
01110100	74	1.3516	AD	7.8125
01110101	75	1.3594	AE	7.8125
01110110	76	1.3672	AF	7.8125
01110111	77	1.3750	B0	7.8125
01111000	78	1.3828	B1	7.8125
01111001	79	1.3906	B2	7.8125
01111010	7A	1.3984	B3	7.8125
01111011	7B	1.4063	B4	7.8125
01111100	7C	1.4141	B5	7.8125
01111101	7D	1.4219	B6	7.8125
01111110	7E	1.4297	B7	7.8125
01111111	7F	2.5000	140	
10000000	80	1.0000	80	
10000001	81	1.4375	B8	7.8125
10000010	82	1.4453	B9	7.8125
10000011	83	1.4531	BA	7.8125
10000100	84	1.4609	BB	7.8125
10000101	85	1.4688	BC	7.8125
10000110	86	1.4766	BD	7.8125
10000111	87	1.4844	BE	7.8125
10001000	88	1.4922	BF	7.8125
10001001	89	1.5000	C0	7.8125

TABLE 7. PROG1 8-BIT (BOOT-UP VOLTAGE) (Continued)

BINARY CODE	HEX CODE	V_{BOOT} (V)	VOUT COMMAND CODE (HEX)	DELTA FROM PREVIOUS CODE (mV)
10001010	8A	1.5078	C1	7.8125
10001011	8B	1.5156	C2	7.8125
10001100	8C	1.5234	C3	7.8125
10001101	8D	1.5313	C4	7.8125
10001110	8E	1.5391	C5	7.8125
10001111	8F	1.5469	C6	7.8125
10010000	90	1.5547	C7	7.8125
10010001	91	1.5625	C8	7.8125
10010010	92	1.5703	C9	7.8125
10010011	93	1.5781	CA	7.8125
10010100	94	1.5859	CB	7.8125
10010101	95	1.5938	CC	7.8125
10010110	96	1.6016	CD	7.8125
10010111	97	1.6094	CE	7.8125
10011000	98	1.6172	CF	7.8125
10011001	99	1.6250	D0	7.8125
10011010	9A	1.6328	D1	7.8125
10011011	9B	1.6406	D2	7.8125
10011100	9C	1.6484	D3	7.8125
10011101	9D	1.6563	D4	7.8125
10011110	9E	1.6641	D5	7.8125
10011111	9F	3.0000	180	
10100000	A0	1.0469	86	
10100001	A1	1.6719	D6	7.8125
10100010	A2	1.6797	D7	7.8125
10100011	A3	1.6875	D8	7.8125
10100100	A4	1.6953	D9	7.8125
10100101	A5	1.7031	DA	7.8125
10100110	A6	1.7109	DB	7.8125
10100111	A7	1.7188	DC	7.8125
10101000	A8	1.7266	DD	7.8125
10101001	A9	1.7344	DE	7.8125
10101010	AA	1.7422	DF	7.8125
10101011	AB	1.7500	E0	7.8125
10101100	AC	1.7578	E1	7.8125
10101101	AD	1.7656	E2	7.8125
10101110	AE	1.7734	E3	7.8125
10101111	AF	1.7813	E4	7.8125
10110000	B0	1.7891	E5	7.8125

TABLE 7. PROG1 8-BIT (BOOT-UP VOLTAGE) (Continued)

BINARY CODE	HEX CODE	V_{BOOT} (V)	VOUT COMMAND CODE (HEX)	DELTA FROM PREVIOUS CODE (mV)
10110001	B1	1.7969	E6	7.8125
10110010	B2	1.8047	E7	7.8125
10110011	B3	1.8125	E8	7.8125
10110100	B4	1.8203	E9	7.8125
10110101	B5	1.8281	EA	7.8125
10110110	B6	1.8359	EB	7.8125
10110111	B7	1.9141	F5	78.125
10111000	B8	1.9922	FF	78.125
10111001	B9	2.0703	109	78.125
10111010	BA	2.1484	113	78.125
10111011	BB	2.2266	11D	78.125
10111100	BC	2.3047	127	78.125
10111101	BD	2.3828	131	78.125
10111110	BE	2.4609	13B	78.125
10111111	BF	3.2969	1A6	
11000000	C0	1.1016	8D	
11000001	C1	2.4688	13C	7.8125
11000010	C2	2.4766	13D	7.8125
11000011	C3	2.4844	13E	7.8125
11000100	C4	2.4922	13F	7.8125
11000101	C5	2.5000	140	7.8125
11000110	C6	2.5078	141	7.8125
11000111	C7	2.5156	142	7.8125
11001000	C8	2.5234	143	7.8125
11001001	C9	2.6016	14D	78.125
11001010	CA	2.6797	157	78.125
11001011	CB	2.7578	161	78.125
11001100	CC	2.8359	16B	78.125
11001101	CD	2.9141	175	78.125
11001110	CE	2.9922	17F	78.125
11001111	CF	3.0703	189	78.125
11010000	D0	3.1484	193	78.125
11010001	D1	3.2266	19D	78.125
11010010	D2	3.2813	1A4	54.6875
11010011	D3	3.2891	1A5	7.8125
11010100	D4	3.2969	1A6	7.8125
11010101	D5	3.3047	1A7	7.8125
11010110	D6	3.3125	1A8	7.8125
11010111	D7	3.3203	1A9	7.8125

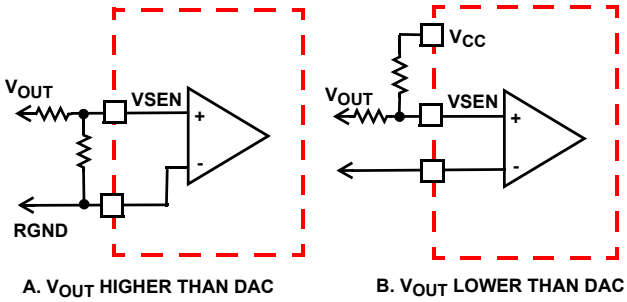
TABLE 7. PROG1 8-BIT (BOOT-UP VOLTAGE) (Continued)

BINARY CODE	HEX CODE	V_{BOOT} (V)	VOUT COMMAND CODE (HEX)	DELTA FROM PREVIOUS CODE (mV)
11011000	D8	3.3281	1AA	7.8125
11011001	D9	3.4063	1B4	78.125
11011010	DA	3.4844	1BE	78.125
11011011	DB	3.5625	1C8	78.125
11011100	DC	3.6406	1D2	78.125
11011101	DD	3.7188	1DC	78.125
11011110	DE	3.7969	1E6	78.125
11011111	DF	5.0000	280	
11100000	E0	1.2031	9A	
11100001	E1	3.8750	1F0	78.125
11100010	E2	3.9531	1FA	78.125
11100011	E3	4.0313	204	78.125
11100100	E4	4.1094	20E	78.125
11100101	E5	4.1875	218	78.125
11100110	E6	4.2656	222	78.125
11100111	E7	4.3438	22C	78.125
11101000	E8	4.4219	236	78.125
11101001	E9	4.5000	240	78.125
11101010	EA	4.5781	24A	78.125
11101011	EB	4.6563	254	78.125
11101100	EC	4.7344	25E	78.125
11101101	ED	4.8125	268	78.125
11101110	EE	4.8906	272	78.125
11101111	EF	4.9688	27C	78.125
11110000	F0	4.9766	27D	7.8125
11110001	F1	4.9844	27E	7.8125
11110010	F2	4.9922	27F	7.8125
11110011	F3	5.0000	280	7.8125
11110100	F4	5.0078	281	7.8125
11110101	F5	5.0156	282	7.8125
11110110	F6	5.0234	283	7.8125
11110111	F7	5.0313	284	7.8125
11111000	F8	5.1094	28E	78.125
11111001	F9	5.1875	298	78.125
11111010	FA	5.2656	2A2	78.125
11111011	FB	5.3438	2AC	78.125
11111100	FC	5.4219	2B6	78.125
11111101	FD	5.4922	2BF	70.3125
11111110	FE	5.5000	2C0	7.8125

TABLE 7. PROG1 8-BIT (BOOT-UP VOLTAGE) (Continued)

BINARY CODE	HEX CODE	V_{BOOT} (V)	VOUT COMMAND CODE (HEX)	DELTA FROM PREVIOUS CODE (mV)
11111111	FF	0	0	

As shown in Table 7, 1 step is 2^{-7} = 7.8125mV; some selections are higher than 1 step from adjacent codes. However, the resolution is ±7.8125mV around the popular voltage regulation points, as in Table 3 on page 11, for fine-tuning purposes. For finer than 7.8125mV tuning, a large ratio resistor divider can be placed on the VSEN pin between the output (V_{OUT}) and RGND for positive offset or V_{CC} for negative offset, as shown in Figure 8.



A. V_{OUT} HIGHER THAN DAC B. V_{OUT} LOWER THAN DAC

FIGURE 8. EXTERNAL PROGRAMMABLE REGULATION

Current Sensing

The ISL68201 supports inductor DCR sensing, or resistive sensing techniques, and senses current continuously for fast response. The current sense amplifier uses the CSEN and CSRTN inputs to reproduce a signal proportional to the inductor current, I_L. The sense current, I_{SEN}, is proportional to the inductor current and is used for current reporting and overcurrent protection.

The input bias current of the current sensing amplifier is typically 10s of nA. Less than 15kΩ input impedance connected to CSEN pin is preferred to minimize the offset error, that is, use a larger C value (select 0.22µF to 1µF instead of 0.1µF when needed). In addition, the current sensing gain resistor connected to CSRTN pin should be within 40Ω to 3.5kΩ.

INDUCTOR DCR SENSING

An inductor's winding is characteristic of a distributed resistance, as measured by the Direct Current Resistance (DCR) parameter. A simple R-C network across the inductor extracts the DCR voltage, as shown in Figure 9.

The voltage on the capacitor V_C, can be shown to be proportional to the inductor current I_L, as in Equation 5.

$$V_C(s) = \frac{\left(s \cdot \frac{L}{DCR} + 1\right) \cdot (DCR \cdot I_L)}{(s \cdot RC + 1)} \quad \text{(EQ. 5)}$$

If the R-C network components are selected so that the R-C time constant (= R*C) matches the inductor time constant (= L/DCR), the voltage across the capacitor V_C is equal to the voltage drop across the DCR. With the internal low-offset current amplifier, the capacitor voltage V_C is replicated across the sense resistor R_{ISEN}. Therefore, the current out of the CSRTN pin, I_{SEN}, is proportional to the inductor current.

Equation 6 shows that the ratio of the inductor current to the sensed current, I_{SEN}, is driven by the value of the sense resistor and the DCR of the inductor.

$$I_{SEN} = I_L \cdot \frac{DCR}{R_{ISEN}} \quad \text{(EQ. 6)}$$

The inductor DCR value will increase as the temperature increases. Therefore, the sensed current will increase as the temperature of the current sense element increases. To compensate for the temperature effect on the sensed current signal, the integrated temperature compensation function of ISL68201 should be used. The integrated temperature compensation function is described in"Thermal Monitoring and Compensation" on page 18.

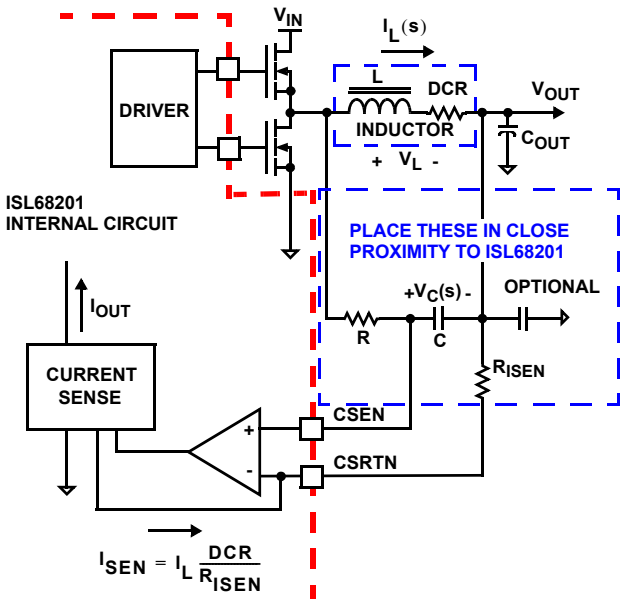


FIGURE 9. DCR SENSING CONFIGURATION

RESISTIVE SENSING

For accurate current sense, a dedicated current-sense resistor, R_{SENSE}, in series with each output inductor, can serve as the current sense element (see Figure 10). This technique, however, reduces overall converter efficiency due to the additional power loss on the current sense element R_{SENSE}.

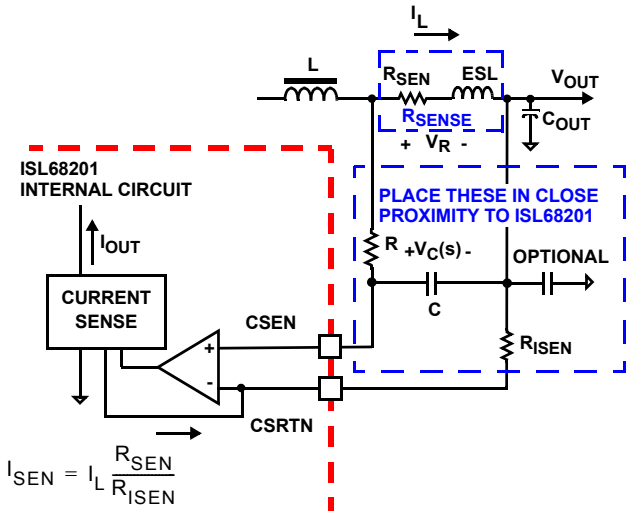


FIGURE 10. SENSE RESISTOR IN SERIES WITH INDUCTORS

A current sensing resistor has a distributed parasitic inductance, known as Equivalent Series Inductance (ESL) parameter, typically less than 1nH. A simple R-C network across the current-sense resistor extracts the R_{SEN} voltage, as shown in Figure 10 on page 17.

The voltage on the capacitor V_C, can be shown to be proportional to the inductor current I_L, see Equation 7.

$$V_C(s) = \frac{\left(s \cdot \frac{ESL}{R_{SEN}} + 1\right) \cdot (R_{SEN} \cdot I_L)}{(s \cdot RC + 1)} \quad \text{(EQ. 7)}$$

If the R-C network components are selected so that the RC time constant matches the ESL-R_{SEN} time constant ($R*C = ESL/R_{SEN}$), the voltage across the capacitor V_C is equal to the voltage drop across the R_{SEN}, that is, proportional to the inductor current. As an example, a typical 1mΩ sense resistor can use R = 348Ω and C = 820pF for the matching. Figures 11 and 12 show the sensed waveforms without and with matching RC when using resistive sense.

FIGURE 11. VOLTAGE ACROSS R WITHOUT RC

FIGURE 12. VOLTAGE ACROSS C WITH MATCHING RC

Equation 8 shows that the ratio of the inductor current to the sensed current, I_{SEN}, is driven by the value of the sense resistor and the R_{ISEN}.

$$I_{SEN} = I_L \cdot \frac{R_{SEN}}{R_{ISEN}} \quad \text{(EQ. 8)}$$

L/DCR OR ESL/R_{SEN} MATCHING

Figure 13 shows the expected load transient response waveforms if L/DCR or ESL/R_{SEN} is matching the R-C time constant. When the load current has a square change, the IOUT pin voltage (V_{IOUT}) without a decoupling capacitor also has a square response. However, there is always some PCB contact impedance of current sensing components between the two current sensing points; it hardly accounts into the L/DCR or ESL/R_{SEN} matching calculation. Fine tuning the matching is done in the board level to improve overall transient performance and system reliability.

If the R-C timing constant is too large or too small, $V_C(s)$ will not accurately represent real-time output current and will worsen the overcurrent fault response. Figure 14 shows the IOUT pin transient voltage response when the R-C timing constant is too small. V_{IOUT} will sag excessively upon load insertion and may create a system failure or early overcurrent trip. Figure 15 shows the transient response when the R-C timing constant is too large. V_{IOUT} is sluggish in reaching its final value. The excessive delay on current sensing will not provide a fast OCP response and hurt system reliability.

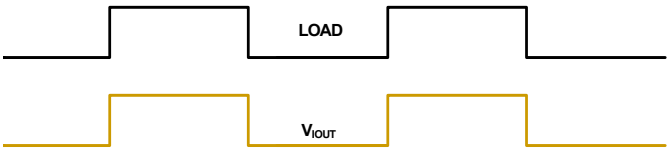


FIGURE 13. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS

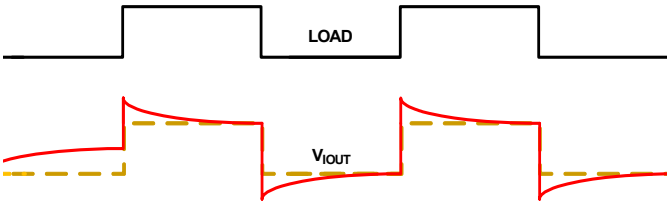


FIGURE 14. LOAD TRANSIENT RESPONSE WHEN R-C TIME CONSTANT IS TOO SMALL

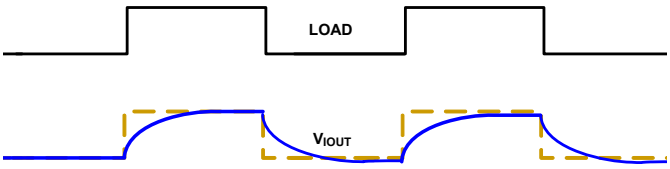


FIGURE 15. LOAD TRANSIENT RESPONSE WHEN R-C TIME CONSTANT IS TOO LARGE

Note that the integrated thermal compensation applies to the DC current, but not the AC current; therefore, the peak current seen by the controller will increase as the temperature decreases and can potentially trigger an OCP event. To overcome this issue, the RC should be over-matching L/DCR at room temperature by (-40°C +25°C)*0.385%/°C = +25% for -40°C operation.

Thermal Monitoring and Compensation

The diagram of thermal monitoring function block is shown in Figure 16 on page 18. One NTC resistor should be placed close to the respective power stage of the voltage regulator VR to sense the operational temperature, and pull-up resistors are needed to form the voltage dividers for the NTC pin. As the temperature of the power stage increases, the resistance of the NTC will reduce, resulting in the reduced voltage at the NTC pin. Figure 18 on page 18 shows the TM voltage over the temperature for a typical design with a recommended 10kΩ NTC (P/N: NCP15XH103J03RC from Murata, β = 3380) and 1.54kΩ resistor RTM. It is recommended to use those resistors for accurate temperature compensation because the internal thermal digital code is developed based on these two components. If a different value is used, the temperature coefficient must be close to 3380 and RTM must be scaled accordingly. For instance, if NTC = 20kΩ (β = 3380), then RTM should be 20kΩ/10kΩ*1.54kΩ = 3.08kΩ.

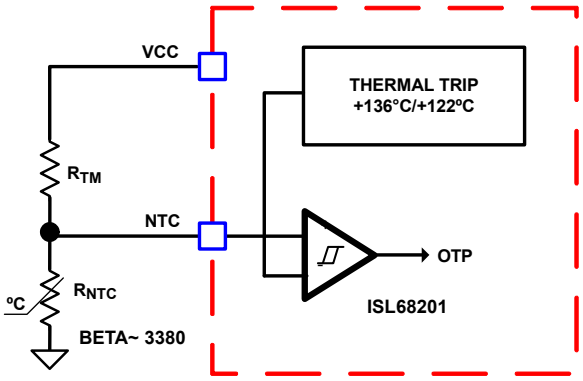


FIGURE 16. BLOCK DIAGRAM OF THERMAL MONITORING AND PROTECTION

The ISL68201 supports inductor DCR sensing, or resistive sensing techniques. The inductor DCR has a positive temperature coefficient, which is about +0.385%/°C. Because the voltage across the inductor is sensed for the output current information, the sensed current has the same positive temperature coefficient as the inductor DCR. To obtain the correct current information, the ISL68201 uses the voltage at the NTC pin and "TCOMP" register to compensate the temperature impact on the sensed current. The block diagram of this function is shown in Figure 17.

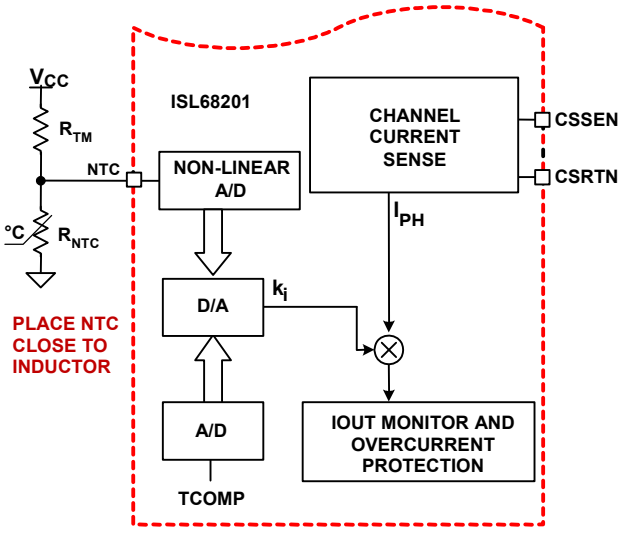


FIGURE 17. BLOCK DIAGRAM OF INTEGRATED TEMPERATURE COMPENSATION

When the NTC is placed close to the current sense component (inductor), the temperature of the NTC will track the temperature of the current sense component. Therefore, the NTC pin voltage can be used to obtain the temperature of the current sense component. Because the NTC could pick up noise from phase node, a 0.1µF ceramic decoupling capacitor is recommended on the NTC pin in close proximity to the controller.

Based on the V_{CC} voltage, the ISL68201 converts the NTC pin voltage to a digital signal for temperature compensation. With the nonlinear A/D converter of the ISL68201, the NTC digital signal is linearly proportional to the NTC temperature. For accurate temperature compensation, the ratio of the NTC voltage to the NTC temperature of the practical design should be similar to that in Figure 18.

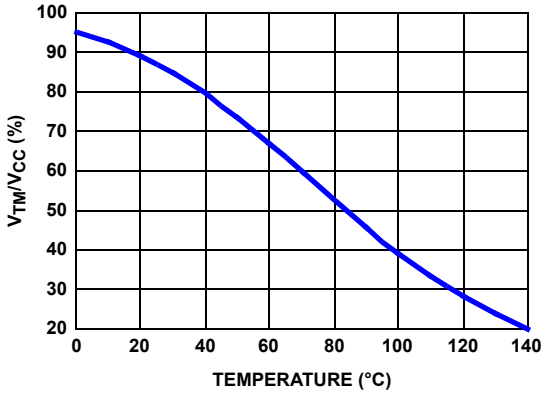


FIGURE 18. THE RATIO OF TM VOLTAGE TO NTC TEMPERATURE WITH RECOMMENDED PART

Because the NTC attaches to the PCB, but not directly to the current sensing component, it inherits high thermal impedance between the NTC and the current sensing element. The “TCOMP” register values can be used to correct the temperature difference between NTC and the current sense component. As shown in Figure 19, the NTC should be placed in proximity to the output rail; DO NOT place it close to the MOSFET side, which generates much more heat.

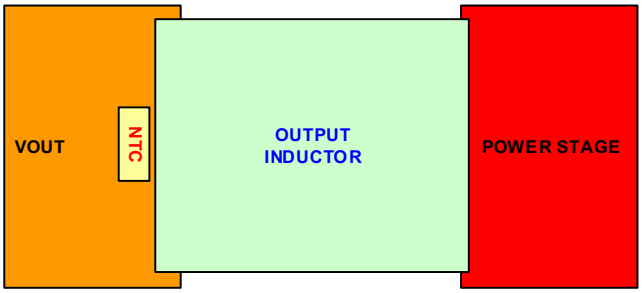


FIGURE 19. RECOMMENDED PLACEMENT OF NTC

The ISL68201 multiplexes the “TCOMP” value with the NTC digital signal to obtain the adjustment gain to compensate the temperature impact on the sensed channel current. The compensated current signal is used for I_{OUT} and overcurrent protection functions. The TCOMP “OFF” code is to disable thermal compensation when the current sensing element is the resistor or smart power stage (internally thermal compensated) that has little thermal drifting.

TABLE 8. TCOMP VALUES

D1h	TCOMP (°C)	D1h	TCOMP (°C)
0h	30	2h	5
1h	15	3h	OFF

The thermal compensation design procedure for inductor current sensing is summarized as follows:

1. Properly choose the voltage divider for the NTC pin to match the NTC voltage vs temperature curve with the recommended curve in Figure 18 on page 18.
2. Run the actual board under the full load and the desired airflow condition.
3. After the board reaches the thermal steady state (often takes 15 minutes), record the temperature (T_{CSC}) of the current sense component (inductor) and the voltage at NTC and VCC pins.
4. Use Equation 9 to calculate the resistance of the NTC, and find out the corresponding NTC temperature T_{NTC} from the NTC datasheet or using Equation 10, where β is equal to 3380 for recommended NTC.

$$R_{NTC}(\text{at } T_{NTC}) = \frac{V_{TM} \times R_{TM}}{V_{CC} - V_{TM}} \quad \text{(EQ. 9)}$$

$$T_{NTC} = \frac{\beta}{\ln\left(\frac{R_{NTC}(\text{at } 25°C)}{R_{NTC}(\text{at } T_{NTC})}\right) + \frac{\beta}{298.15}} - 273.15 \quad \text{(EQ. 10)}$$

5. Choose a number close to the result as in Equation 11 for the “TCOMP” register.

$$T_{COMP} = T_{CSC} - T_{NTC} \quad \text{(EQ. 11)}$$

6. Run the actual board under full load again.
7. Record the IOUT pin voltage as V1 immediately after the output voltage is stable with the full load. Record the IOUT pin voltage as V2 after the VR reaches the thermal steady state.
8. If the IOUT pin voltage increases over 10mV as the temperature increases (that is, V2 - V1 > 10mV), reduce the “TCOMP” value. If the IOUT pin voltage decreases over 10mV as the temperature increases (that is, V1 - V2 > 10mV), increase the “TCOMP” value. The “TCOMP” value can be adjusted through the serial bus for easy thermal compensation optimization.

I_{OUT} Calibration

The current flowing out of the IOUT pin is equal to the sensed average current inside ISL68201. A resistor is placed from the IOUT pin to GND to generate a voltage, which is proportional to the load current and the resistor value, as shown in Equation 12:

$$R_{IOUT} = \frac{2.5V \times R_{ISEN}}{63.875A \times R_X} = \frac{2.5V \times \left(\frac{R_X \times I_{OCP}}{100\mu A}\right)}{63.875A \times R_X}$$

$$= \frac{2.5V \times I_{OCP}}{63.875A \times 100\mu A} = \frac{25V \times I_{OCP}}{63.875A}\ k\Omega \quad \text{(EQ. 12)}$$

where V_{IOUT} is the voltage at the IOUT pin, R_{IOUT} is the resistor between the IOUT pin and GND, I_{LOAD} is the total output current of the converter, R_{ISEN} is the sense resistor connected to the CSRTN pin, and R_X is the DC resistance of the current sense element, either the DCR of the inductor or R_{SENSE} depending on the sensing method. The R_{IOUT} resistor should be scaled to ensure that the voltage at the IOUT pin is typically 2.5V at 63.875A load current. The I_{OUT} voltage is linearly digitized every 108µs and stored in the READ_IOUT register (8Ch).

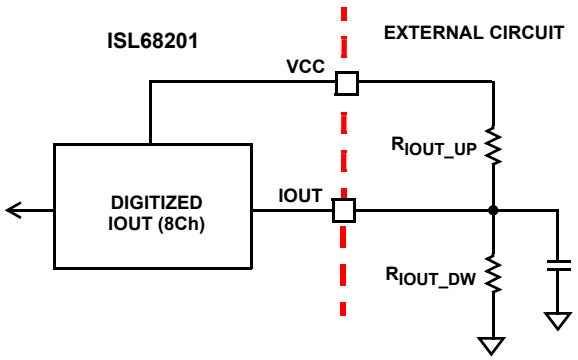


FIGURE 20. IOUT NO LOAD OFFSET CALIBRATION

A small capacitor can be placed between IOUT and GND to reduce the noise impact and provide averaging, > 200µs (typically).

To deal with layout and design variation of different platforms, the ISL68201 is intentionally trimmed to negative at no load, thus, an offset can easily be added to calibrate the digitized I_{OUT}

reading (8Ch). Hence, the analog vs digitized current slope is set by the equivalent impedance of $R_{IOUT_UP}//R_{IOUT_DW} = R_{IOUT}$ (as in Figure 20); the slope of the ideal curve should set to 1A/A with 0A offset.

For a precision digital I_{OUT}, follow the fine-tuned procedure below. Steps 1 to 5 must be completed before Step 6.

1. Properly tune L/DCR or ESL/R_{SEN} matching as shown on page 17 over the range of temperature operation. +25% over-matching L/DCR at room temperature is needed for -40°C operation.
2. Properly complete thermal compensation as shown in "Thermal Monitoring and Compensation" on page 18.
3. Finalize the R_{ISEN} resistor to set OCP for overall operating conditions and board variations as shown in "Overcurrent and Short-Circuit Protection" on page 20.
4. Collect no load I_{OUT} current with sufficient prototypes and determine the mean of no load I_{OUT} current.
5. The pull-up impedance on IOUT pin should be "VCC/IOUT_NO_LOAD". For instance, a mean of -2.5µA I_{OUT} at 0A load will need R_{IOUT_UP} = 2MΩ.
6. Start with the value below and then fine-tune the R_{IOUT_DW} value until the average slope of various boards equals 1A/A.

$$R_{IOUT_DW} = \frac{R_{IOUT_UP} \times R_{IOUT}}{R_{IOUT_UP} - R_{IOUT}} \quad \text{(EQ. 13)}$$

Fault Protection

The ISL68201 provides high system reliability with many fault protections, as summarized in Table 9.

TABLE 9. FAULT PROTECTION SUMMARY

FAULT	DESCRIPTION	FAULT ACTION
Input UVLO	VIN pin UVLO; or set by EN pin with an external divider for a higher level. See Figures 4 and 5.	Shut down and recover when V_{IN} > UVLO
Bias UVLO	VCC, PVCC, 7VLDO UVLO	Shut down and recover when Bias > UVLO
Start-Up OVP	Higher than V_{BOOT}. See Electrical Specifications on page 7.	Latch OFF, reset by V_{CC} or toggling enable (including EN pin and/or OPERATION command based on the ON_OFF_CONFIG setting)
Output OVP	Rising = 120%; Falling = 100%	
Output UVP	74% of V_{OUT}, Latch OFF	
Output OCP	Average OCP = 100µA with 128µs blanking time.	Latch OFF (reset by V_{CC} or toggling enable including EN pin and/or OPERATION command based on the ON_OFF_CONFIG setting), or retry every 9ms; option is programmable by PROG3 or D3[0]
Short-Circuit Protection	Peak OCP = 130% of Average OCP with 50ns filter.	
OTP	Rising = 22.31%VCC (~+136°C); Falling =27.79%VCC (~+122°C).	Shut down above +136°C and recover when temperature drops below +122°C

UVLO and OTP faults will respond to the current state with hysteresis, while output OVP and output UVP faults are latch events, while output OCP and output short-circuit faults can be latch or retry events depending upon PROG3 or D3[0] setting. All fault latch event can be reset by VCC cycling, toggling the Enable pin and/or the serial bus OPERATION command based on the ON_OFF_CONFIG setting, while the OCP retry event has a hiccup time of 9ms and the regulator can be recovered when the fault is removed.

OVERVOLTAGE PROTECTION

The OVP fault detection circuit triggers after the voltage between VSEN+ and VSEN- is above the rising overvoltage threshold. When an OVP fault is declared, the controller will be latched off and the PGOOD pin will be asserted low. The fault will remain latched and can be reset by V_{CC} cycling or toggling EN pin and/or the serial bus OPERATION command based on the ON_OFF_CONFIG setting.

Although the controller has latched off in response to an OVP fault, the LGATE gate-driver output will retain the ability to toggle the low-side MOSFET on and off, in response to the output voltage transversing the OVP rising and falling thresholds. The LGATE gate driver will turn on the low-side MOSFET to discharge the output voltage, protecting the load. The LGATE gate driver will turn off the low-side MOSFET when the sensed output voltage is lower than the falling overvoltage threshold (typically 100%). If the output voltage rises again, the LGATE driver will again turn on the low-side MOSFET when the output voltage is above the rising overvoltage threshold (typically 120%). By doing so, the IC protects the load when there is a consistent overvoltage condition.

In addition to normal operation OVP, 5.5ms (typically, worst case = 6.5ms) after all rails (VCC, PVCC, 7VLDO, VIN) POR and before the end of soft-start, the start-up OVP circuits are enabled to protect against an OVP event, while the OVP level is set higher than V_{BOOT}. See Electrical Specifications on page 7.

UNDERVOLTAGE PROTECTION

The UVP fault detection circuit triggers when the output voltage is below the undervoltage threshold (typically 74% of DAC). When a UVP fault is declared, the controller will be latched off, forcing the LGATE and UGATE gate-driver outputs low, and the PGOOD pin will be asserted low. The fault will remain latched and can be reset by V_{CC} cycling or toggling the EN pin and/or the serial bus OPERATION command based on the ON_OFF_CONFIG setting.

OVERCURRENT AND SHORT-CIRCUIT PROTECTION

The average Overcurrent Protection (OCP) is triggered when the internal current out of the IOUT pin goes above the fault threshold (typically 100µA) with 128µs blanking time. It also has a fast (50ns filter) secondary overcurrent protection whose threshold is +30% above average OCP. This protects inductor saturation from a short-circuit event and provides a more robust

power train and system protection. When an OCP or short-circuit fault is declared, the controller will be latched off, forcing the LGATE and UGATE gate-driver outputs low, or retry with a hiccup time of 9ms. The fault response is programmable by PROG3 or D3[0]. However, the latched off event can be reset by V_{CC} cycling or toggling EN pin and/or the serial bus OPERATION command based on the ON_OFF_CONFIG setting.

Equation 14 provides a starting point to set a preliminary OCP trip point, in which IOCP is the targeted OCP trip point and DI (as in Equation 15) is the peak-to-peak inductor ripple current.

$$R_{ISEN1} = \frac{R_x x I_{OCP}}{100\mu A} \quad \text{(EQ. 14)}$$

$$R_{ISEN2} = \frac{R_x x \left(\frac{\Delta I}{2} + I_{OCP}\right)}{100\mu A x (100\% + 30\%)}$$

$$R_{ISEN} = MAX\,(R_{ISEN1},\ R_{ISEN2})$$

To deal with layout and PCB contact impedance variation, follow the fine-tuning procedure below for a more precise OCP. Steps 1 to 3 must be completed before Step 4.

1. Properly tune L/DCR or ESL/R_{SEN} matching as shown on page 17 over the range of temperature operation. +25% over-matching L/DCR at room temperature is needed for -40°C operation.
2. Properly complete thermal compensation as shown in "Thermal Monitoring and Compensation" on page 18.
3. Collect OCP trip points (IOCP_MEASURED) with sufficient prototypes and determine the mean for overall operating conditions and board variations.
4. Change R_{ISEN} by IOCP_TARGETED/IOCP_MEASURED percentage to meet the targeted OCP.

Note that if the inductor peak-to-peak current is higher or closer to 30%, the +30% threshold could be triggered instead of the average OCP threshold. However, the fine-tuning procedure can still be used.

OVER-TEMPERATURE PROTECTION

As shown in Figures 16 on page 18, there is a comparator with hysteresis to compare the NTC pin voltage to the threshold set. When the NTC pin voltage is lower than 22.31% of the V_{CC} voltage (typically +136°C), it triggers Over-Temperature Protection (OTP) and shuts down the ISL68201. When the NTC pin voltage is above 27.79% of the V_{CC} voltage (typically +122.4°C), the ISL68201 will resume normal operation. When an OTP fault is declared, the controller forces the LGATE and UGATE gate-driver outputs low.

PGOOD Monitor

The PGOOD pin indicates when the converter is capable of supplying regulated voltage. If there is a fault condition of a rail's (VCC, PVCC, 7VLDO, or VIN) UVLO, output Overcurrent (OCP), Overvoltage (OVP), Undervoltage (UVP), or Over-Temperature (OTP), PGOOD is asserted low. Note that the PGOOD pin is an undefined impedance with insufficient V_{CC} (typically <2.5V).

PFM Mode Operation

In PFM mode, programmable by PROG2 or serial bus D0[0:0], the switching frequency is dramatically reduced to minimize the switching loss and significantly improve light-load efficiency. The ISL68201 can enter and exit PFM mode seamlessly as the load changes. The PFM mode is only compatible with Intersil's ISL99140 DrMOS with SMOD input by connecting to ISL68201's FCCM output pin. Incompatible power stages should operate in PWM mode.

SMBus, PMBus, and I²C Operation

The ISL68201 features SMBus, PMBus, and I²C with 32 programmable addresses through the PROG2 pin, while SMBus/PMBus includes an Alert# line (SALERT) and Packet Error Check (PEC) to ensure data properly transmitted. The telemetry update rate is 108µs (typically). The supported SMBus/PMBus/I²C addresses are summarized in Table 10. The 7-bit format address does not include the last bit (write and read): 40-47h, 60-67h, and 70-7Fh.

SMBus/PMBus/I²C allows users to program the registers as in Table 11, except for SMBus/PMBus/I²C addresses, 5.5ms (typically, worst 6.5ms) after all rails (VCC, PVCC, 7VLDO, and VIN) above POR. Figures 21 and 22 show the initialization timing diagram for the serial bus with different state of EN (Enable) pin.

For proper operation, users should follow the SMBus, PMBus, and I²C protocol, as shown in Figure 23 on page 23. Note that the STOP (P) bit is NOT allowed before the repeated START condition when reading the contents of the register.

When the device's serial bus is not used, simply ground the device's SCL, SDA, and SALERT pins and do not connect them to the bus.

TABLE 10. SMBus/PMBus/I²C 7-BIT FORMAT ADDRESS (HEX)

7-BIT ADDRESS	7-BIT ADDRESS	7-BIT ADDRESS
40	63	76
41	64	77
42	65	78
43	66	79
44	67	7A
45	70	7B
46	71	7C
47	72	7D
60	73	7E
61	74	7F
62	75	

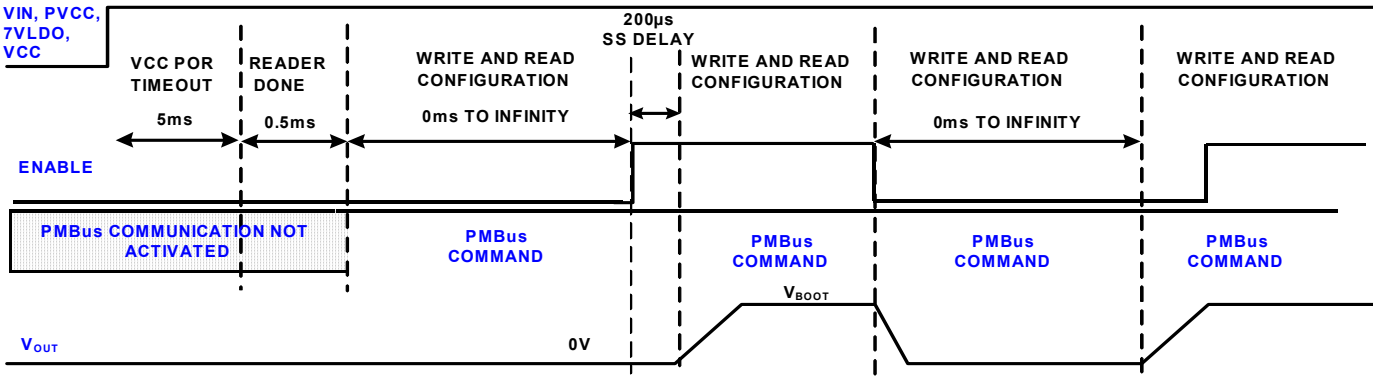


FIGURE 21. SIMPLIFIED SMBus/PMBus/I2C INITIALIZATION TIMING DIAGRAM WITH ENABLE LOW

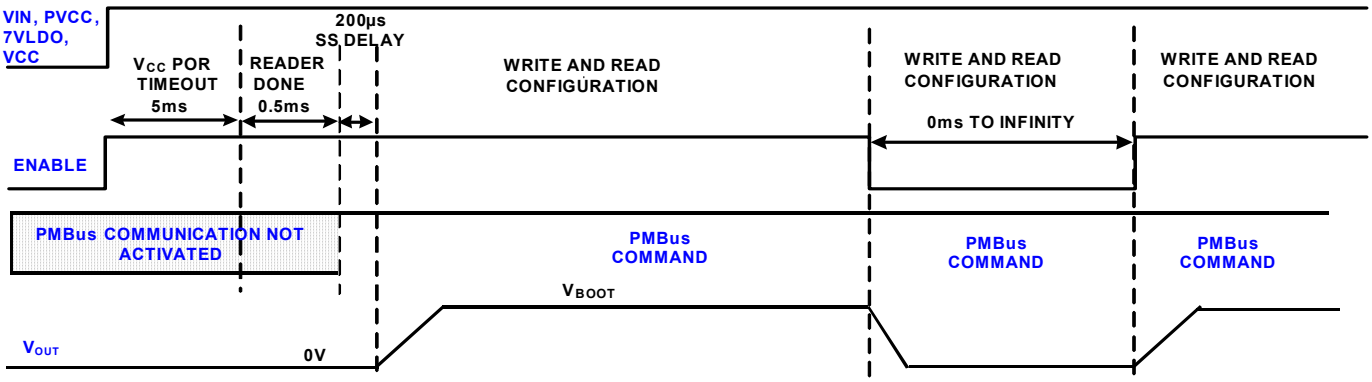
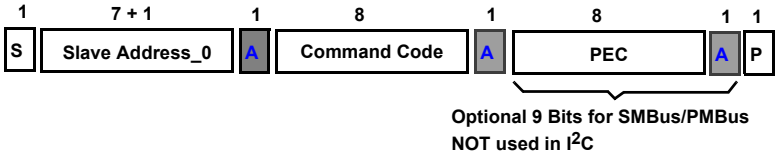


FIGURE 22. SIMPLIFIED SMBus/PMBus/I2C INITIALIZATION TIMING DIAGRAM WITH ENABLE HIGH

1. Send Byte Protocol

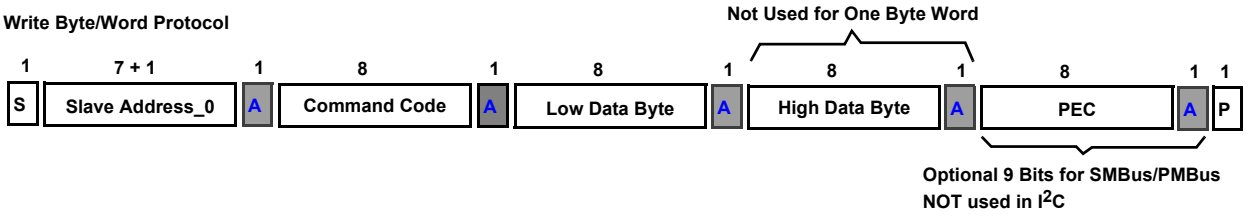


Example command: 03h Clear Faults
(This will clear all of the bits in Status Byte for the selected Rail)

S: Start Condition
A: Acknowledge (“0”)
N: Not Acknowledge (“1”)
W: Write (“0”)
RS: Repeated Start Condition
R: Read (“1”)
PEC: Packet Error Checking
P: Stop Condition

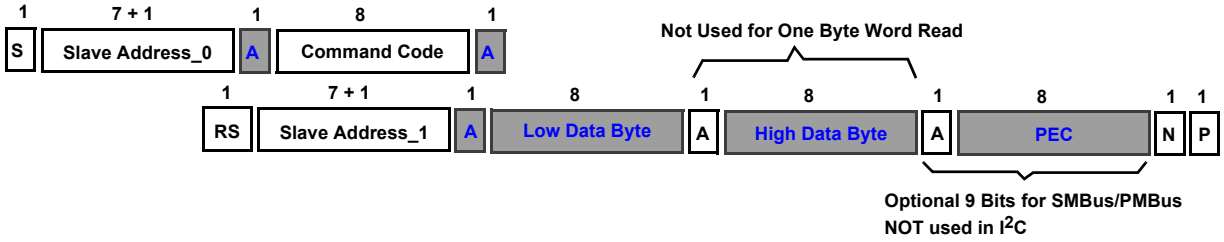
Acknowledge or DATA from Slave, ISL68201

2. Write Byte/Word Protocol



Example command: D0h ENABLE_PFM (one word, High Data Byte, and ACK are not used)

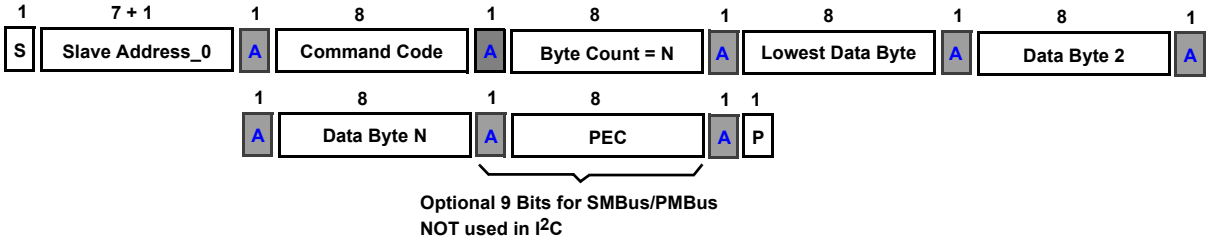
3. Read Byte/Word Protocol



Example command: 8B READ_VOUT (Two words, read voltage of the selected rail).

NOTE: That all Writable commands are read with one byte word protocol.
STOP (P) bit is NOT allowed before the repeated START condition when “reading” contents of a register.

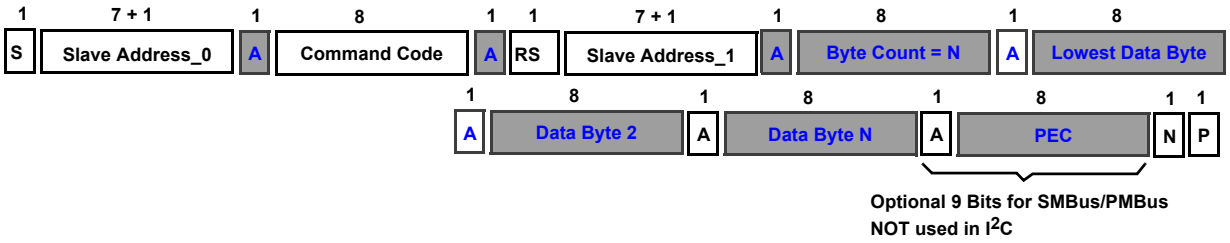
4. Block Write Protocol



Example command: ADh IC_DEVICE_ID (2 Data Byte)

FIGURE 23. SMBus/PMBus/I2C COMMAND PROTOCOL

5. Block Read Protocol



Example command: 8B READ_VOUT (Two words, read voltage of the selected rail).

NOTE: That all Writable commands are read with one byte word protocol.
STOP (P) bit is NOT allowed before the repeated START condition when “reading” contents of a register.

6. Group Command Protocol - No more than one command can be sent to the same Address

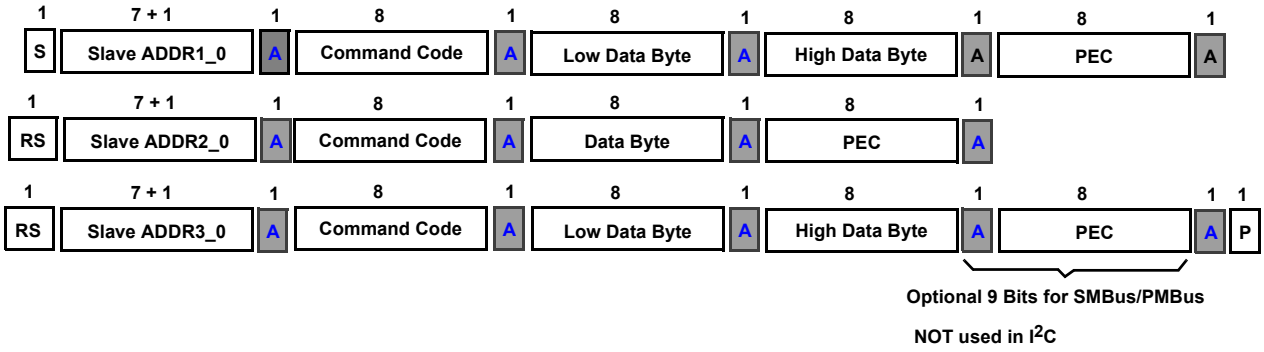


FIGURE 24. SMBus/PMBus/I2C COMMAND PROTOCOL

TABLE 11. SMBus, PMBus, AND I^2C SUPPORTED COMMANDS

COMMAND CODE	ACCESS	WORD LENGTH (BYTE)	DEFAULT VALUE	COMMAND NAME	DESCRIPTION
01h[7:0]	R/W	ONE	80h	OPERATION	VR Enable (depending upon ON_OFF_CONFIG configuration): Bit[7]: 0 = OFF (0-F); 1 = ON (80-8Fh) Bit[6:4] = 0 Bit[3:0] = Don't care
02h[7:0]	R/W	ONE	1Fh	ON_OFF_CONFIG	Configure VR Enabled by OPERATION and/or EN pin: Bit[7:5] = 0 Bit[4] = 1 Bit[3] = OPERATION command Enable 0h = OPERATION command has no control on VR 1h = OPERATION command can turn ON/OFF VR Bit[2] = CONTROL pin Enable 0h = EN Pin has no control on VR 1h = EN pin can turn ON/OFF VR Bit[1] = 1 Bit[0] = 1 Bit[3:2] = 00b = 13h (ALWAYS ON) Bit[3:2] = 01b = 17h (EN controls VR) Bit[3:2] = 10b = 1Bh (OPERATION controls VR) Bit[3:2] = 11b = 1Fh (EN and OPERATION control VR)
03h	SEND BYTE	N/A		CLEAR_FAULTS	Clear faults in status registers
20h[7:0]	R	ONE	19h	VOUT_MODE	Set host format of V_{OUT} command. Always Linear Format: N = -7
21h[2:0]	R/W	TWO	PROG1[7:0]	VOUT_COMMAND	Set output voltage HEX Code = DEC2HEX [ROUND($V_{OUT}/2^{-7}$)]
24h[15:0]	R/W	TWO	VBOOT+500mV	VOUT_MAX	Set maximum output voltage that VR can command (DAC ≤ VOUT_MAX). Linear Format. N = -7 HEX Code = DEC2HEX(ROUNDUP(VOUT_MAX/ 2^{-7})
33h[15:0]	R/W	TWO	PROG3[5:3]	FREQUENCY_SWITCH	Set VR Switching Frequency (In Linear Format) Support 8 options (N = 0): 12Ch = 300kHz; 190h = 400kHz; 1F4h = 500kHz 258h = 600kHz; 2BCh = 700kHz; 352h = 850kHz 3E8h = 1MHz; 5DCh = 1.5MHz* * Very high frequency is not recommended for very high duty cycle applications as the boot capacitor will not has enough time to be charged due to low LGATE ON time.
78h[8:0]	R	ONE		STATUS_BYTE	Fault Reporting; Bit7 = Busy Bit6 = OFF (Reflect current state of operation and ON_OFF_CONFIG registers as well as VR Operation) Bit5 = OVP Bit4 = OCP Bit3 = 0 Bit2 = OTP Bit1 = Bus communication error Bit0 = NONE OF ABOVE (OUTPUT UVP, VOUT_COMAND > VOUT_MAX, or VOUT OPEN SENSE)
88h[15:0]	R	TWO		READ_VIN	Input Voltage (N = - 4, Max = 31.9375V) VIN (V) = HEX2DEC(88 hex data - E000h) * 0.0625V
8Bh[15:0]	R	TWO		READ_VOUT	VR Output Voltage, Resolution = 7.8125mV = 2^{-7} VOUT (V) = HEX2DEC(8B hex data) * 2^{-7}
8Ch[15:0]	R	TWO		READ_IOUT	VR Output Current (N = -3, IMAX = 63.875A) IOUT (A) = HEX2DEC(8C hex data-E800) * 0.125A when IOUT pin voltage = 2.5V at 63.875A load.

TABLE 11. SMBus, PMBus, AND I²C SUPPORTED COMMANDS (Continued)

COMMAND CODE	ACCESS	WORD LENGTH (BYTE)	DEFAULT VALUE	COMMAND NAME	DESCRIPTION
8Dh[15:0]	R	TWO		READ_TEMP	VR Temperature TEMP (°C) = 1/{ln[Rup*HEX2DEC(8D hex data)/(511 - HEX2DEC(8D hex data)/RNTC(at +25°C)]/Beta + 1/298.15} -273.15
98h[7:0]	R	ONE	02h	PMBUS_REVISION	Indicates PMBus Revision 1.2
AD[15:0]	BLOCK R	TWO	8201h	IC_DEVICE_ID	ISL68201 Device ID
AE[15:0]	BLOCK R	TWO	0003h	IC_DEVICE_REVISION	ISL68201 Device Revision
D0[0:0]	R/W	ONE	PROG2[7:7]	ENABLE_PFM	PFM OPERATION 0h = PFM Enabled (DCM at light load) 1h = PFM Disabled (always CCM mode)
D1[1:0]	R/W	ONE	PROG2[6:5]	TEMP_COMP	Thermal Compensation: 0h = 30°C; 01h = 15°C; 02h = 5°C; 03h = OFF
D2[0:0]	R/W	ONE	PROG3[7:7]	ENABLE_ULTRASONIC	Ultrasonic PFM Enable 0h = 25kHz Clamp Disabled 1h = 25kHz Clamp Enabled
D3[0:0]	R/W	ONE	PROG3[6:6]	OCP_BEHAVIOR	Set latch or infinite retry for OCP fault: 0h = Retry every 9ms; 01 = Latch-OFF
D4[2:0]	R/W	ONE	PROG3[2:0]	AV_GAIN	R4 AV GAIN (PROG4, AV Gain Multiplier = 2x) 0h = 84; 1h = 73; 2h = 61; 3h = 49 4h = 38; 5h = 26; 6h = 14; 7h = 2 R4 AV GAIN (PROG4, AV Gain Multiplier = 1x) 0h = 42; 1h = 36.5; 2h = 30.5; 3h = 29.5 4h = 19; 5h = 13; 6h = 7; 7h = 1
D5[2:0]	R/W	ONE	PROG4[7:5]	RAMP_RATE	Soft-Start and Margining DVID Rate (mV/µs) 0h = 1.25; 1h = 2.5; 2h = 5; 3h = 10; 4h = 0.078; 5h = 0.157 6h = 0.315; 7h = 0.625;
D6[1:0]	R/W	ONE	PROG4[4:3]	SET_RR	Set RR 0h = 200k; 01h = 400k; 02h = 600k; 03h = 800k
DC[7:0]	R	ONE		READ_PROG1	Read PROG1
DD[7:0]	R	ONE		READ_PROG2	Read PROG2
DE[7:0]	R	ONE		READ_PROG3	Read PROG3
DF[7:0]	R	ONE		READ_PROG4	Read PROG4

NOTE: Serial bus communication is valid 5.5m (typically, worst 6.5ms) after V_{CC}, V_{IN}, 7VLDO, and PVCC above POR. The telemetry update rate is 108µs.

R4 Modulator

The R4 modulator is an evolutionary step in R3 technology. Like R3, the R4 modulator is a linear control loop and variable frequency control during load transients to eliminate beat frequency oscillation at the switching frequency and maintains the benefits of current-mode hysteretic controllers. In addition, the R4 modulator reduces regulator output impedance and uses accurate referencing to eliminate the need for a high-gain voltage amplifier in the compensation loop. The result is a topology that can be tuned to voltage-mode hysteretic transient speed while maintaining a linear control model and removes the need for any compensation. This greatly simplifies the regulator design for customers and reduces external component cost.

STABILITY

The removal of compensation derives from the R4 modulator's lack of need for high DC gain. In traditional architectures, high DC gain is achieved with an integrator in the voltage loop. The integrator introduces a pole in the open-loop transfer function at low frequencies. That, combined with the double-pole from the output L/C filter, creates a three pole system that must be compensated to maintain stability.

Classic control theory requires a single-pole transition through unity gain to ensure a stable system. Current-mode architectures (includes peak, peak-valley, current-mode hysteric, R3, and R4) generate a zero at or near the L/C resonant point, effectively canceling one of the system's poles. The system still contains two poles, one of which must be canceled with a zero before unity gain crossover to achieve stability.

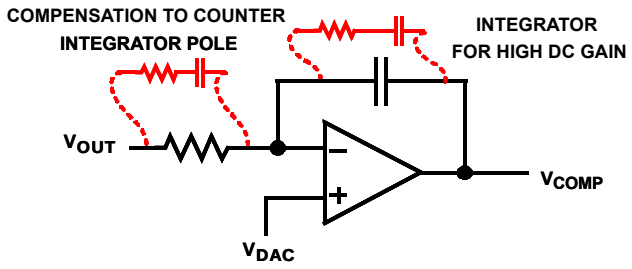


FIGURE 25. CLASSICAL INTEGRATOR ERROR-AMPLIFIER CONFIGURATION

Figure 25 illustrates the classic integrator configuration for a voltage loop error amplifier. While the integrator provides the high DC gain required for accurate regulation in traditional technologies, it also introduces a low-frequency pole into the control loop. Figure 26 shows the open-loop response that results from the addition of an integrating capacitor in the voltage loop. The compensation components found in Figure 25 are necessary to achieve stability.

Because R4 does not require a high-gain voltage loop, the integrator can be removed, reducing the number of inherent poles in the loop to two. The current-mode zero continues to cancel one of the poles, ensuring a single-pole crossover for a wide range of output filter choices. The result is a stable system with no need for compensation components or complex equations to properly tune the stability.

Figure 27 shows the R4 error-amplifier that does not require an integrator for high DC gain to achieve accurate regulation. The result to the open loop response can be seen in Figure 28.

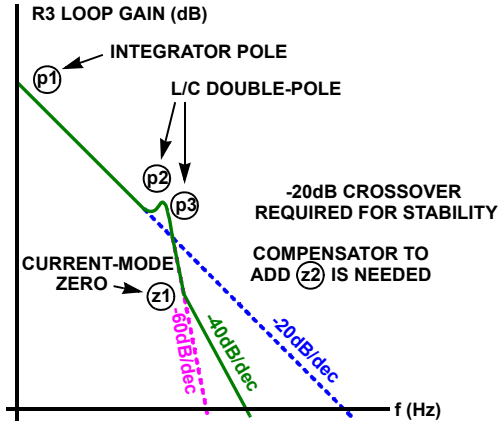


FIGURE 26. UNCOMPENSATED INTEGRATOR OPEN-LOOP RESPONSE

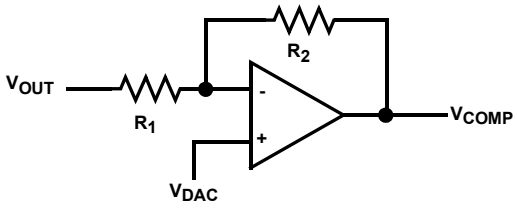


FIGURE 27. NON-INTEGRATED R4 ERROR-AMPLIFIER CONFIGURATION

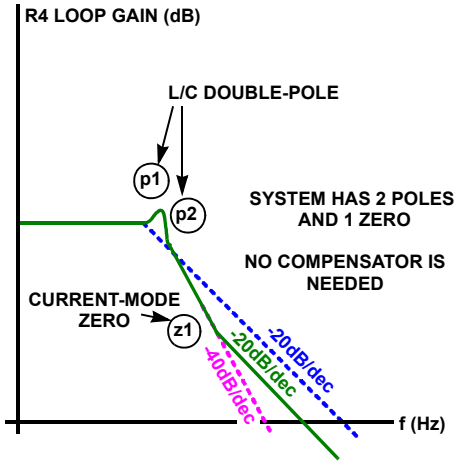


FIGURE 28. UNCOMPENSATED R4 OPEN-LOOP RESPONSE

TRANSIENT RESPONSE

In addition to requiring a compensation zero, the integrator in traditional architectures also slows system response to transient conditions. The change in COMP voltage is slow in response to a rapid change in output voltage. If the integrating capacitor is removed, COMP moves as quickly as V_{OUT}, and the modulator immediately increases or decreases switching frequency to recover the output voltage.

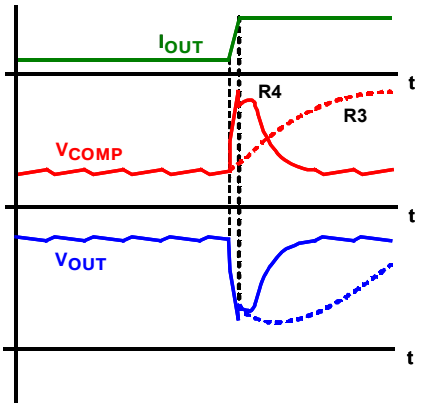


FIGURE 29. R3 vs R4 IDEALIZED TRANSIENT RESPONSE

The dotted red and blue lines in Figure 29 represent the time delayed behavior of V_{OUT} and V_{COMP} in response to a load transient when an integrator is used. The solid red and blue lines illustrate the increased response of R4 in the absence of the integrator capacitor.

To optimize transient response and improve phase margin for very wide range applications, the ISL68201 integrates selectable AV and RR options that move the DC gain and z1 point, as shown in Figure 28. However, the defaulted AV gain of 42 and RR of 200kΩ can cover many cases and provides sufficient gain and phase margin. For some extreme cases, lower AV gain and bigger RR values are needed to provide a better phase margin and improve transient ringback. The optimal choice AV and RR can be obtained, by simple monitoring transient response when adjusting AV and RR values through the serial bus.

General Application Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to design a single-phase buck converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts.

Output Filter Design

The output inductors and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase nodes. The output filter also must provide the transient energy until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter limits the system transient response. The output capacitor must supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI; the load current slew rate, di/dt; and the maximum allowable output voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount, as shown in Equation 15:

$$\Delta V \approx \Delta I \cdot ESR + \frac{ESL}{L_{OUT}} \cdot V_{IN} + \frac{1}{C_{OUT}} \cdot \frac{\Delta I}{8 \cdot N \cdot f_{SW}} \quad \text{(EQ. 15)}$$

$$\Delta I = \frac{V_{OUT} \cdot (1 - D)}{L_{OUT} \cdot f_{SW}}$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high-frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation. The ESR of the bulk capacitors also creates the majority of the output voltage ripple. As the bulk capacitors sink and source the inductor AC ripple current, a voltage develops across the bulk capacitor ESR equal to $I_{L(P-P)}$ (ESR).

Thus, after the output capacitors are selected, the maximum allowable ripple voltage, $V_{P-P(MAX)}$, determines the lower limit on the inductance, as shown in Equation 16.

$$L_{OUT} \geq ESR \cdot \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{f_{SW} \cdot V_{IN} \cdot V_{P-P(MAX)}} \quad \text{(EQ. 16)}$$

Because the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Equation 17 gives the upper limit on L for cases when the trailing edge of the current transient causes a greater output to voltage deviation than the leading edge. Equation 18 addresses the leading edge. Normally, the trailing edge dictates the selection of L because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In Equations 17 and 18, L is the per-channel inductance and C is the total output capacitance.

$$L_{OUT} \leq \frac{2 \cdot C \cdot V_{OUT}}{(\Delta I)^2}\left[\Delta V_{MAX} - (\Delta I \cdot ESR)\right] \quad \text{(EQ. 17)}$$

$$L_{OUT} \leq \frac{1.25 \cdot C}{(\Delta I)^2}\left[\Delta V_{MAX} - (\Delta I \cdot ESR)\right]\left(V_{IN} - V_{OUT}\right) \quad \text{(EQ. 18)}$$

Input Capacitor Selection

The input capacitors are responsible for sourcing the AC component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the AC component of the current drawn by the upper MOSFETs, which is related to duty cycle and the number of active phases. The input RMS current can be calculated with Equation 19.

$$I_{IN,RMS} = \sqrt{(D - D^2) \cdot Io^2 + \frac{D}{12} \cdot (\Delta I)^2} \quad \text{(EQ. 19)}$$

Use Figure 30 on page 29 to determine the input capacitor RMS current requirement given the duty cycle, maximum sustained output current (I_O), and the ratio of the per-phase peak-to-peak inductor current ($I_{L(P-P)}$ to I_O). Select a bulk capacitor with a ripple current rating, which will minimize the total number of input capacitors required to support the RMS current calculated. The voltage rating of the capacitors should also be at least 1.25 times greater than the maximum input voltage.

Low capacitance, high-frequency ceramic capacitors are needed in addition to the bulk capacitors to suppress leading and falling edge voltage spikes. The result of the high current slew rates produced by the upper MOSFETs turn on and off requires low ESL ceramic capacitors, which should be placed as close as possible to each upper MOSFET drain to minimize board parasitic impedances and maximize noise suppression.

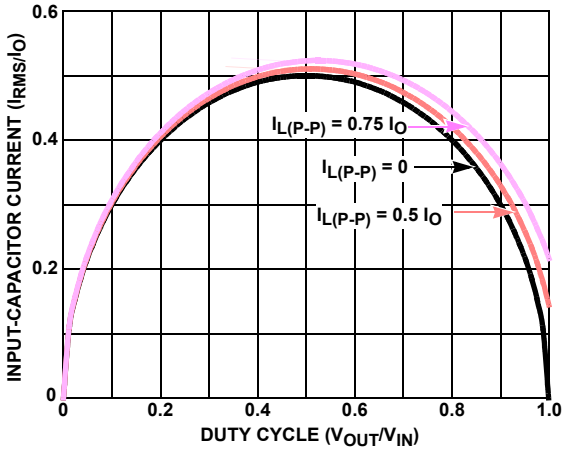


FIGURE 30. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR SINGLE-PHASE CONVERTER

Design and Layout Considerations

To ensure a first pass design, the schematics design must be done right with correct pinout and net names, and the board must be carefully laid out.

As a general rule, power layers should be close together, either on the top or bottom of the board, with the weak analog or logic signal layers on the opposite side of the board or internal layers. The ground-plane layer should be in between power layers and the signal layers to provide shielding, often the layer below the top and the layer above the bottom should be the ground layers.

There are two sets of components in a DC/DC converter, the power components and the small signal components. The power components are the most critical because they switch large amounts of energy. The small signal components connect to sensitive nodes or supply critical bypassing current and signal coupling.

The power components should be placed first and these include MOSFETs, input and output capacitors, and the inductor. Keeping the distance between the power train and the control IC short helps keep the gate drive traces short. These drive signals include the LGATE, UGATE, GND, PHASE, and BOOT.

When placing MOSFETs, keep the source of the upper MOSFETs and the drain of the lower MOSFETs as close as thermally possible. Input high-frequency capacitors should be placed close to the drain of the upper MOSFETs and the source of the lower MOSFETs. Place the output inductor and output capacitors between the MOSFETs and the load. High frequency output decoupling capacitors (ceramic) should be placed as close as possible to the decoupling target, making use of the shortest connection paths to any internal planes. Place the components in such a way that the area under the IC has less noise traces with high dV/dt and di/dt, such as gate signals, phase node signals, and VIN plane.

Tables 12 and 13 provide a design and layout checklist that the designer can reference.

TABLE 12. DESIGN AND LAYOUT CHECKLIST

PIN NAME	NOISE SENSITIVITY	DESCRIPTION
EN	YES	There is an internal 1µs filter. Decoupling the capacitor is NOT needed, but if needed, use a low time constant one to avoid too large a shutdown delay.
VIN	YES	Place 16V+ X7R 1µF in close proximity to the pin and the system ground plane.
7VLDO	YES	Place 10V+ X7R 1µF in close proximity to the pin and the system ground plane.
VCC	YES	Place X7R 1µF in close proximity to the pin and the system ground plane.
SCL, SDA	YES	50kHz to 1.25MHz signal when the SMBus, PMBus, or I^2C is sending commands. Pairing up with SALERT and routing carefully back to SMBus, PMBus or I^2C master. 20 mils spacing within SDA, SALERT, and SCL; and more than 30 mils to all other signals. Refer to the SMBus, PMBus or I^2C design guidelines and place proper terminated (pull-up) resistance for impedance matching. Tie them to GND when not used.
SALERT	NO	Open-drain and high dv/dt pin during transitions. Route it in the middle of SDA and SCL. Tie it to GND when not used.
PGOOD	NO	Open-drain pin. Tie it to GND when not used.
RGND, VSEN	YES	Differential pair routed to the remote sensing points with sufficient decoupling ceramics capacitors and not across or go above/under any switching nodes (BOOT, PHASE, UGATE, LGATE) or planes (VIN, PHASE, VOUT) even though they are not in the same layer. At least 20 mils spacing from other traces. DO NOT share the same trace with CSRTN.
CSRTN	YES	Connect to the output rail side of the output inductor or current sensing resistor pin with a series resistor in close proximity to the pin. The series resistor sets the current gain and should be within 40Ω and 3.5kΩ. Decoupling (~ 0.1µF/X7R) on the output end (not the pin) is optional and might be required for long sense trace and a poor layout (see Figures 9 and 10).
CSEN	YES	Connect to the phase node side of the output inductor or current sensing resistor pin with L/DCR or ESL/R_{SEN} matching network in close proximity to CSEN and CSRTN pins. Differentially routing back to the controller with at least 20 mils spacing from other traces. Should NOT cross or go above/under the switching nodes [BOOT, PHASE, UGATE, LGATE], and power planes (VIN, PHASE, VOUT) even though they are not in the same layer.

TABLE 12. DESIGN AND LAYOUT CHECKLIST (Continued)

PIN NAME	NOISE SENSITIVITY	DESCRIPTION
NTC	YES	Place NTC 10k (Murata, NCP15XH103J03RC, β = 3380) in close proximity to the output inductor's output rail, not close to MOSFET side (see Figure 19); the return trace should be 20 mils away from other traces. Place 1.54kΩ pull-up and decoupling capacitor (typically 0.1µF) in close proximity to the controller. The pull-up resistor should be exactly tied to the same point as VCC pin, not through an RC filter. If not used, connect this pin to VCC.
IOUT	YES	Scale R so that the IOUT pin voltage is 2.5V at 63.875A load. Place R and C in general proximity to the controller. The time constant of RC should be sufficient as an averaging function (>200µs) for the digital IOUT. An external pull-up resistor to VCC placeholder is recommended to cancel I_{OUT} offset at 0A load. See "I_{OUT} Calibration" on page 19
PROG1-4	NO	The resistor divider must be referenced to VCC pin and the system ground (GND); they can be placed anywhere. DO NOT use decoupling capacitors on these pins.
GND	YES	Directly connect to a low noise area of the system ground. The GND PAD should use at least four vias. Separate analog ground and power ground with a 0Ω resistor is highly NOT recommended.
FCCM	NO	DO NOT place it across or under external components of the controller. Keep it at least 20 mils away from sensitive nodes.
PWM	NO	DO NOT place it across or under external components of the controller. Keep it at least 20 mils away from any other traces.
LGIN	NO	Keep it at least 20 mils away from sensitive nodes. A series 100Ω resistor to low-side gate signal is required for noise attenuation.
PVCC	YES	Place X7R 4.7µF in proximity to the PVCC pin and the system ground plane.

TABLE 13. TOP LAYOUT TIPS

NUMBER	DESCRIPTION
1	The layer next to controller (top or bottom) should be a ground layer. Separate analog ground and power ground with a 0Ω resistor is highly NOT recommended. Directly connect GND PAD to low noise area of the system ground with at least four vias.
2	Never place controller and its external components above or under VIN plane or any switching nodes.
3	Never share CSRTN and VSEN on the same trace.
4	Place the input rail decoupling ceramic capacitors closely to the high-side FET on the same layer as possible. Never use only one via and a trace connect the input rail decoupling ceramics capacitors; must connect to VIN and GND planes.
5	Place all decoupling capacitors in close proximity to the controller and the system ground plane.
6	Connect remote sense (VSEN and RGND) to the load and ceramic decoupling capacitors nodes; never run this pair above or below switching noise plane.
7	Always double check critical component pinout and their respective footprints.

Voltage Regulator Design Materials

To support VR design and layout, Intersil also developed a set of tools and evaluation boards, as listed in Table 14 and Ordering Information on page 5. Contact Intersil's local office or field support at www.intersil.com/ask for the latest available information.

TABLE 14. AVAILABLE DESIGN ASSISTANCE MATERIALS

ITEM	DESCRIPTION
1	SMBus/PMBus/I^2C communication tool with the PowerNavigator GUI.
2	Evaluation board schematics in OrCAD format and layout in Allegro format. See Ordering Information on page 5 for details.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Oct 17, 2017	FN8696.4	Updated Pin 11 and 12 descriptions on page 6.
Sep 25, 2017	FN8696.3	Updated LGIN pin description. Updated Figure 4, changed “10.2V/9.24V” to “10.08V/9.12V”. Updated 3Fh R_{UP} value in Table 3. Replaced entire paragraph on page 11. Added units to R = 348Ω on page 17 above Figure 11. On page 28 last sentence in paragraph in left column changed “$I_{C(P-P)}$” to “$I_{L(P-P)}$”.
Aug 29, 2017	FN8696.2	For Figures 1 and 2 on page 3, added a resistor to the CSRTN circuit. On page 1, updated the Related Literature section to current standards. Added three demonstration boards to the Ordering Information table on page 5. Removed Table 15 on page 30 because the demonstration board information is in the Ordering Information section.
Mar 7, 2016	FN8696.1	Removed unreleased parts from Table 1.
Mar 2, 2016	FN8696.0	Initial release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, please see the respective product information page found at www.intersil.com.

For a listing of definitions and abbreviations of common terms used in our documents, visit www.intersil.com/glossary.

You can report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

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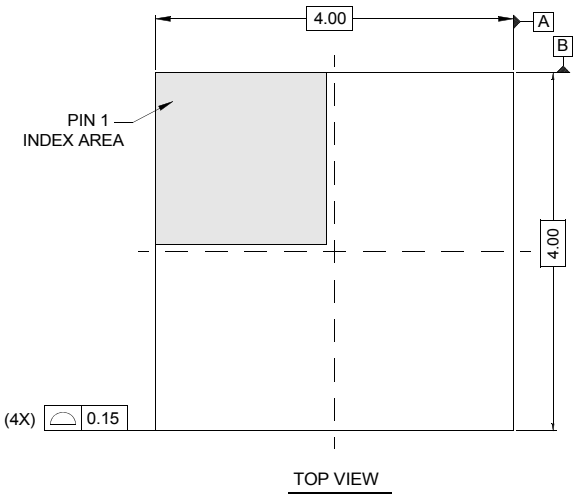
Package Outline Drawing

For the most recent package outline drawing, see L24.4x4C.

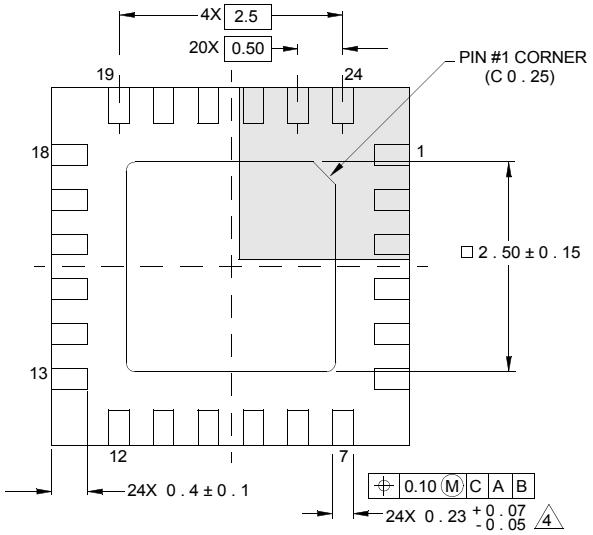
L24.4x4C

24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

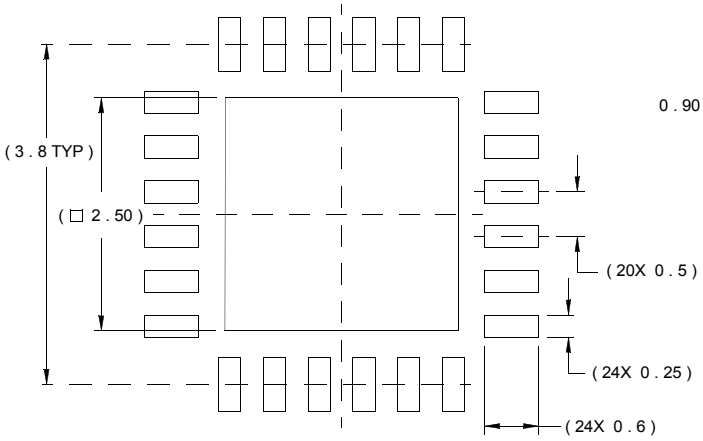
Rev 2, 10/06



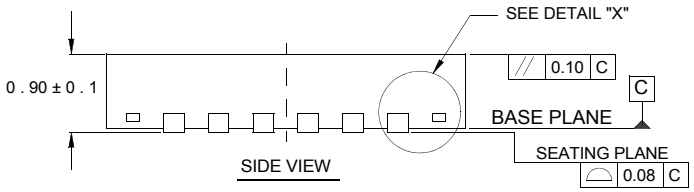
TOP VIEW



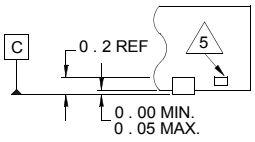
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.