MK2727
Low Cost 27 MHz VCXO

Description

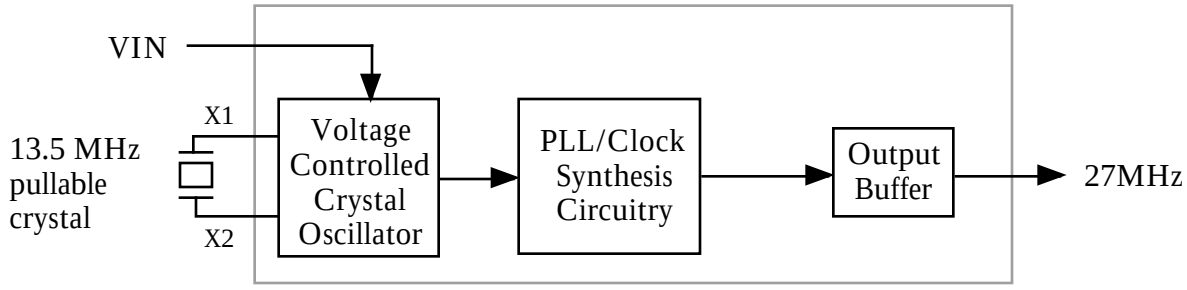
The MK2727 is MicroClock's lowest cost, low jitter, high performance VCXO and PLL clock synthesizer designed to replace expensive 27MHz VCXOs. The on-chip Voltage Controlled Crystal Oscillator accepts a 0 to 3V input voltage to cause the output clocks to vary by ±100 ppm. Using MicroClock's patented VCXO and analog Phase-Locked Loop (PLL) techniques, the device uses an inexpensive external 13.5 MHz pullable crystal input to produce a 27 MHz output clock.

MicroClock manufactures the largest variety of Set-Top Box and multimedia clock synthesizers for all applications. If more clock outputs are needed, see the MK2731 or MK277x family of parts. Consult MicroClock to eliminate VCXOs, crystals and oscillators from your board.

Features

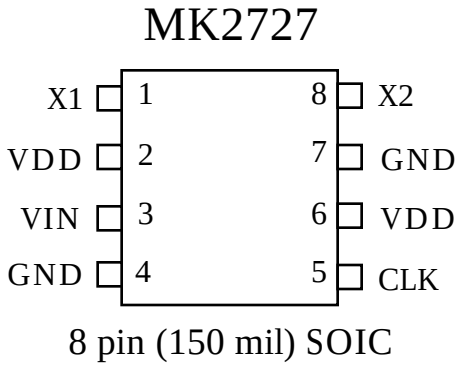
- Packaged in 8 pin narrow SOIC
- Uses an inexpensive 13.500 MHz external crystal
- On-chip VCXO (patented) with pull range of 200ppm (minimum)
- VCXO tuning voltage of 0 to 3V
- 25mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- 5V operating voltage

Block Diagram



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Pin Assignment



8 pin (150 mil) SOIC

Pin Descriptions

Number	Name	Description
1	X1	Crystal connection. Connect to a pullable 13.5 MHz crystal.
2	VDD	VDD. Connect to +5V.
3	VIN	Voltage input to VCXO. Zero to 3V analog input which controls the frequency of the VCXO.
4	GND	Connect to ground.
5	CLK	27 MHz clock output.
6	VDD	VDD. Connect to +5V.
7	GND	Connect to ground.
8	X2	Crystal connection. Connect to a pullable 13.5 MHz crystal.

Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (note 1)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 5.0V unless noted)					
Operating Voltage, VDD		4.75		5.25	V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
Output High Voltage, VOH, CMOS level	IOH=-8mA	VDD-0.4			V
Operating Supply Current, IDD	No Load		20		mA
Short Circuit Current			±100		mA
VIN, VCXO control voltage		0		3	V
AC CHARACTERISTICS (VDD = 5.0V unless noted)					
Input Crystal Frequency			13.50000		MHz
Input Crystal Accuracy				±30	ppm
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle	At 1.4V	40	50	60	%
Maximum Absolute Jitter, short term			200		ps
27 MHz output pullability, note 2	0V ≤ VIN ≤ 3V	±100			ppm

Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. With a MicroClock approved pullable crystal.

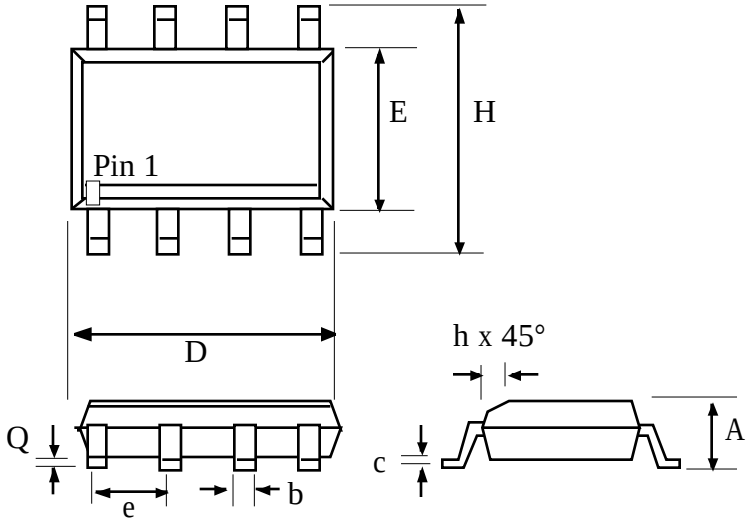
External Components

The MK2727 requires a minimum number of external components for proper operation. A decoupling capacitor of 0.1µF should be connected between VDD and GND on pins 2 and 4, as close to the MK2727 as possible. A series termination resistor of 33Ω may be used for the clock output. The input crystal must be connected as close to the chip as possible. The input crystal should be a parallel mode, pullable, AT cut, 13.5MHz, with 14pF load capacitance. Consult MicroClock for recommended suppliers. IMPORTANT - read application note MAN05 before laying out the PCB.

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Package Outline and Package Dimensions

8 pin SOIC



	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.055	0.068	1.397	1.7272
b	0.013	0.019	0.330	0.483
D	0.185	0.200	4.699	5.080
E	0.150	0.160	3.810	4.064
H	0.225	0.245	5.715	6.223
e	.050 BSC		1.27 BSC	
h		0.015		0.381
Q	0.004	0.01	0.102	0.254

Ordering Information

Part/Order Number	Marking	Shipping packaging	Package	Temperature
MK2727S	MK2727S	tubes	8 pin SOIC	0-70°C
MK2727STR	MK2727S	tape and reel	8 pin SOIC	0-70°C

CHANGE HISTORY

Version	Date first published	Status	Comments
A	12/12/96	Advance	Original
B	12/2/97	Released	Updated logo & address. Corrected pkg height.

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