

FEATURES

- 1.8 V analog/digital core**
- Integrated 12-channel vertical driver (V-driver)**
- 12-bit, 60 MHz analog-to-digital converter (ADC)**
- Complete on-chip timing generator**
- Precision Timing* core with ~260 ps resolution**
- Correlated double sampler (CDS) with variable gain**
- 0 dB to 36 dB, 10-bit variable gain amplifier (VGA)**
- Black level clamp with variable level control**
- On-chip 3 V horizontal and reset gate (RG) drivers**
- 2-phase and 4-phase H-clock modes**
- Electronic and mechanical shutter support**
- On-chip 1.8 V LDO**
- On-chip driver for external crystal**
- On-chip sync generator with external sync input**

APPLICATIONS

High speed digital cameras

GENERAL DESCRIPTION

The **ADDI9020** is a complete 60 MHz front-end solution for digital still cameras and other charge-coupled device (CCD) imaging applications. The **ADDI9020** includes the analog front end (AFE), a fully programmable timing generator (TG), and a 12-channel V-driver. A *Precision Timing*® core allows adjustment of high speed clocks with approximately 260 ps resolution at 60 MHz operation.

The on-chip V-driver supports up to 12 channels for use with multifield CCDs.

The analog front end includes black level clamping, CDS, VGA, and a 12-bit ADC. The timing generator and V-driver provide all the necessary CCD clocks: RG, H-clocks, vertical clocks, sensor gate pulses, a substrate clock, and substrate bias control. The internal registers are programmed using a 3-wire serial interface.

Packaged in a 7 mm × 7 mm CSP_BGA, the **ADDI9020** is specified over an operating temperature range of -25°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

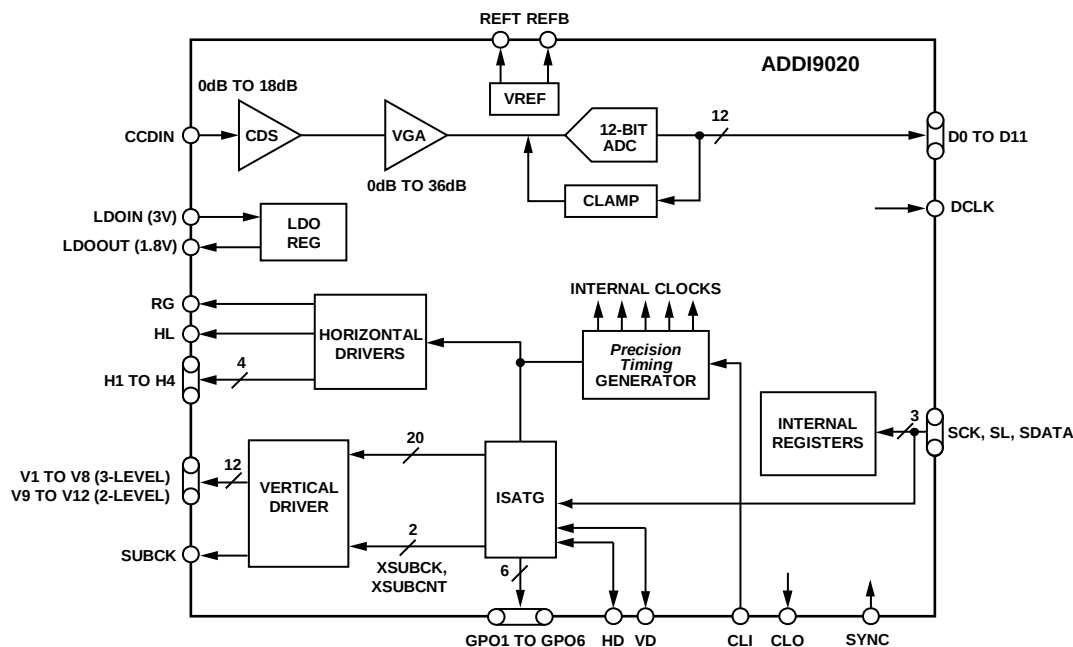


Figure 1.

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For more information about the **ADDI9020**, contact Analog Devices, Inc. via email at: afe.ccd@analog.com

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