

Document Title**512Kx16 bit Low Power CMOS Static RAM****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	June 18, 1999	Advance
1.0	Finalize - Adopt New Code system. - Improve V_{IN} , V_{OUT} max. on ABSOLUTE MAXIMUM RATINGS from 7.0V to $V_{CC}+0.5V$.	February 29, 2000	Final
1.01	Errata correction	April 17, 2000	Final

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512Kx16 bit Low Power CMOS Static RAM

FEATURES

- Process Technology: TFT
- Organization: 512K x16
- Power Supply Voltage: 4.5~5.5V
- Low Data Retention Voltage: 2.0V(Min)
- Three state output and TTL Compatible
- Package Type: 44-TSOP2-400F/R

GENERAL DESCRIPTION

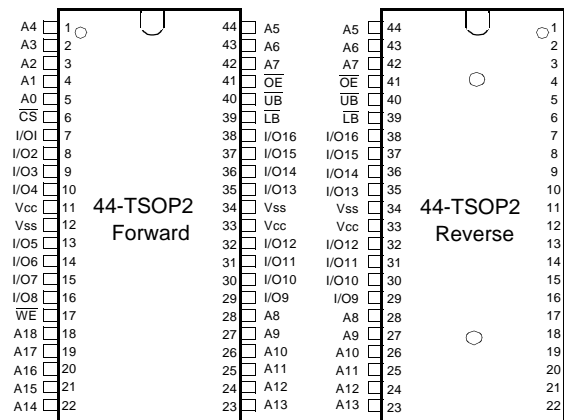
The K6T8016C3M families are fabricated by SAMSUNG's advanced CMOS process technology. The families support industrial operating temperature ranges for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I _{SB1} , Max)	Operating (I _{CC2} , Max)	
K6T8016C3M-B	Commercial(0~70°C)	4.5~5.5V	55 ¹⁾ /70ns	50μA	90mA	44-TSOP2-400F/R
K6T8016C3M-F	Industrial(-40~85°C)			80μA		

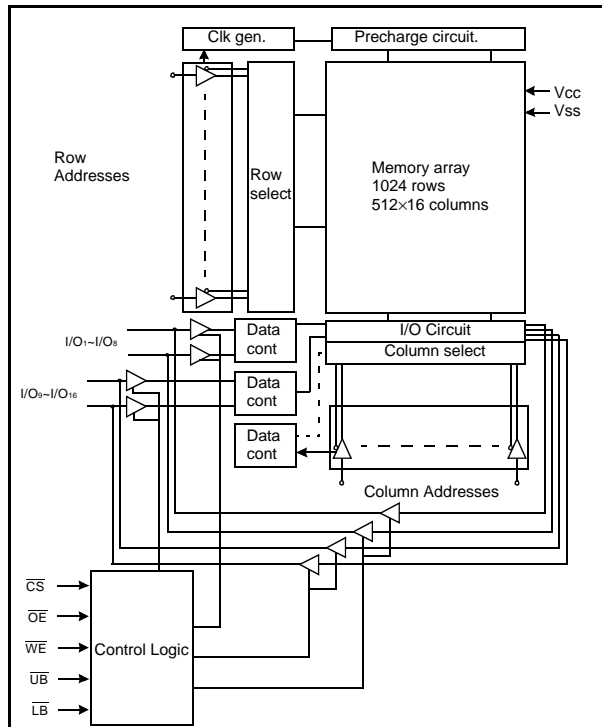
1. The parameter is measured with 50pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
\overline{CS}	Chip Select Input	Vcc	Power
\overline{OE}	Output Enable Input	Vss	Ground
\overline{WE}	Write Enable Input	\overline{UB}	Upper Byte(I/O _{9~16})
A0~A18	Address Inputs	\overline{LB}	Lower Byte(I/O _{1~8})
I/O _{1~I/O16}	Data Inputs/Outputs		

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
K6T8016C3M-TB55 K6T8016C3M-TB70	44-TSOP2-F, 55ns, Low Low Power 44-TSOP2-F, 70ns, Low Low Power	K6T8016C3M-TF55 K6T8016C3M-TF70	44-TSOP2-F, 55ns, Low Low Power 44-TSOP2-F, 70ns, Low Low Power
K6T8016C3M-RB55 K6T8016C3M-RB70	44-TSOP2-R, 55ns, Low Low Power 44-TSOP2-R, 70ns, Low Low Power	K6T8016C3M-RF55 K6T8016C3M-RF70	44-TSOP2-R, 55ns, Low Low Power 44-TSOP2-R, 70ns, Low Low Power

FUNCTIONAL DESCRIPTION

\overline{CS}	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O ₁₋₈	I/O ₉₋₁₆	Mode	Power
H	X	X	X	X	High-Z	High-Z	Deselected	Standby
L	H	H	X	X	High-Z	High-Z	Output Disabled	Active
L	X	X	H	H	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	L	H	L	L	Dout	Dout	Word Read	Active
L	X	L	L	H	Din	High-Z	Lower Byte Write	Active
L	X	L	H	L	High-Z	Din	Upper Byte Write	Active
L	X	L	L	L	Din	Din	Word Write	Active

Note: X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to V _{ss}	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5V	V	-
Voltage on V _{CC} supply relative to V _{ss}	V _{CC}	-0.3 to 7.0	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	K6T8016C3M-B
		-40 to 85	°C	K6T8016C3M-F

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	-	V _{CC} +0.5 ²⁾	V
Input low voltage	V _{IL}	-0.5 ³⁾	-	0.8	V

Note:

1. Commercial Product: T_A=0 to 70°C, otherwise specified.

Industrial Product: T_A=-40 to 85°C, otherwise specified.

2. Overshoot: V_{CC}+3.0V in case of pulse width ≤30ns.

3. Undershoot: -3.0V in case of pulse width ≤30ns.

4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

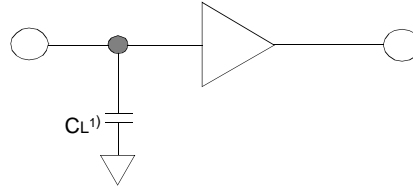
DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA	
Output leakage current	I _{LO}	$\overline{CS}=V_{IH}$, $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA	
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS}=V_{IL}$, $\overline{WE}=V_{IH}$, V _{IN} =V _{IH} or V _{IL}	-	-	12	mA	
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA, $\overline{CS} \leq 0.2V$, V _{IN} ≤ 0.2V or V _{IN} ≥ V _{CC} -0.2V	-	-	15	mA	
	I _{CC2}	Cycle time=Min, I _{IO} =0mA, 100% duty, $\overline{CS}=V_{IL}$, V _{IN} =V _{IL} or V _{IH}	-	-	90	mA	
Output low voltage	V _{OL}	I _{OL} = 2.1mA	-	-	0.4	V	
Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4	-	-	V	
Standby Current(TTL)	I _{SB}	$\overline{CS}=V_{IH}$, Other inputs=V _{IH} or V _{IL}	-	-	3	mA	
Standby Current(CMOS)	I _{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, Other inputs=0~V _{CC}	K6T8016C3M-B	-	-	50	μA
			K6T8016C3M-F	-	-	80	

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V
 Input rising and falling time: 5ns
 Input and output reference voltage: 1.5V
 Output load(see right): $C_L=100\text{pF}+1\text{TTL}$
 $C_L=50\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

AC CHARACTERISTICS ($V_{CC}=4.5\sim 5.5\text{V}$, Commercial product: $T_A=0$ to 70°C , Industrial product: $T_A=-40$ to 85°C)

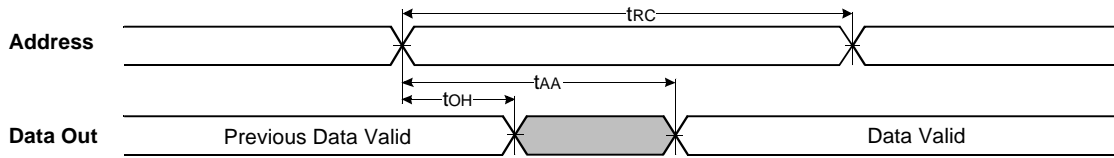
Parameter List		Symbol	Speed Bins				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	55	-	70	-	ns
	Address access time	t _{AA}	-	55	-	70	ns
	Chip select to output	t _{CO}	-	55	-	70	ns
	Output enable to valid output	t _{OE}	-	25	-	35	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	ns
	$\overline{\text{LB}}, \overline{\text{UB}}$ enable to low-Z output	t _{BLZ}	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ}	0	20	0	25	ns
	Output Disable to High-Z Output	t _{OHZ}	0	20	0	25	ns
	Output hold from address change	t _{OH}	10	-	10	-	ns
	$\overline{\text{LB}}, \overline{\text{UB}}$ valid to data output	t _{BA}	-	25	-	35	ns
$\overline{\text{UB}}, \overline{\text{LB}}$ disable to high-Z output	t _{BHZ}	0	20	0	25	ns	
Write	Write cycle time	t _{WC}	55	-	70	-	ns
	Chip select to end of write	t _{CW}	45	-	60	-	ns
	Address set-up time	t _{AS}	0	-	0	-	ns
	Address valid to end of write	t _{AW}	45	-	60	-	ns
	Write pulse width	t _{WP}	40	-	55	-	ns
	Write recovery time	t _{WR}	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	20	0	25	ns
	Data to write time overlap	t _{DW}	20	-	30	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	ns
$\overline{\text{LB}}, \overline{\text{UB}}$ valid to end of write	t _{BW}	45	-	60	-	ns	

DATA RETENTION CHARACTERISTICS

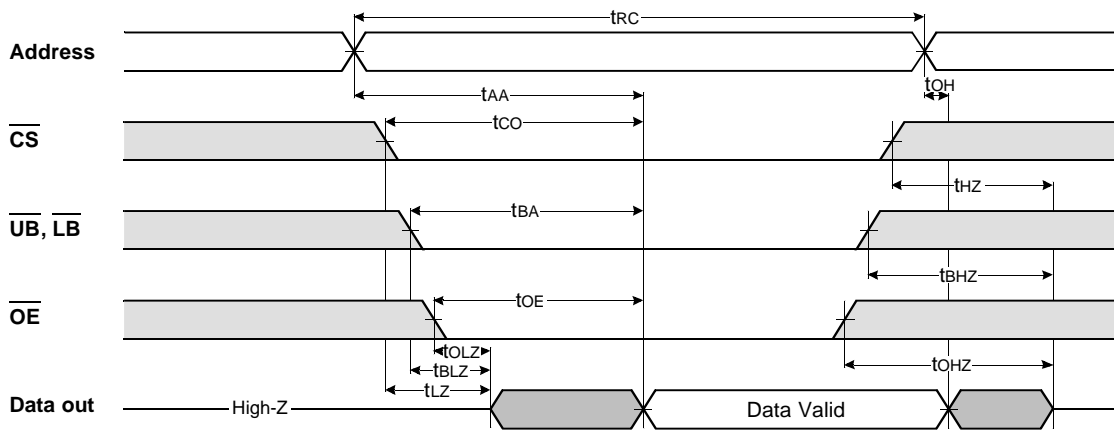
Item	Symbol	Test Condition	Min	Typ	Max	Unit	
V _{CC} for data retention	V _{DR}	$\overline{\text{CS}} \geq V_{CC}-0.2\text{V}$	2.0	-	5.5	V	
Data retention current	I _{DR}	$V_{CC}=3.0\text{V}, \overline{\text{CS}} \geq V_{CC}-0.2\text{V}$ $\overline{\text{CS}} \geq V_{CC}-0.2\text{V}$	K6T8016C3M-B	-	-	20	μA
			K6T8016C3M-F	-	-	30	
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ms	
Recovery time	t _{RDR}		5	-	-		

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, \overline{UB} or/and $\overline{LB}=V_{IL}$)



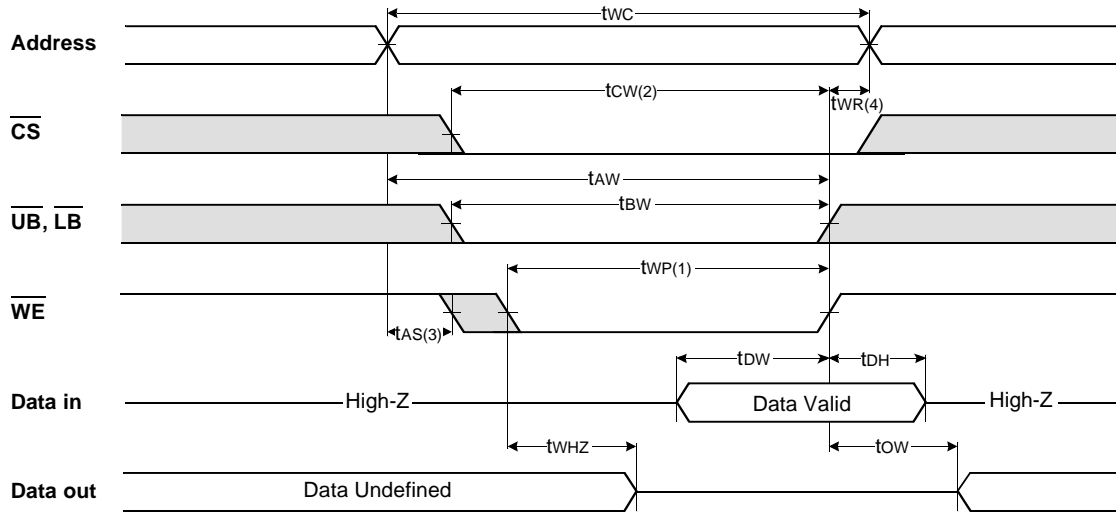
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



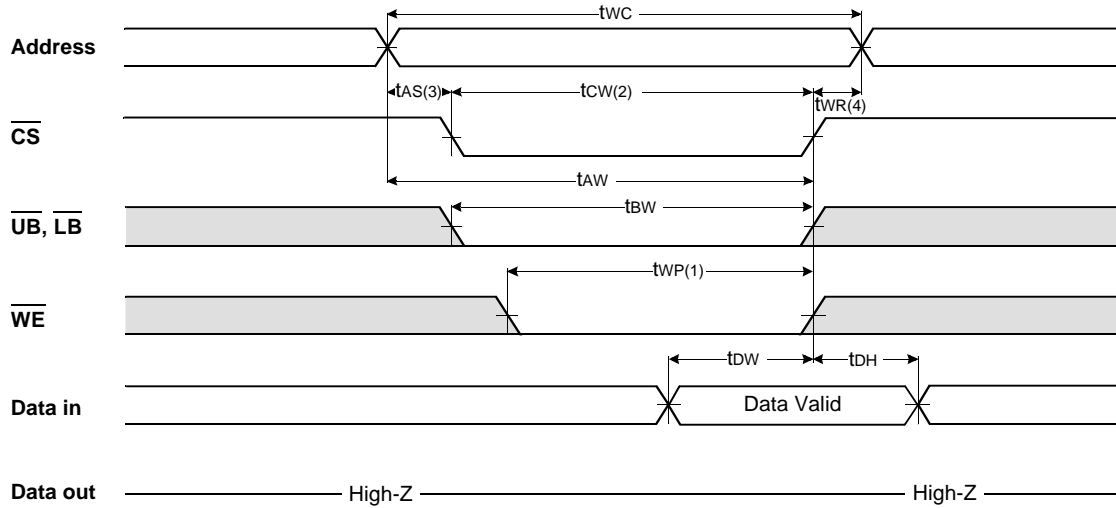
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

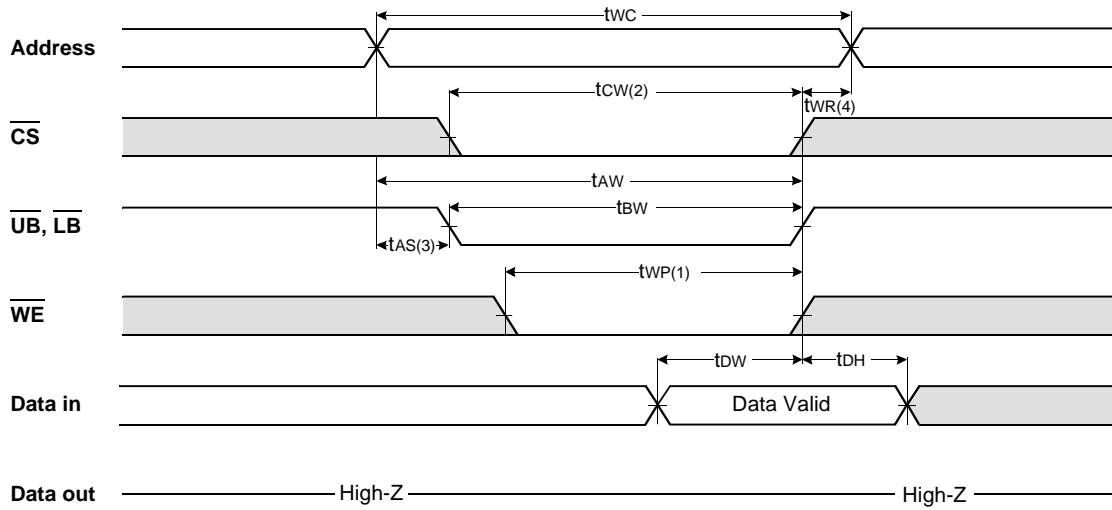
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{CS} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (\overline{UB} , \overline{LB} Controlled)

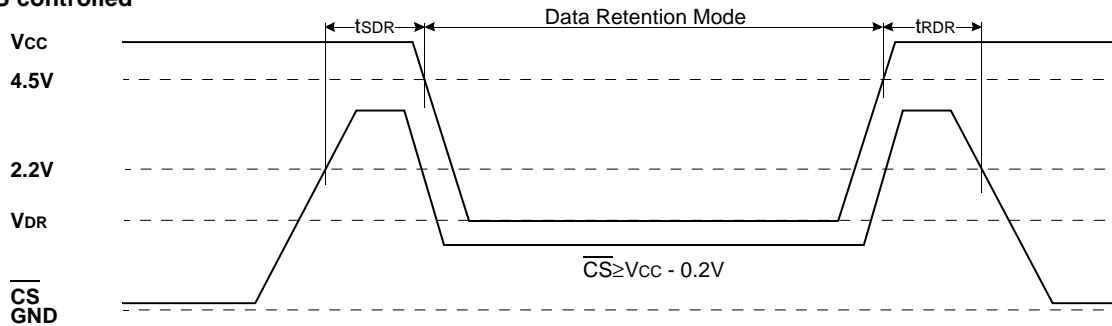


NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high and \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as \overline{CS} or \overline{WE} going high.

DATA RETENTION WAVE FORM

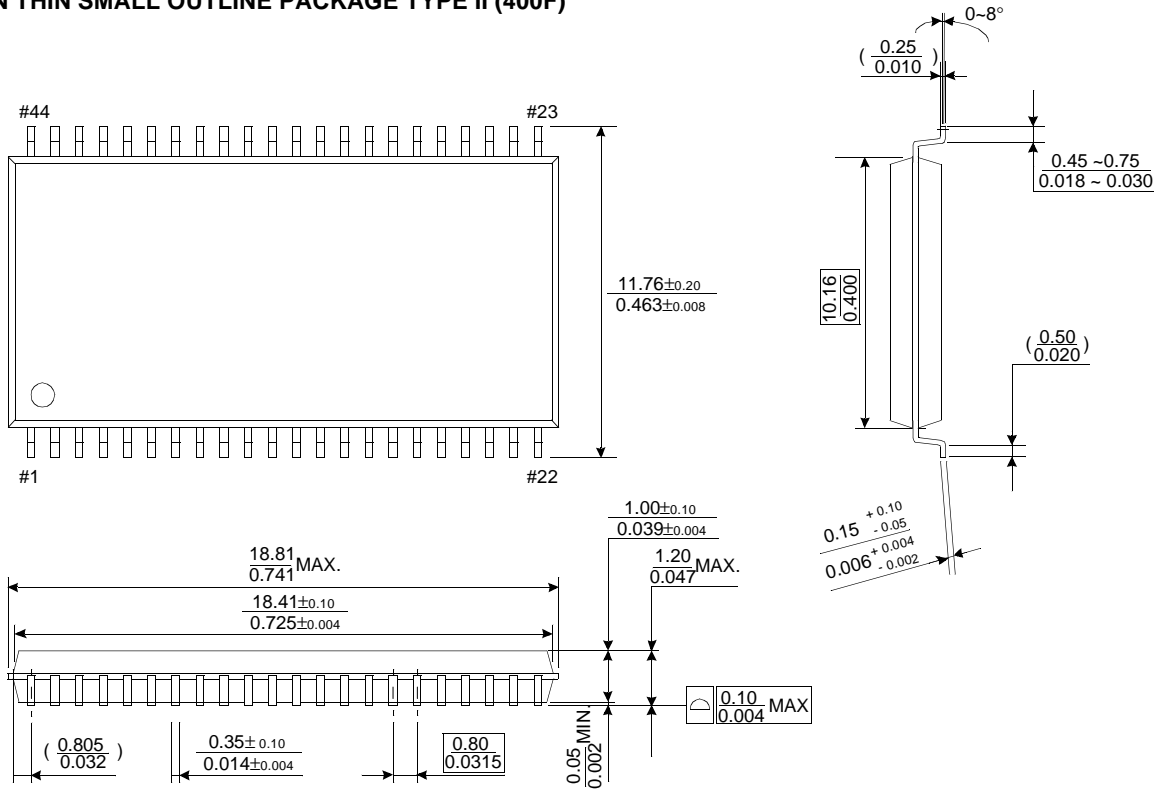
\overline{CS} controlled



PACKAGE DIMENSIONS

Unit: millimeters(inches)

44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)



44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400R)

