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1. GENERAL DESCRIPTION

The N567Kxxx is a powerful microcontroller (uC) dedicated to speech and melody synthesis applications. With the help of the embedded 8-bit microprocessor & dedicated H/W, the N567Kxxx can synthesize 6-channel speech+melody simultaneously.

The two channels of synthesized speech can be in different kinds of format, for example ADPCM and MDPCM. The N567Kxxx can provide 6-channel high-quality wavetable melody, which can emulate the characteristics of musical instruments, such as piano and violin. More colorful melody effects are implemented in N567Kxxx series, such as modulation, vibrato, and pitch-bending etc. The output of speech/melody channels are mixed together through the on-chip digital mixer to produce colorful effects. With these hardware resources, the N567Kxxx is very suitable for high-quality and sophisticated scenario applications.

The N567Kxxx provides at most 32 I/O pins, 384 bytes RAM , IR carrier, Serial Interface Management (SIM), and more sophisticated applications, such as interactive toys, cartridge toys and final count down function. 3-pair LED output pins with 64-level control means that numerous combination of RGB colors may result in a versatility of colorful effects. In addition, N567Kxxx also provides PWM mode audio output to save power during playback and Watch Dog Timer to prevent latch-up situation occurring.

The N567Kxxx family contains several items with different playback duration as shown below: (@4-bit NM4 algorithm, 6 KHz sampling rate)

Item	**N567K030**	**N567K041**	**N567K080**	**N567K120**	**N567K160**	**N567K200**
*Duration	34 sec.	44 sec.	84 sec.	124 sec.	158 sec.	192 sec.
Item	**N567K240**	**N567K280**	**N567K330**	****N567K121**	****N567K161**	****N567K201**
*Duration	233 sec.	272 sec.	311 sec.	124 sec.	158 sec.	192 sec.

Note: *: The duration time is based on 4-bit NM4 at 6 KHz sampling rate. The firmware library and timber library have been excluded from user's ROM space for the duration estimation.

Note: **: N567K121, K161, K201 are modified from N567K120, K160, K200 respectively to consist with OTP's pad sequence.

2. FEATURES

- Wide range of operating voltage:
  - 8 MHz @ 3.0 volt ~ 5.5 volt
  - 6 MHz @ 2.4 volt ~ 5.5 volt
- Oscillator
  - Trim function -Build in Rosc and system clock setting: 4MHz, 6MHz or 8MHz by Mask Option
  - X'tal oscillator –Only in N567K240/280/330/041/030 by Mask Option
    - Add external Crystal 8MHz~16MHz for system clock 4M~8MHz
- Power management:
  - 4 ~ 8 MHz system clocks, with Ring type or crystal type.
  - Stop mode for stopping all IC operations
    - Status changes of the IP0 and BP0~BP2 pins can wake up the chip
- Provides up to 8 inputs and 24 I/O pins
  - N567K030~K201: 24I/O
  - N567K240~K330: 8I + 24I/O
- Audio output : 1 speaker outputs, mono effect available
  - DAC : maximum output is 3mA/5mA , (10+3)-bit without Noise Shaping to drive speaker output.
  - PWM: direct drive 12 bit with Noise Shaping to save power consumption.
- F/W speech synthesis:
  - Multiple format parser that supports
    - New 4-bit MDPCM(NM4), 5-bit MDPCM(MDM), 4-bit MDPCM(MD4), 4-bit ADPCM(APM), 8-bit Log PCM(LP8) algorithm can be used
    - Pitch shippable ADPCM for voice changer application
  - Dual-sample rate voice synthesis
- F/W Melody synthesis:
  - 6 melody channels that can emulate characteristics of musical instruments
  - Multi-MIDI files simultaneous
  - Multi-MIDI channels dynamic control
  - More MIDI events are supported for colorful melody playback, such as modulation wheel, pitch-bending, pedal, pitch-shift, and vibrato…etc.
- Speech and melody can be playing at the same time
  - 2 channels speech + 4 channels wavetable melody
  - 1 channel speech + 5 channels wavetable melody
  - 6 channels wavetable melody
- Built-in IR carrier generation circuit for simplifying firmware IR application
- Built-in TimerG1 for general purpose applications
- Harmonized synchronization among MIDI, Speech, LED, and Motor
- Build-in 3-pair LED outputs with 64-level control of brightness in N567K240~K330
  - BP00/02/04 are defined as 3 H/W PWM I/O pins. They can be paired with BP01/03/05 respectively by same (or opposite) phase of output waveform

- Built-in Watch-Dog Timer (WDT) and Low Voltage Reset (LVR) by mask option
- Provide Serial Interface Management (SIM) to access the external memory in N567K030~K080 and N567K240~K330
  - W55F, W551C
  - SPI flash/ROM
- Support ***PowerScript™*** for developing codes in easy way
- Full-fledged development system
  - Source-level ICE debugger (Assembly & ***PowerScript™*** format)
  - ***Ultra I/O™*** tool for event synchronization mechanism
  - ICE system with USB port
  - User-friendly GUI environment
- Available package form:
  - COB is essential

3. FAMILY OVERVIEW

The characteristics of N567Kxxx series are depicted in Table 1.

Part Number	N567K030	N567K041	N567K080	N567K120, /N567K121	N567K160 /N567K161
ROM (Byte)	126K	158K	286K	416K	528K
RAM (Byte)	384	384	384	384	384
Duration[1]	34 sec	44 sec	84 sec	124 sec	158 sec
System Clock	TRIM/X'tal	TRIM/X'tal	TRIM	TRIM	TRIM
In : Bid[2]	0 : 24	0 : 24	0 : 24	0 : 24	0 : 24
Audio Output	DAC PWM	DAC PWM	DAC PWM	DAC PWM	DAC PWM
Speaker	1	1	1	1	1
Mixer Input	6	6	6	6	6
Synthesis Algorithm	MDPCM ADPCM PCM	MDPCM ADPCM PCM	MDPCM ADPCM PCM	MDPCM ADPCM PCM	MDPCM ADPCM PCM
IR-Carrier (Tx)	✓	✓	✓	✓	✓
64-Level Output	X	X	X	X	X
Watch Dog Timer (WDT)	✓	✓	✓	✓	✓
Low Voltage Reset (LVR)	✓	✓	✓	✓	✓
SIM for SPI Flash Interface	✓	✓	✓	X	X
Stop mode	✓	✓	✓	✓	✓
PowerScript	✓	✓	✓	✓	✓

[1] The F/W library & program code are excluded from the ROM space for the duration estimate, which is based on 6-KHz sample rate & 4-bit NM4 algorithm.

[2] "In" is the number of input pins; "Bid" is the number of Bi-directional pins.

Part Number	N567K200 /N567K201	N567K240	N567K280	N567K330
ROM (Byte)	638K	768K	896K	1022K
RAM (Byte)	384	384	384	384
Duration	192 sec	233 sec	272 sec	311 sec
System Clock	TRIM	TRIM/X'tal	TRIM/X'tal	TRIM/X'tal
In : Bid	0 :24	8 : 24	8 : 24	8 : 24
Audio Output	DAC PWM	DAC PWM	DAC PWM	DAC PWM
Speaker	1	1	1	1
Mixer Input	6	6	6	6
Synthesis Algorithm	MDPCM ADPCM PCM	MDPCM ADPCM PCM	MDPCM ADPCM PCM	MDPCM ADPCM PCM
IR-Carrier (Tx)	✓	✓	✓	✓
64-Level Output	X	*3-Pair	*3-Pair	*3-Pair
Watch Dog Timer (WDT)	✓	✓	✓	✓
Low Voltage Reset (LVR)	✓	✓	✓	✓
SIM for W55F/W551C	X	✓	✓	✓
SIM for SPI Flash Interface	X	✓	✓	✓
Stop mode	✓	✓	✓	✓
PowerScript	✓	✓	✓	✓

Note *:BP00/02/04 are defined as 3 H/W PWM I/O pins. They can be paired with BP01/03/05 respectively by same (or opposite) phase of output waveform

Table 1: N567Kxxx family selection guide

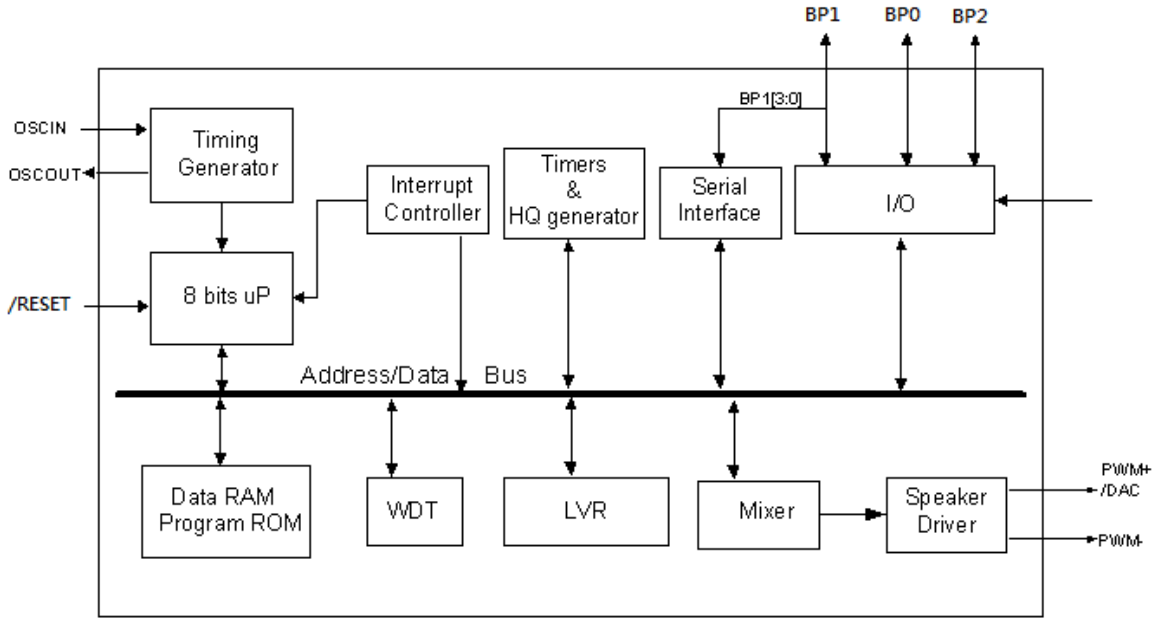
4. PIN DESCRIPTION

PIN NAME	I/O	FUNCTION
/RESET	In	IC reset input with an internal pull-up resistor, low active.
OSCIN	I	Main-clock oscillation input for X'tal mode. Build-in ROSC by mask option.
OSCOUT	O	Main-clock oscillation output for X'tal.
IP00~IP07	In	General input port with pull-high selection. Each input pin can be programmed to generate interrupt request and used to release IC from STOP mode. It is provided in N567K240~K330 only.
BP00~BP07	I/O	General input/output pins. When used as output pin, it can be open–drain or CMOS type and it can sink 25mA for high-current applications. When used as input pin, there may have a pull-high option and generate interrupt request to release IC from STOP mode. When BP07 is used as output pin, it can be the IR transmission carrier for IR applications. Only for N567K240/280/330. BP00/02/04 can be set as 3-pin H/W PWM output with 64-level resolution. They can be paired with BP01/03/05 (also H/W PWM output) respectively with same or opposite phase of output waveform.
BP10~BP17	I/O	General input/output pins. When used as output pin, it can be open–drain or CMOS type. When used as input pin, there may have a pull-high option and generate interrupt request to release IC from STOP mode. When serial interface management (SIM) is enabled, and set memory type as W55F/W551C, BP10~12 are used to be an interface with the external memory, W55Fxx or W551Cxxx. If set memory to SPI flash, BP10~13 are used to be an interface.
BP20~BP27	I/O	General input/output pins. When used as output pin, it can be open–drain or CMOS type. When used as input pin, there may have a pull-high option and generate interrupt request to release IC from STOP mode.
PWM+/DAC	O	PWM driver positive output or Current type DAC output
PWM-	O	PWM driver negative output
VDD	Power	Positive power supply for uP and peripherals.
VSS	Power	Negative power supply for uP and peripherals.
VDD_SPK	Power	Positive power supply for speaker driver.
VSS_SPK	Power	Negative power supply for speaker driver.
VDD_SIM	Power	Positive power supply for serial interface Management (SIM) BP10~13 Only providing in N567K240~N567K330. For non-SIM application, it should be connect to V_{DD} to keep normal standby current.
VDD_OSC	Power	Positive power supply for oscillator. Only providing in N567K240~N567K330. It must be connected to VDD.
VSS_OSC	Power	Negative power supply for oscillator. Only providing in N567K240~N567K330. This pad must be connected to VSS.

5. ITEM VS PIN TABLE

PIN name	K030/041	K080	K120/160/200 K121/161/201	K240/280/330	Comment
BP00~07	V	V	V	V	
BP10~17	V	V	V	V	
BP20~27	V	V	V	V	
IP00~07	-	-	-	V	
/RESET	V	V	V	V	
PWM+/DAC	V	V	V	V	
PWM-	V	V	V	V	
OSCIN	V	V	V	V	
OSCOUT	V	-	-	V	Crystal mode
VDD	V	V	V	V	
VSS	V	V	V	V	
VDD_SPK	V	V	V	V	Support speaker power
VSS_SPK	V	V	V	V	
VDD_SIM	-	-	-	V	Support BP10~13 SIM interface power
VDD_OSC	-	-	-	V	Support OSCIN/OUT power
VSS_OSC	-	-	-	V	

6. BLOCK DIAGRAM



7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +7.0	V
D.C. Voltage on Any Pin to Ground Potential	-0.3 to V_{DD} +0.3	V
Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7.2 D.C. Characteristics

(V_{DD}–V_{SS} = 4.5 V, F_M = 8 MHz, Ta = 25°C, No Load unless otherwise specified)

PARAMETER	SYM.	TEST CONDITIONS	SPEC.			UNIT
			Min.	Typ.	Max.	
Operating Voltage	V_{DD}	F_{SYS} = 6 MHz	2.4	-	5.5	V
		F_{SYS} = 8 MHz	3.0	-	5.5	V
Operating Current	I_{OP}	F_{SYS} = 8MHz, normal operation	-	8	12	mA
Standby Current	I_{SB}	STOP mode	-	1	2	μA
Input Low Voltage	V_{IL}	All input pins	V_{SS}	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	All input pins	0.7 V_{DD}	-	V_{DD}	V
Input Current I/O pins	I_{IN1}	V_{IN} = 0V, pulled-high resistor = 500k ohm	-5	-9	-14	μA
Input Current I/O pins	I_{IN2}	V_{IN} = 0V, pulled-high resistor = 150k ohm	-15	-30	-45	μA
Output Current (BP0)	I_{OL}	V_{DD} = 3V, V_{OUT} = 0.4V	8	12	-	mA
	I_{OH}	V_{DD} = 3V, V_{OUT} = 2.6V	-4	-8	-	mA
	I_{OL}	V_{DD} = 4.5V, V_{OUT} = 1.0V	-	35	-	mA
	I_{OH}	V_{DD} = 4.5V, V_{OUT} = 3.5V	-	-20	-	mA
Output Current (BP1, BP2)	I_{OL}	V_{DD} = 3V, V_{OUT} = 0.4V	4	6	-	mA
	I_{OH}	V_{DD} = 3V, V_{OUT} = 2.6V	-4	-8		mA
	I_{OL}	V_{DD} = 4.5V, V_{OUT} = 1.0V	-	15	-	mA
	I_{OH}	V_{DD} = 4.5V, V_{OUT} = 3.5V	-	-20	-	mA
DAC Full Scale Current	I_{DAC}	V_{DD} = 4.5V, RL = 100Ω	-2.4 -4.0	-3.0 -5.0	-3.6 -6.0	mA
Output Current PWM+ / PWM-	I_{OL1}	RL= 8 Ohm, [PWM+]---[RL]---[PWM-]	+200	-	-	mA
	I_{OH1}		-200	-	-	mA

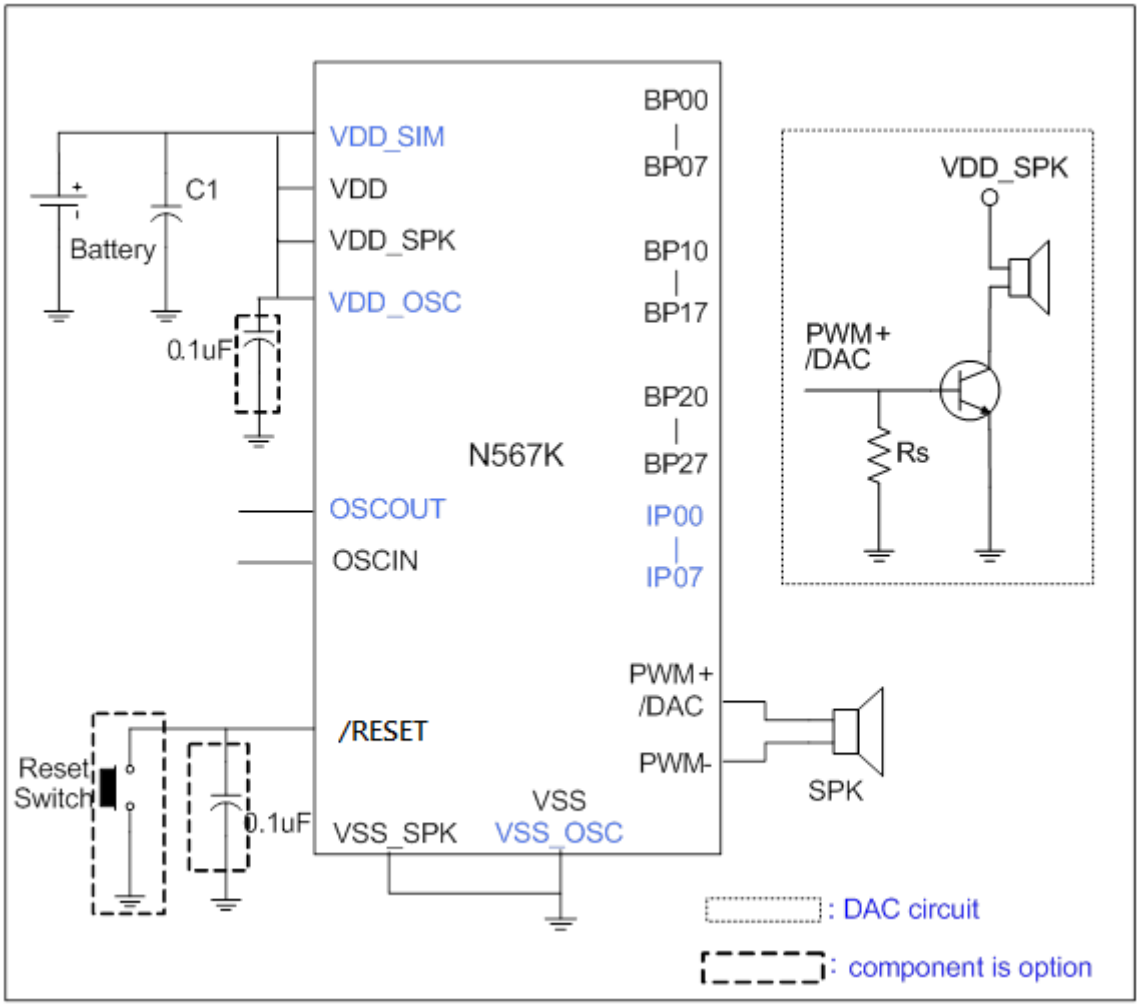
7.3 A.C. Characteristics

(V_{DD}-V_{SS} = 4.5 V, F_M = 8 MHz, Ta = 25°C; No Load unless otherwise specified)

PARAMETER	SYM.	TEST CONDITIONS	SPEC.			UNIT
			Min.	Typ.	Max.	
Main-Clock	F_M	ROSC build-in, @3.0~5.5V	3973	4096	4218	KHz
		ROSC build-in, @3.0~5.5V	5959	6144	6328	
		ROSC build-in, @3.0~5.5V	7946	8192	8437	
Main-Clock	F_M	ROSC build-in, @2.4~3.6V	3973	4096	4218	KHz
		ROSC build-in, @2.4~3.6V	5959	6144	6328	
Main-Clock Wake-up Stable Time	T_{WSM}	2^16 clock cycle	8		16	mS

8. TYPICAL APPLICATION CIRCUITS

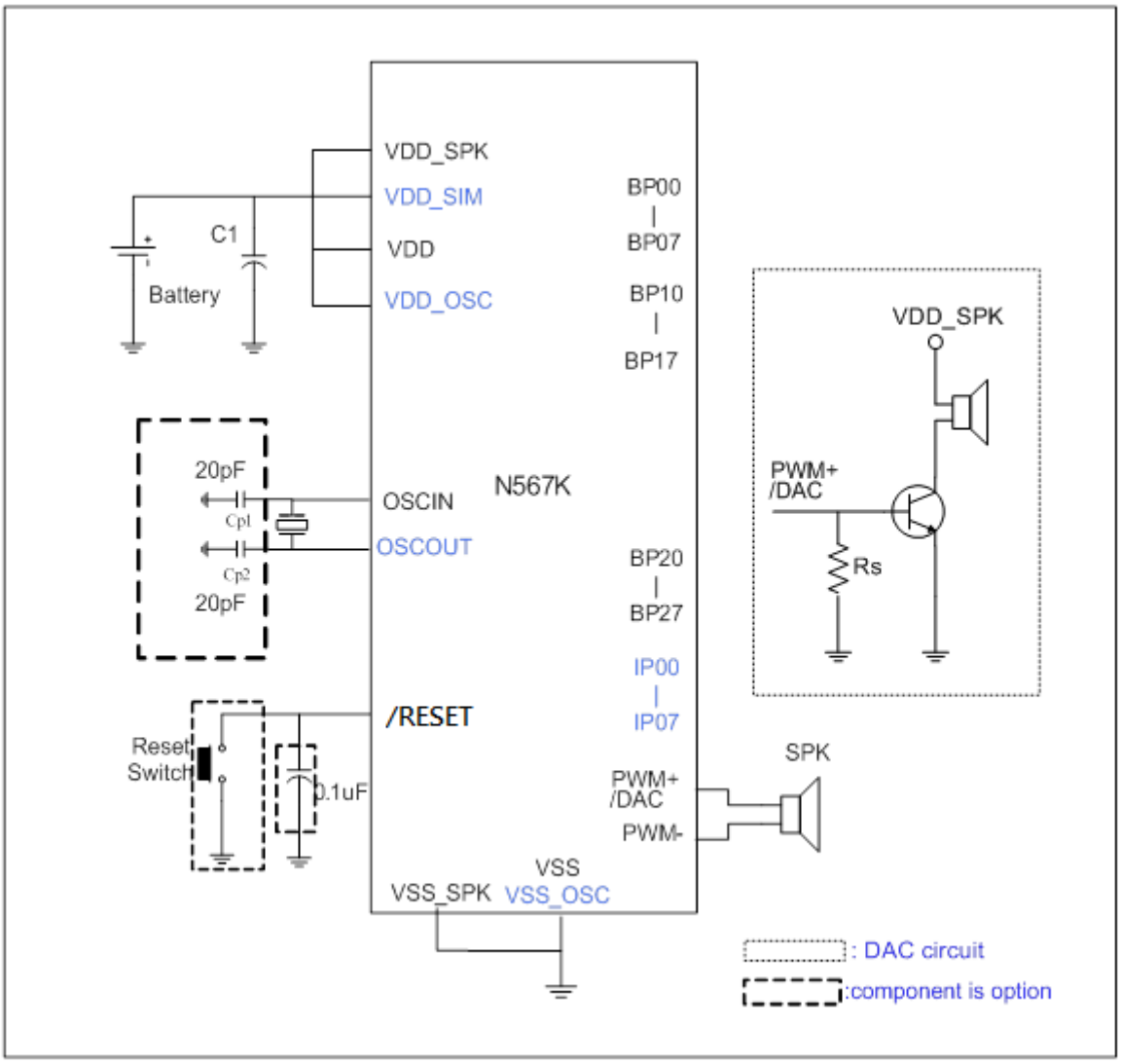
(a) Trim Ring oscillator application



Notes:

1. Rosc is built in N567K chip internally. User needn't connect Rosc resistor to OSCIN pin.
2. The C1 value is suggested 4.7uF for audio PWM output or 0.1uF for DAC output.
3. The Rs value is suggested in 270Ω ~ 1KΩ to limit too large DAC output current flowing into transistor.
4. The VDD_OSC pad must be connected to VDD. To add a 0.1uF capacitor to VSS is optional to improve oscillator stability.
5. The VDD_SIM pad must be connected to VDD for non-SIM application.
6. The above application circuits are for reference only. No warranty for mass production.

(b) Crystal application



Notes:

1. The crystal value must be double of system clock. If System clock is 6MHz, please select 12MHz crystal device. The crystal should be placed close to IC, and the location is as near as possible.
2. The value of Cp1 and Cp2 are depended on PCB layout and crystal type suggested 15~30pF or skip.
3. The C1 value is suggested 4.7uF in audio PWM output and 0.1uF in DAC output.
4. The VDD_OSC pad must be connected to VDD.
5. The VDD_SIM pad must be connected to VDD if without SIM application.
6. The above application circuits are for reference only. No warranty for mass production.
7. Other application circuits please refer to Design Guide.

(c) PCB layout guide

1. The IC substrate should be connected to VSS in PCB layout. But VSS_SPK can't connect with IC substrate directly. Both VSS and VSS_SPK tie together in battery negative power.

2. Each VDD, VDD_OSC, VDD_SIM and VDD_SPK pad must connect to positive power to support stable voltage for individual function work successfully. (Don't let them floating)

9. REVISION HISTORY

VERSION	DATE	REASONS FOR CHANGE	PAGE
A0.0	June 2009	Preliminary release.	
A1.0	July 2009	➢ SIM is provided in N567K040~K080. ➢ PWM speaker output is provided in N567K040~K080.	
A2.0	Aug. 2009	➢ Add VDDOSC and VSSOSC in the pin description ➢ Remove TEST pad in the pin description ➢ Modify N567K240~K330 application circuit	
A3.0	Aug. 2009	➢ Modify Frequency deviation in 5.3 A.C. Characteristics.	
A4.0	Sep. 2009	➢ Modify Main Clock and Frequency deviation condition in 5.3 A.C. Characteristics.	
A5.0	Oct. 2009	➢ Remove LVD function in 2 Features	
A6.0	Nov. 2009	➢ Revise frequency deviation value of 2.4~3.6V in section 5.3 A.C. Characteristics.	
A7.0	Feb. 2011	➢ Remove N567K240~330 SPIO function except N567H000 ICE chip ➢ VDD_SPIO/VSS_SPIO and VDD_SIM/VSS_SIM pins must be connect to V_{DD} /V_{SS} to keep normal standby current. ➢ Update output current for BP1/2 @4.5V/3.0V and update BP0 @4.5V ➢ Update 4.7uF is optional as power stability on DAC application on application circuit ➢ Update 4.7uF is necessary as power stability on PWM application on application circuit	11 5 7 9 10
A8.0	Apr. 2011	➢ Add N567Kxx chip family overview ➢ Add SIM SPI Flash application circuit for N567K040~K080 ➢ Update Application Circuit and note description ➢ Add power circuit in PCB layout ➢ N567K240~330 modify VDD_SPI pad to VDD2 which must be connected to VDD.(please refer bonding pad diagram rev. A1)	5~6 13 11~18 18 7
A9.0	Sep. 2011	➢ Modify OSCIN application circuits, for DAC output no connected, PWM output add a 200pF capacitor to VDD to improve voice quality optional. ➢ Add new 4-bit MDPCM (NM4) speech synthesis algorithm	11~15 3

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