SATURN® User Network Interface for 9.953 Gbit/s

GENERAL DESCRIPTION

- The S/UNI-9953-POS is a single chip ATM, POS User-Network Interface operating at 9953.28 Mbit/s. The S/UNI 9953-POS is intended for use in OC-192c and high-density OC-48c POS/ATM applications.

FEATURES

- Supports framing, scrambling/ descrambling and pointer processing for the following:
  - STS-192c (STM-64-64c).
  - 4 x STS-48c (4 x STM-16-16c).
  - STS-192 (STM-64) channelized down to STS-48c (STM-16c).
- Supports alarm signal insertion/detection, B1/2/3 processing and insertion/termination of SONET Section/Line/Path overhead bytes (or SDH equivalents).
- Provides ATM and POS payload processing for:
  - STS-192c (STM-64-64c)
  - 4 x STS-48c (4 x STM-16-16c).
  - STS-192 (STM-64) channelized down to STS-48c (STM-16c).

INTERFACES

- Provides SATURN® POS-PHY™ Level 4 16-bit LVDS System-side Interface (clocked at 700 MHz nominal).
- Directly connects to optics via 16 bit by 622 MHz OIF SFI-4 (OIF99.102) line-side interface.

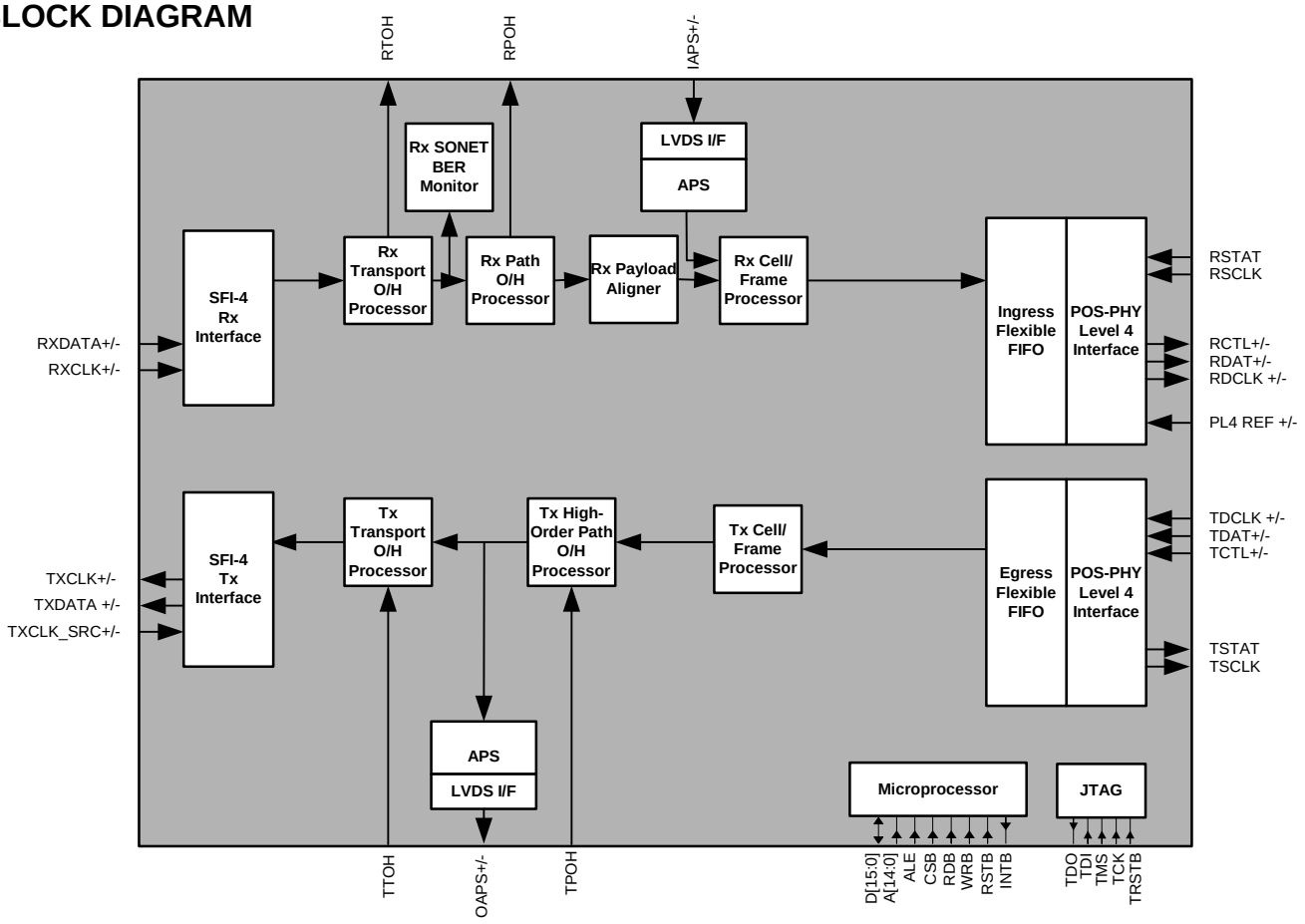
POS/ATM

- Implements the ATM Forum User Network Interface Specification and the ATM physical layer for Broadband ISDN according to CCITT Recommendation I.432.
- Implements the Point-to-Point Protocol (PPP) over SONET/SDH specification according to RFC 2615(1619)/1662 of the PPP Working Group of the Internet Engineering Task Force (IETF).

GENERAL

- Provides internal FIFOs (16 KB ingress, 20 KB egress) to accommodate system latencies.
- Provides line-side and system-side loopbacks for system level diagnostic capability.
- Provides support for automatic protection switching (APS) via two 16-bit LVDS 777.76 MHz ports.
- Provides a generic 16-bit microprocessor bus interface for configuration, control and status monitoring.
- Standard 5 signal P1149.1 JTAG test port.

BLOCK DIAGRAM



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- Low power 1.8 V CMOS core logic with 3.3 V CMOS/TTL compatible digital inputs and digital outputs.
- Industrial temperature range (-40 °C to +85 °C).
- 1152 pin FCBGA package.

DEVICE INTERWORKING

- Other PMC-Sierra devices that implement the POS-PHY Level 4 interface include:
  - S/UNI 1x10GE.
  - S/UNI 10xGE.
  - S/UNI 9953.

POS-PHY LEVEL 4 INTERFACE

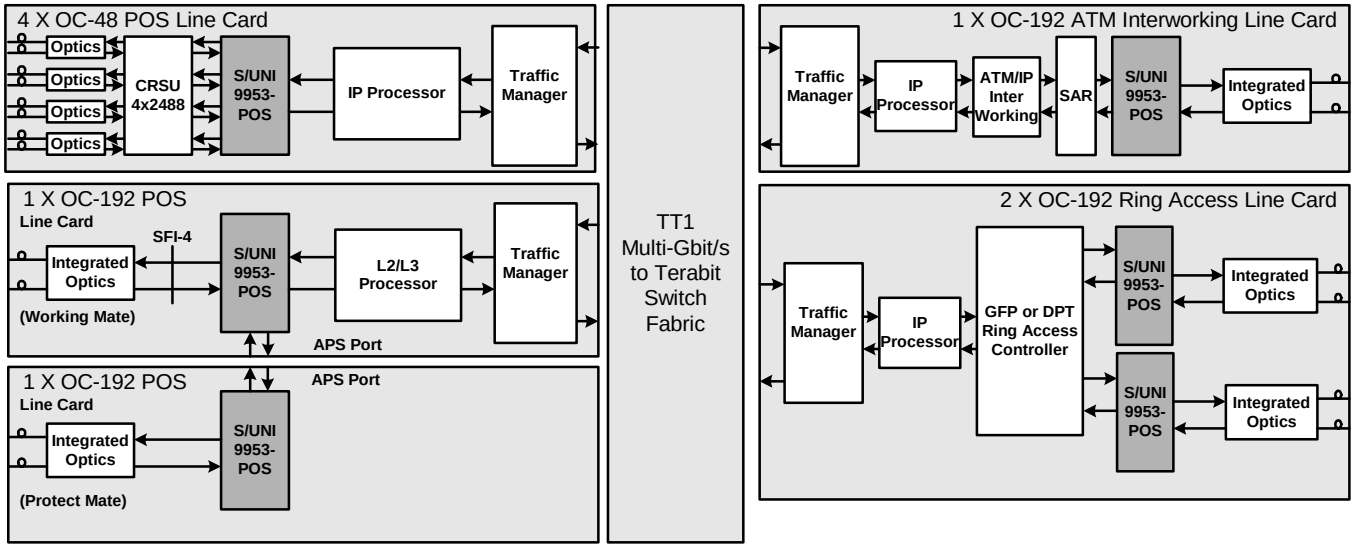
- Designed to transmit cells, packets, or frames between physical and data-link layer devices.
- Requires less pins and draws less power than other 10 Gigabit interface options.
- Compliant with the following standards:
  - Optical Internetworking Forum - System Physical Interface Level 4 Phase II (SPI-4 Phase II).
  - ATM Forum - Frame Based ATM Interface Level 4 (ATMF0161.00).
  - SATURN® POS-PHY™ Level 4, Issue 6, March 2001.

APPLICATIONS

- Edge and Core Routers.
- Multi-Service (Multi-Protocol) Switches.
- SONET/SDH add/drop multiplexers and optical cross-connects.
- WAN and Edge ATM switches.
- Up-link cards.
- SONET/SDH ATM/POS test equipment.
- Emerging DPT, IPT and GFP applications.

TYPICAL APPLICATION

10 GIGABIT / OC-192 ROUTER PORT CARD APPLICATION



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All product documentation is available on our web site at: http://www.pmc-sierra.com For corporate information, send email to: info@pmc-sierra.com

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