

EARTH LEAKAGE CURRENT DETECTOR Earth Leakage Current Detector IC



BD95820F-LB BD95820N-LB

General Description

This product guarantees long time support in Industrial market.
BD95820F-LB/BD95820N-LB integrates leakage detector and amplifier. Especially, it is suitable for high sensitivity and a high-speed operation use, and since the operating temperature range is wide, it can be used for various uses.

Key Specifications

- Operating Supply Voltage Range : 12V to 22V
- Operating Temperature Range : -20°C to +95°C
- Supply Current : 330µA (typ)
- Trip Voltage : 4.92mV to 11.06mV
- Output Current(Ta=-20°C) : -200µA (min)

Features

- Long Time Support a Product for Industrial Applications
- Small Temperature Fluctuation and High Input Sensitivity
- Wide Operating Temperature Range

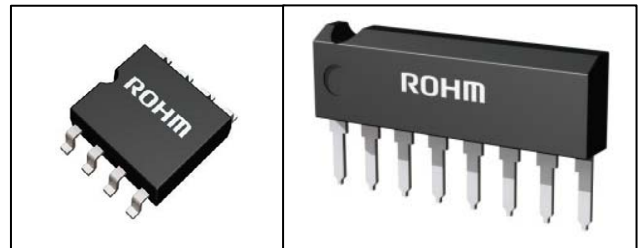
Applications

- Earth leakage circuit breaker
- Earth leakage circuit relay
- Industrial Equipment

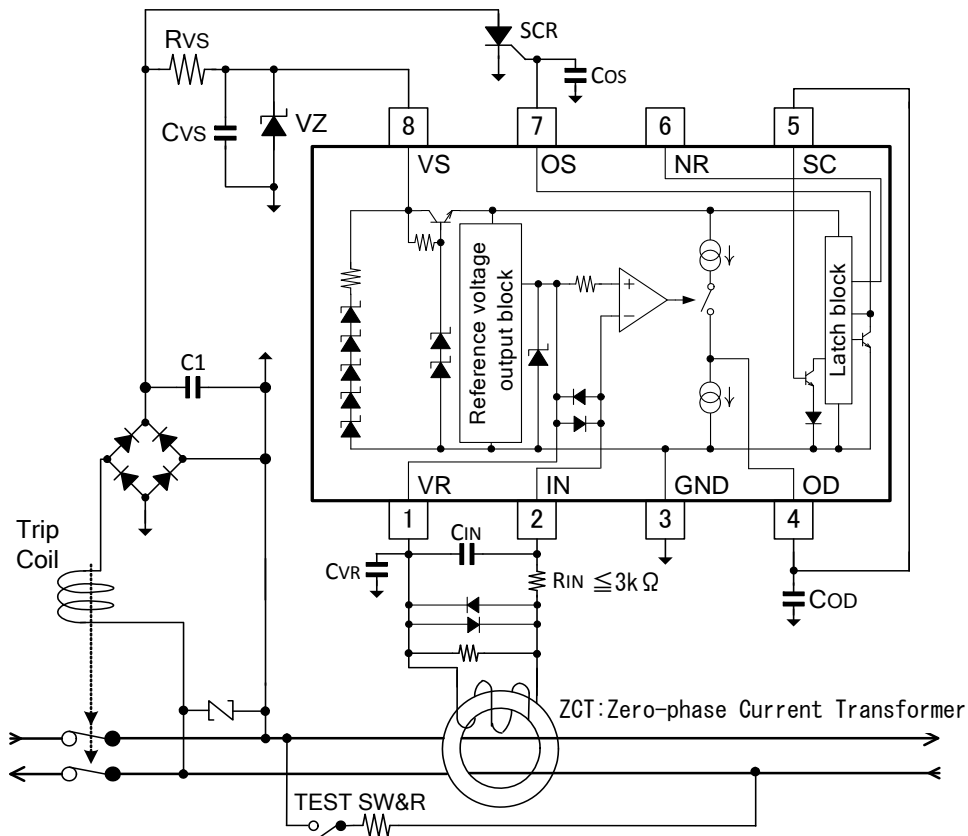
Packages

SOP8
SIP8

W(Typ) x D(Typ) x H(Max)
5.00mm x 6.20mm x 1.71mm
19.30mm x 10.50mm x 3.00mm

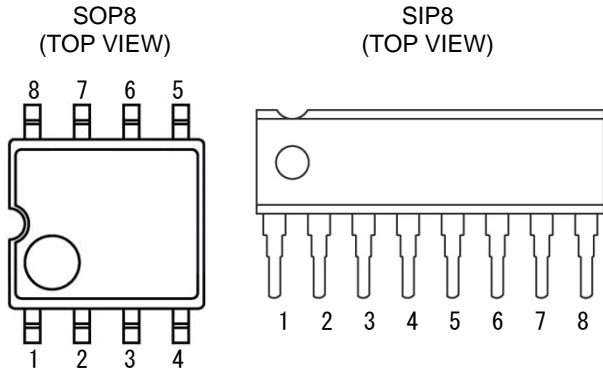


Typical Application Circuit

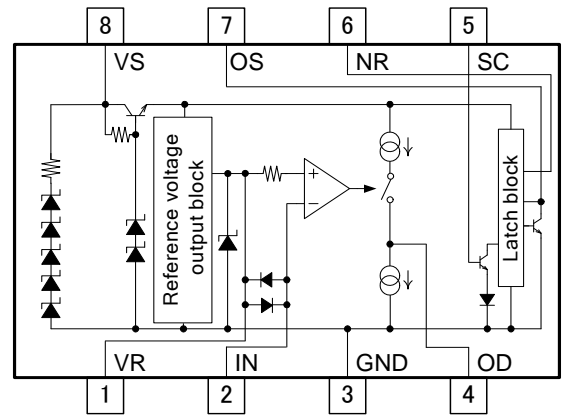


○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays.

Pin Configurations



Block Diagrams



Pin Descriptions

Pin No.	Symbol	Function
1	VR	Reference voltage
2	IN	Input
3	GND	Ground
4	OD	Output of input comparator
5	SC	Input of latch circuit
6	NR	Noise absorption
7	OS	Output
8	VS	Power supply

Absolute Maximum Ratings

(Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply current ^(Note 1)	I _S	8	mA
IN-VR current	I _{IN-VR}	±250	mA
VR pin current	I _{VR}	30	mA
IN terminal current	I _{IN}	30	mA
SC terminal current	I _{SC}	5	mA
Power Supply voltage	V _S	36	V
Input terminal voltage	V _{VR/IN}	17	V
OD/SC/NR/OS terminal voltage	V _{OD/SC/NR/OS}	8	V
Power dissipation	P _D	0.68(SOP8) ^(Note 2)	W
		1.12(SIP8) ^(Note 3)	
Storage temperature	T _{stg}	-55 to +150	°C

(Note 1) The power-supply voltage is limited by the internal clamping circuit.
 (Note 2) Mounted on 70mm x 70mm x 1.6mm glass epoxy board. Reduce 5.5mW per 1°C above 25°C.
 (Note 3) P_D is a value in the package unit. Reduce 9.0mW per 1°C above 25°C.

Recommended Operating Ratings

Parameter	Symbol	Limits	Unit
Supply voltage	V_S	12 to 22	V
Operating temperature	T_{opr}	-20 to +95	°C
External capacitor between VS and GND	C_{VS}	$1 \leq$	μF
External capacitor between OS and GND	C_{OS}	≤ 1	μF

Electrical Characteristics

(Unless otherwise specified, $V_S=12V$, $GND=0V$, $T_a=25^\circ C$, Full range: $-20^\circ C$ to $+95^\circ C$)

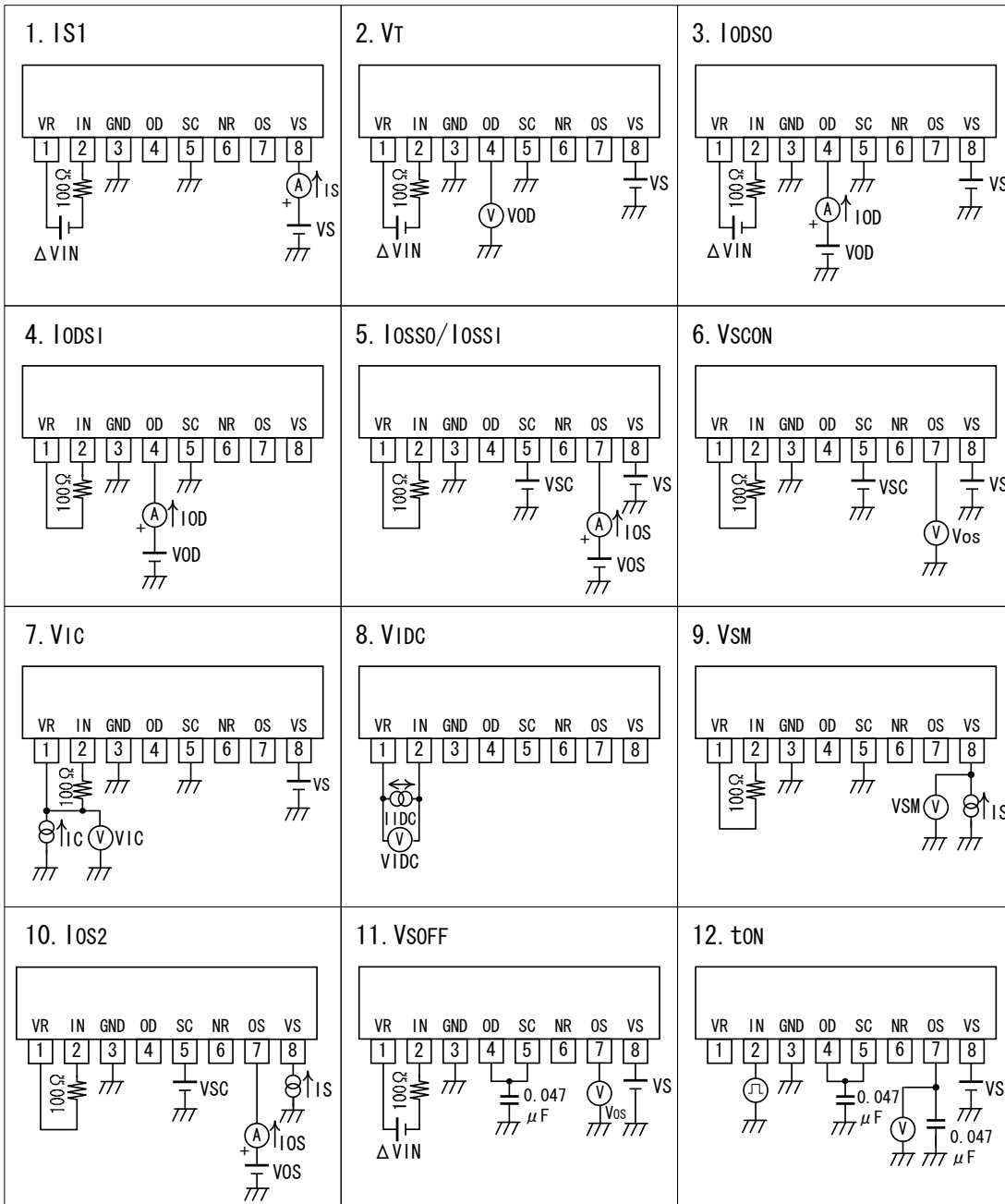
Parameter	Symbol	Temperature range	Limits			Unit	Conditions
			Min	Typ	Max		
Supply current	I_{S1}	-20°C	-	-	520	μA	$\Delta V_{IN}=V_{VR}-V_{IN}=30mV$
		25°C	-	330	500		
		95°C	-	-	460		
Trip voltage	V_T	Full range	4.92	7.50	11.06	mV	$V_T=\Delta V_{IN}=V_{VR}-V_{IN}$
OD Source current	I_{ODSO}	25°C	-27.2	-20.6	-14.0	μA	$\Delta V_{IN}=V_{VR}-V_{IN}=30mV$, $V_{OD}=1.2V$
OD Sink current	I_{ODSI}	25°C	16.7	26.0	35.3	μA	$V_{OD}=0.8V$, $\Delta V_{IN}=V_{VR}-V_{IN}=0mV$
OS Source current	I_{OSSO}	-20°C	-200	-	-	μA	$V_{SC}=2.0V$, $V_{OS}=0.8V$
		25°C	-100	-	-		
		95°C	-75	-	-		
OS Sink current	I_{OSSI}	Full range	200	-	-	μA	$V_{SC}=0.2V$, $V_{OS}=0.2V$
SC ON voltage	V_{SCON}	25°C	1.00	1.24	1.48	V	
Input clamp voltage	V_{IC}	Full range	4.2	5.5	6.7	V	$I_{IC}=20mA$
Differential input clamp voltage	V_{IDC}	Full range	0.6	1.0	1.4	V	$I_{IDC}=100mA$
Maximum current voltage	V_{SM}	25°C	26	29	32	V	$I_S=7mA$
Supply current 2 (Note 4)	I_{OS2}	Full range	-100	-	-	μA	$I_S=900\mu A$, $V_{SC}=2.0V$ $V_{OS}=0.8V$
Latch OFF Supply Voltage	V_{SOFF}	25°C	2.7	3.7	4.7	V	
Operating time (Note 5)	t_{ON}	25°C	1.8	2.9	4.0	ms	

(Note 4) Supply current 2 is OS source current value when the power supply current ($I_S=900\mu A$) is given.

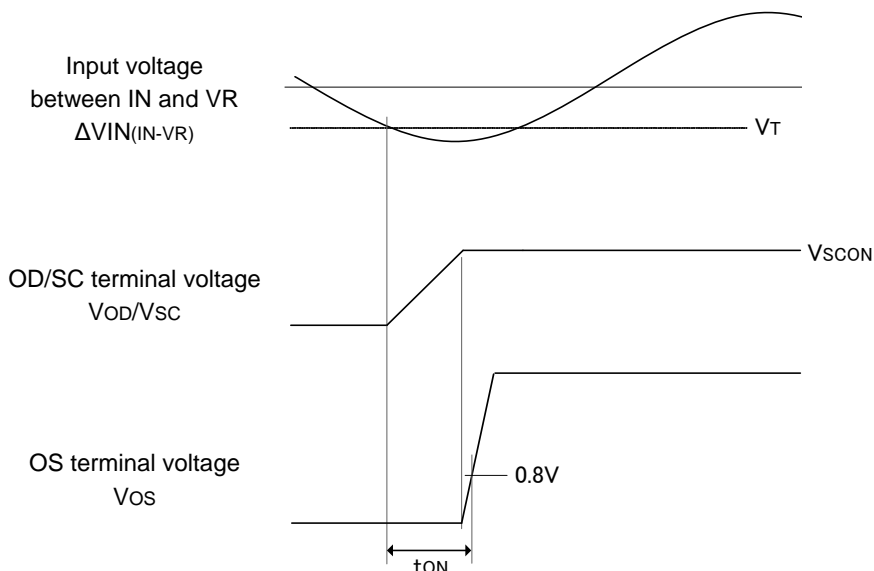
(Note 5) Operating time is time until output voltage reaches 0.8V after detecting the leakage signal.

Conditions : Capacitor (0.047 μF) is connected between OD(OS) and GND.

Test circuits



Timing Chart



Typical Performance Curves(reference data)

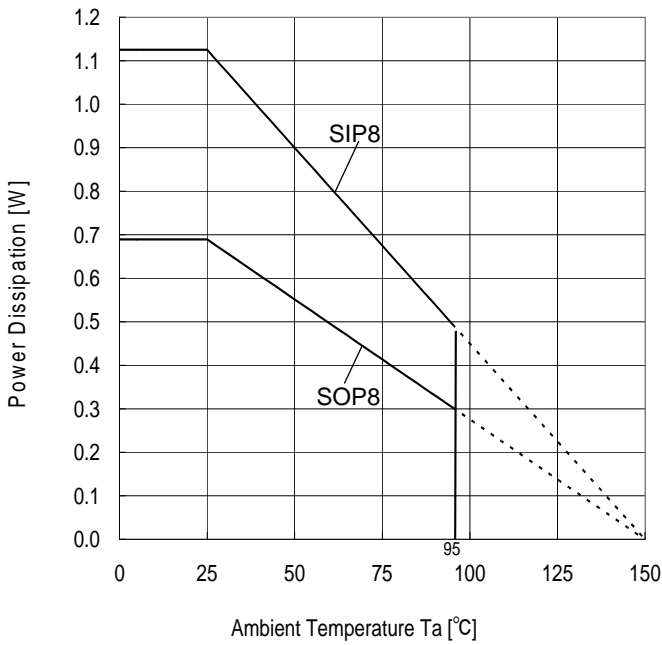


Figure 1
Derating curve

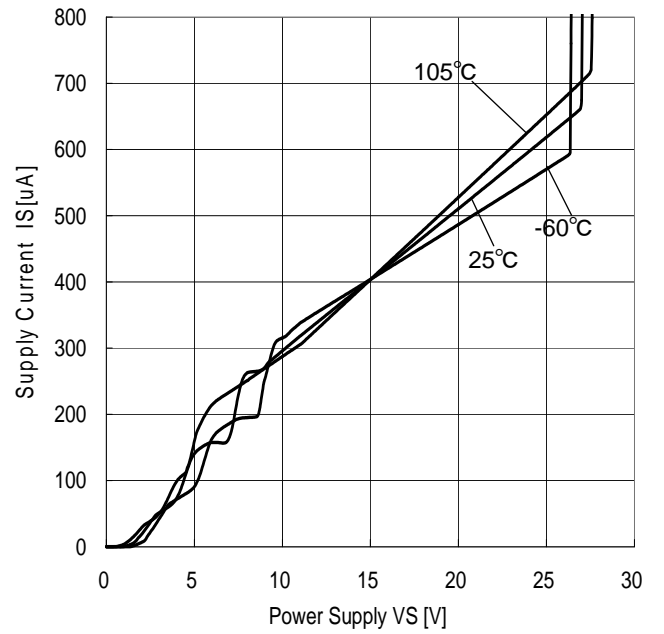


Figure 2
Circuit current - Supply voltage

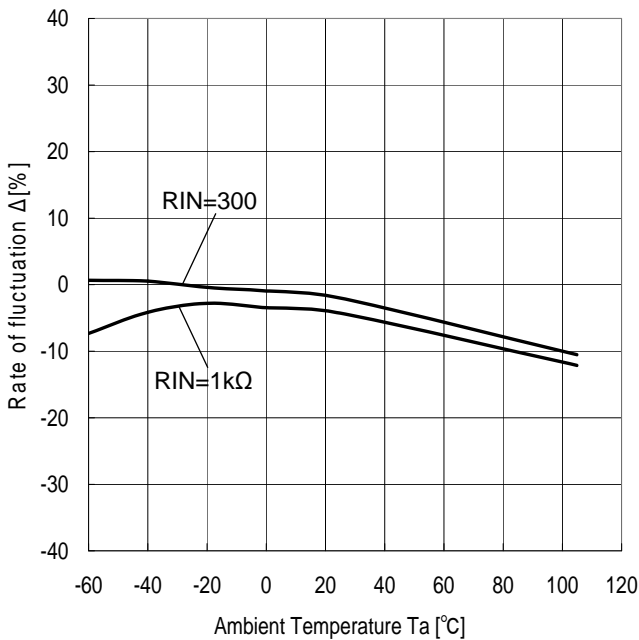


Figure 3
Trip voltage fluctuation rate
- Ambient temperature

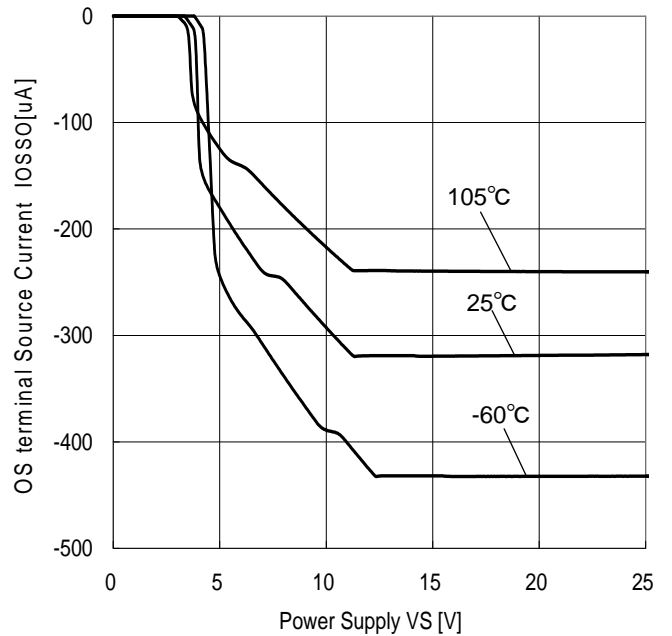


Figure 4
OS terminal source current - Supply voltage

Typical Performance Curves(reference data) - continued

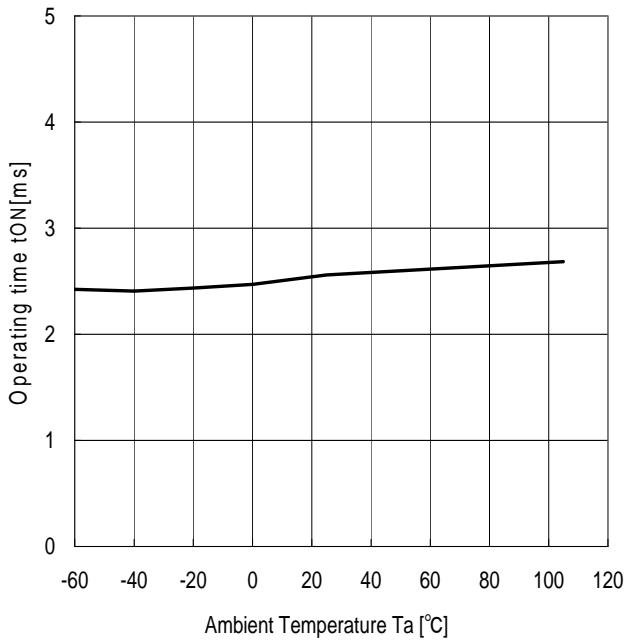


Figure 5
Operating time - Ambient temperature

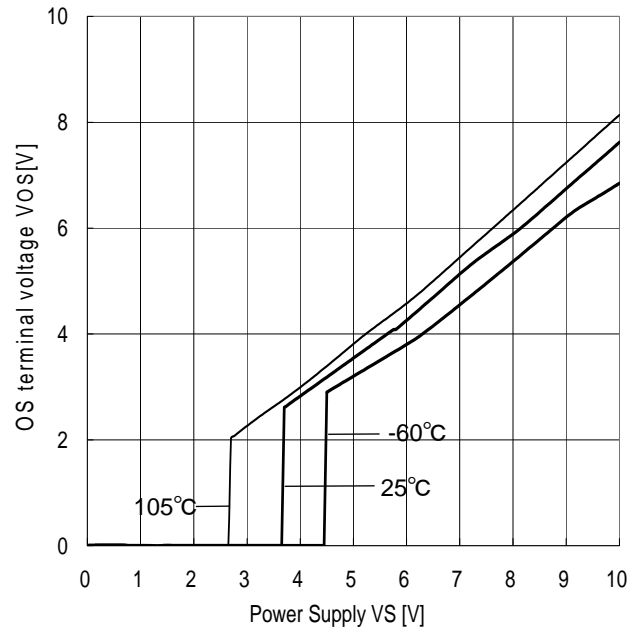


Figure 6
Latch OFF supply voltage - Ambient temperature

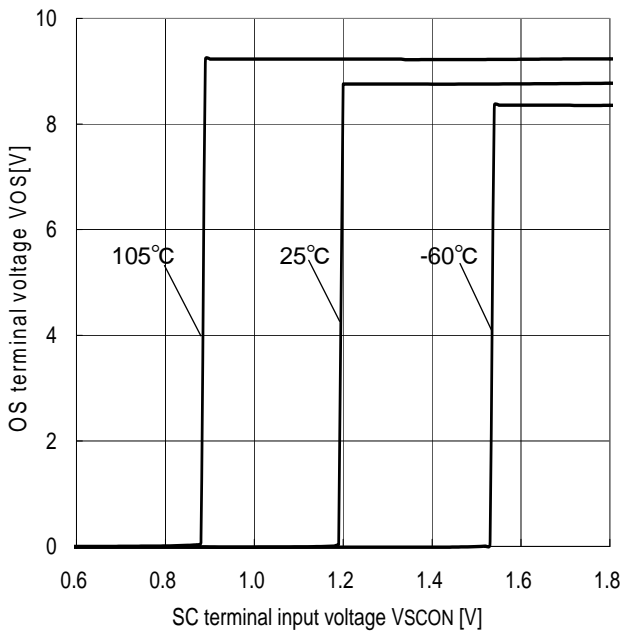


Figure 7
SC ON voltage - Ambient temperature

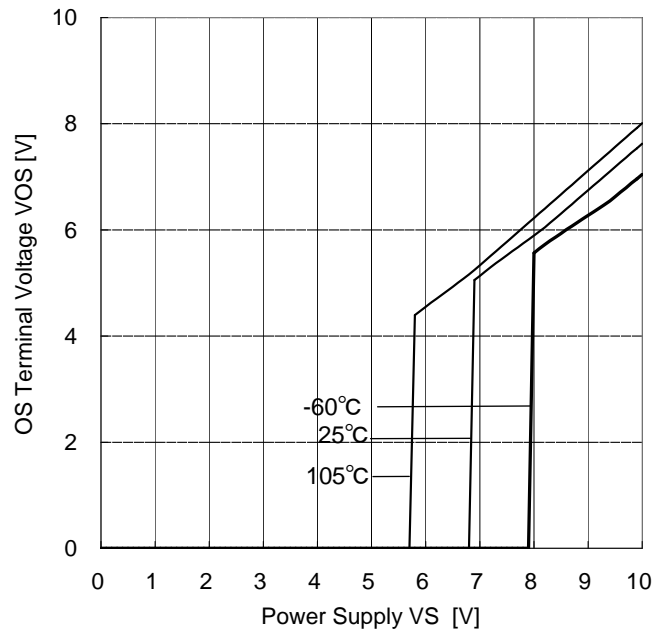


Figure 8
Latch ON supply voltage - Ambient temperature

Power Dissipation

Power dissipation(total loss) indicates the power that can be consumed by IC at Ta=25°C(normal temperature).IC is heated when it consumed power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability(hardness of heat release)is called thermal resistance, represented by the symbol θ_{ja} °C/W.The temperature of IC inside the package can be estimated by this thermal resistance. Fig.9(a) shows the model of thermal resistance of the package. Thermal resistance θ_{ja} , ambient temperature Ta, junction temperature Tj, and power dissipation Pd can be calculated by the equation below

$$\theta_{ja} = (T_j - T_a) / P_d \quad \text{°C/W} \quad \dots \dots \dots (I)$$

Derating curve in Fig.9(b) indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θ_{ja} . Thermal resistance θ_{ja} depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Fig.10(a) show a derating curve for an example of BD95820F-LB and BD95820N-LB.

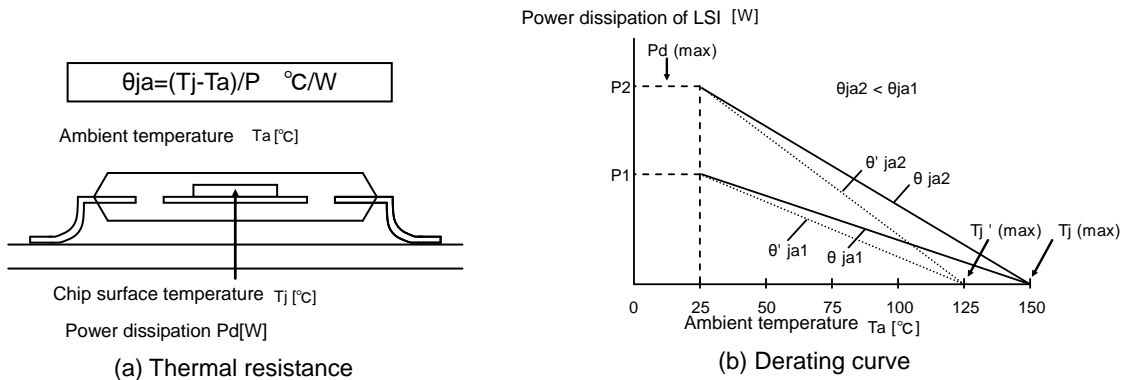
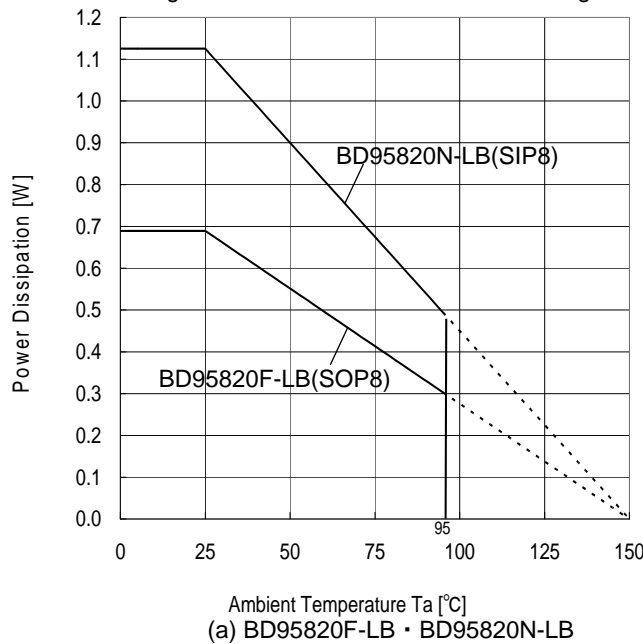


Figure 9. Thermal resistance and derating

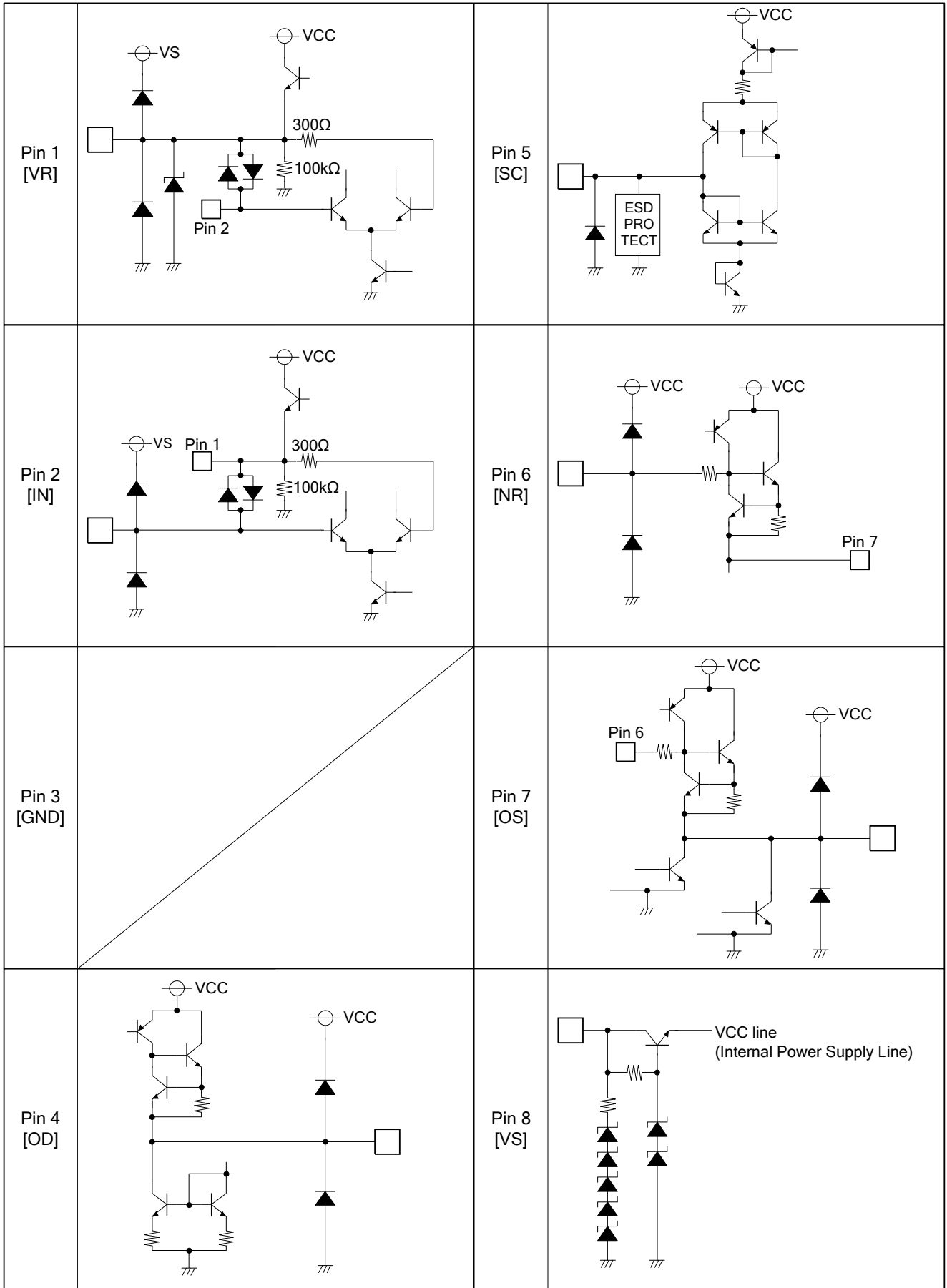


	Derating curve slope	UNIT
BD95820F-LB(SOP8)	5.5	mW/°C
BD95820N-LB(SIP8)	9.0	

When using the unit above Ta=25°C, subtract the value above per degree°C
 BD95820F-LB : Permissible dissipation is a value when glass epoxy board 70mmx70mmx1.6mm (cooper foil area below 3%) is mounted.
 BD95820N-LB : Permissible dissipation is a value in the package unit.

Figure 10. Derating curve

I/O equivalence circuit



Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin\ A$ and $GND > Pin\ B$, the P-N junction operates as a parasitic diode.
 When $GND > Pin\ B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

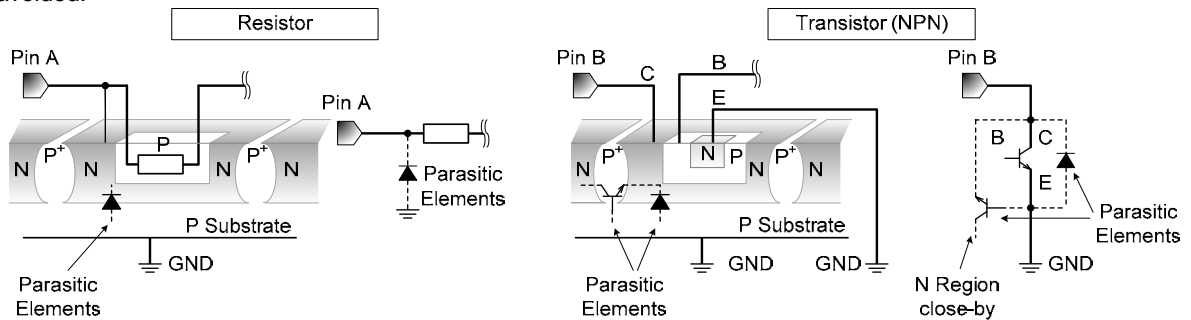


Figure 11. Example of monolithic IC structure

13. Input Resistance R_{IN}

Input resistance R_{IN} sets it in less than $3k\Omega$.

The input bias current to IN terminal increases at the time of the power supply start before reaching the operating power supply range, and when input resistance is lower than $3k\Omega$, the voltage between the input terminals becomes larger than trip voltage, and may malfunction.

Revision History

Date	Revision	Changes
13.Jun.2014	001	New Release

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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