

# SN74SSTVF16859

## 13-BIT TO 26-BIT REGISTERED BUFFER WITH SSTL\_2 INPUTS AND OUTPUTS

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- Member of the Texas Instruments Widebus™ Family
- Operates at 2.3 V to 2.7 V for PC1600, PC2100, and PC2700
- Operates at 2.5 V to 2.7 V for PC3200 (QFN Package)
- Pinout and Functionality Compatible With JEDEC Standard SSTV16859
- 600 ps Faster (Simultaneous Switching) Than the JEDEC Standard SSTV16859 in PC2700 DIMM Applications
- 1-to-2 Outputs to Support Stacked DDR DIMMs
- Output Edge-Control Circuitry Minimizes Switching Noise in an Unterminated Line
- Outputs Meet SSTL\_2 Class I Specifications
- Supports SSTL\_2 Data Inputs
- Differential Clock (CLK and  $\overline{\text{CLK}}$ ) Inputs
- Supports LVCMOS Switching Levels on the  $\overline{\text{RESET}}$  Input
- $\overline{\text{RESET}}$  Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low
- Pinout Optimizes DIMM PCB Layout
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DGG PACKAGE  
(TOP VIEW)

|                  |    |    |                           |
|------------------|----|----|---------------------------|
| Q13A             | 1  | 64 | V <sub>DDQ</sub>          |
| Q12A             | 2  | 63 | GND                       |
| Q11A             | 3  | 62 | D13                       |
| Q10A             | 4  | 61 | D12                       |
| Q9A              | 5  | 60 | V <sub>CC</sub>           |
| V <sub>DDQ</sub> | 6  | 59 | V <sub>DDQ</sub>          |
| GND              | 7  | 58 | GND                       |
| Q8A              | 8  | 57 | D11                       |
| Q7A              | 9  | 56 | D10                       |
| Q6A              | 10 | 55 | D9                        |
| Q5A              | 11 | 54 | GND                       |
| Q4A              | 12 | 53 | D8                        |
| Q3A              | 13 | 52 | D7                        |
| Q2A              | 14 | 51 | $\overline{\text{RESET}}$ |
| GND              | 15 | 50 | GND                       |
| Q1A              | 16 | 49 | $\overline{\text{CLK}}$   |
| Q13B             | 17 | 48 | CLK                       |
| V <sub>DDQ</sub> | 18 | 47 | V <sub>DDQ</sub>          |
| Q12B             | 19 | 46 | V <sub>CC</sub>           |
| Q11B             | 20 | 45 | V <sub>REF</sub>          |
| Q10B             | 21 | 44 | D6                        |
| Q9B              | 22 | 43 | GND                       |
| Q8B              | 23 | 42 | D5                        |
| Q7B              | 24 | 41 | D4                        |
| Q6B              | 25 | 40 | D3                        |
| GND              | 26 | 39 | GND                       |
| V <sub>DDQ</sub> | 27 | 38 | V <sub>DDQ</sub>          |
| Q5B              | 28 | 37 | V <sub>CC</sub>           |
| Q4B              | 29 | 36 | D2                        |
| Q3B              | 30 | 35 | D1                        |
| Q2B              | 31 | 34 | GND                       |
| Q1B              | 32 | 33 | V <sub>DDQ</sub>          |

### description/ordering information

This 13-bit to 26-bit registered buffer is designed for 2.3-V to 2.7-V V<sub>CC</sub> operation.

### ORDERING INFORMATION

| T <sub>A</sub> | PACKAGE†                     |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------------|---------------|-----------------------|------------------|
| 0°C to 70°C    | QFN – RGQ (Tin-Pb Finish)    | Tape and reel | SN74SSTVF16859SR      | SSF859           |
|                | QFN – RGQ (Matte-Tin Finish) |               | SN74SSTVF16859S8      |                  |
|                | TSSOP – DGG                  | Tape and reel | SN74SSTVF16859GR      | SSTVF16859       |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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WITH SSTL\_2 INPUTS AND OUTPUTS

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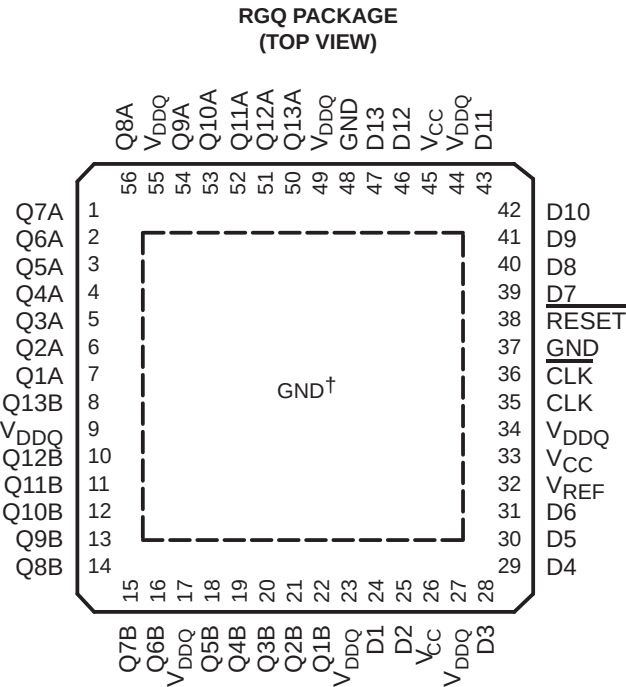
description/ordering information (continued)

All inputs are SSTL\_2, except the LVCMOS reset ( $\overline{\text{RESET}}$ ) input. All outputs are edge-controlled LVCMOS circuits optimized for unterminated DIMM loads.

The SN74SSTVF16859 operates from a differential clock (CLK and  $\overline{\text{CLK}}$ ). Data are registered at the crossing of CLK going high and  $\overline{\text{CLK}}$  going low.

The device supports low-power standby operation. When  $\overline{\text{RESET}}$  is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage ( $V_{\text{REF}}$ ) inputs are allowed. In addition, when  $\overline{\text{RESET}}$  is low, all registers are reset and all outputs are forced low. The LVCMOS  $\overline{\text{RESET}}$  input always must be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied,  $\overline{\text{RESET}}$  must be held in the low state during power up.



† The center die pad must be connected to GND.

FUNCTION TABLE

| INPUTS                    |               |                         |               | OUTPUT<br>Q    |
|---------------------------|---------------|-------------------------|---------------|----------------|
| $\overline{\text{RESET}}$ | CLK           | $\overline{\text{CLK}}$ | D             |                |
| H                         | ↑             | ↓                       | H             | H              |
| H                         | ↑             | ↓                       | L             | L              |
| H                         | L or H        | L or H                  | X             | Q <sub>0</sub> |
| L                         | X or floating | X or floating           | X or floating | L              |

The diagram illustrates the internal logic of one of the 13 channels in the AD7792. It shows the following components and connections:

- Inputs:** RESET (51), CLK (48), CLK (49), VREF (45), and D1 (35).
- Logic:** The inputs are connected to a network of inverters and AND gates. The output of the logic is connected to a 1D C1 R flip-flop.
- Flip-flop:** The flip-flop has inputs 1D, C1, and R. Its output is connected to two comparators.
- Comparators:** The comparators have outputs Q1A (16) and Q1B (32).
- Output:** The outputs Q1A and Q1B are connected to the output pins 16 and 32.
- Label:** The diagram is labeled "One of 13 Channels" and includes a note "To 12 Other Channels".

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# SN74SSTVF16859

## 13-BIT TO 26-BIT REGISTERED BUFFER

### WITH SSTL 2 INPUTS AND OUTPUTS

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#### recommended operating conditions (see Note 5)

|             |                                             |                              | MIN                    | NOM  | MAX                    | UNIT |
|-------------|---------------------------------------------|------------------------------|------------------------|------|------------------------|------|
| $V_{CC}$    | Supply voltage                              |                              | $V_{DDQ}$              |      | 2.7                    | V    |
| $V_{DDQ}$   | Output supply voltage                       | PC1600, PC2100, PC2700       | 2.3                    |      | 2.7                    | V    |
|             |                                             | PC3200                       | 2.5                    |      | 2.7                    | V    |
| $V_{REF}$   | Reference voltage ( $V_{REF} = V_{DDQ}/2$ ) | PC1600, PC2100, PC2700       | 1.15                   | 1.25 | 1.35                   | V    |
|             |                                             | PC3200                       | 1.25                   | 1.3  | 1.35                   | V    |
| $V_I$       | Input voltage                               |                              | 0                      |      | $V_{CC}$               | V    |
| $V_{IH}$    | AC high-level input voltage                 | Data inputs                  | $V_{REF}+310\text{mV}$ |      |                        | V    |
| $V_{IL}$    | AC low-level input voltage                  | Data inputs                  |                        |      | $V_{REF}-310\text{mV}$ | V    |
| $V_{IH}$    | DC high-level input voltage                 | Data inputs                  | $V_{REF}+150\text{mV}$ |      |                        | V    |
| $V_{IL}$    | DC low-level input voltage                  | Data inputs                  |                        |      | $V_{REF}-150\text{mV}$ | V    |
| $V_{IH}$    | High-level input voltage                    | $\overline{\text{RESET}}$    | 1.7                    |      |                        | V    |
| $V_{IL}$    | Low-level input voltage                     | $\overline{\text{RESET}}$    |                        |      | 0.7                    | V    |
| $V_{ICR}$   | Common-mode input voltage range             | CLK, $\overline{\text{CLK}}$ | 0.97                   |      | 1.53                   | V    |
| $V_{I(PP)}$ | Peak-to-peak input voltage                  | CLK, $\overline{\text{CLK}}$ | 360                    |      |                        | mV   |
| $I_{OH}$    | High-level output current                   |                              |                        |      | -16                    | mA   |
| $I_{OL}$    | Low-level output current                    |                              |                        |      | 16                     | mA   |
| $T_A$       | Operating free-air temperature              |                              | 0                      |      | 70                     | °C   |

NOTE 5: The  $\overline{\text{RESET}}$  input of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless  $\overline{\text{RESET}}$  is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

#### electrical characteristics for PC1600, PC2100, and PC2700 over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                   |                                         | TEST CONDITIONS                                                                                                                                                                                     |  | V <sub>CC</sub> <sup>†</sup> | MIN                   | TYP <sup>‡</sup> | MAX  | UNIT                 |
|-----------------------------|-----------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|------------------------------|-----------------------|------------------|------|----------------------|
| V <sub>IK</sub>             |                                         | I <sub>I</sub> = −18 mA                                                                                                                                                                             |  | 2.3 V                        |                       |                  | −1.2 | V                    |
| V <sub>OH</sub>             |                                         | I <sub>OH</sub> = −100 μA                                                                                                                                                                           |  | 2.3 V to 2.7 V               | V <sub>DDQ</sub> −0.2 |                  |      | V                    |
|                             |                                         | I <sub>OH</sub> = −8 mA                                                                                                                                                                             |  | 2.3 V                        | 1.95                  |                  |      |                      |
| V <sub>OL</sub>             |                                         | I <sub>OL</sub> = 100 μA                                                                                                                                                                            |  | 2.3 V to 2.7 V               | 0.2                   |                  |      | V                    |
|                             |                                         | I <sub>OL</sub> = 8 mA                                                                                                                                                                              |  | 2.3 V                        | 0.35                  |                  |      |                      |
| I <sub>I</sub>              | All inputs                              | V <sub>I</sub> = V <sub>CC</sub> or GND                                                                                                                                                             |  | 2.7 V                        |                       |                  | ±5   | μA                   |
| I <sub>CC</sub>             | Static standby                          | RESET = GND                                                                                                                                                                                         |  | 2.7 V                        |                       |                  | 10   | μA                   |
|                             | Static operating                        | RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH</sub> (AC) or V <sub>IL</sub> (AC)                                                                                                             |  |                              |                       |                  | 25   | mA                   |
| I <sub>CCD</sub>            | Dynamic operating – clock only          | RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH</sub> (AC) or V <sub>IL</sub> (AC), CLK and CLK switching 50% duty cycle                                                                       |  | 2.5 V                        |                       |                  | 19   | μA/MHz               |
|                             | Dynamic operating – per each data input | RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH</sub> (AC) or V <sub>IL</sub> (AC), CLK and CLK switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle |  |                              |                       |                  | 7    | μA/clock MHz/D input |
| C <sub>i</sub> <sup>§</sup> | Data inputs                             | V <sub>I</sub> = V <sub>REF</sub> ± 310 mV                                                                                                                                                          |  | 2.5 V                        |                       |                  | 2.5  | pF                   |
|                             | CLK, CLK                                | V <sub>ICR</sub> = 1.25 V, V <sub>I</sub> (PP) = 360mV                                                                                                                                              |  |                              |                       |                  | 2.5  |                      |
|                             | RESET                                   | V <sub>I</sub> = V <sub>CC</sub> or GND                                                                                                                                                             |  |                              |                       |                  | 2.3  |                      |

$^\dagger$  For this test condition,  $V_{DDQ}$  always is equal to  $V_{CC}$ .

$^\ddagger$  All typical values are at  $V_{CC} = 2.5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

$^\S$  Measured at 50-MHz input frequency



**electrical characteristics for PC3200 over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER                   |                                         | TEST CONDITIONS                                                                                                                                                                                     | V <sub>CC</sub> <sup>†</sup> | MIN                   | TYP <sup>‡</sup> | MAX  | UNIT                 |
|-----------------------------|-----------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|-----------------------|------------------|------|----------------------|
| V <sub>IK</sub>             |                                         | I <sub>I</sub> = -18 mA                                                                                                                                                                             | 2.5 V                        |                       |                  | -1.2 | V                    |
| V <sub>OH</sub>             |                                         | I <sub>OH</sub> = -100 µA                                                                                                                                                                           | 2.5 V to 2.7 V               | V <sub>DDQ</sub> -0.2 |                  |      | V                    |
|                             |                                         | I <sub>OH</sub> = -8 mA                                                                                                                                                                             | 2.5 V                        | 1.95                  |                  |      |                      |
| V <sub>OL</sub>             |                                         | I <sub>OL</sub> = 100 µA                                                                                                                                                                            | 2.5 V to 2.7 V               |                       |                  | 0.2  | V                    |
|                             |                                         | I <sub>OL</sub> = 8 mA                                                                                                                                                                              | 2.5 V                        |                       |                  | 0.35 |                      |
| I <sub>I</sub>              | All inputs                              | V <sub>I</sub> = V <sub>CC</sub> or GND                                                                                                                                                             | 2.7 V                        |                       |                  | ±5   | µA                   |
| I <sub>CC</sub>             | Static standby                          | RESET = GND                                                                                                                                                                                         | 2.7 V                        |                       |                  | 10   | µA                   |
|                             | Static operating                        | RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH</sub> (AC) or V <sub>IL</sub> (AC)                                                                                                             |                              |                       |                  | 25   | mA                   |
| I <sub>CCD</sub>            | Dynamic operating – clock only          | RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH</sub> (AC) or V <sub>IL</sub> (AC), CLK and CLK switching 50% duty cycle                                                                       | 2.6 V                        |                       |                  | 19   | µA/MHz               |
|                             | Dynamic operating – per each data input | RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH</sub> (AC) or V <sub>IL</sub> (AC), CLK and CLK switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle |                              |                       |                  | 7    | µA/clock MHz/D input |
| C <sub>i</sub> <sup>§</sup> | Data inputs                             | V <sub>I</sub> = V <sub>REF</sub> ± 310 mV                                                                                                                                                          | 2.6 V                        | 2.5                   | 3                | 3.5  | pF                   |
|                             | CLK, CLK                                | V <sub>ICR</sub> = 1.25 V, V <sub>I</sub> (PP) = 360mV                                                                                                                                              |                              | 2.5                   | 3                | 3.5  |                      |
|                             | RESET                                   | V <sub>I</sub> = V <sub>CC</sub> or GND                                                                                                                                                             |                              | 2.3                   | 3                | 3.5  |                      |

<sup>†</sup> For this test condition, V<sub>DDQ</sub> always is equal to V<sub>CC</sub>.

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 2.6 V, T<sub>A</sub> = 25°C.

<sup>§</sup> Measured at 50-MHz input frequency

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

|                    |                                                |                                     | V <sub>CC</sub> = 2.5 V<br>± 0.2 V <sup>†</sup> |     | V <sub>CC</sub> = 2.6 V<br>± 0.1 V <sup>†</sup> |      | UNIT |
|--------------------|------------------------------------------------|-------------------------------------|-------------------------------------------------|-----|-------------------------------------------------|------|------|
|                    |                                                |                                     | MIN                                             | MAX | MIN                                             | MAX  |      |
| f <sub>clock</sub> | Clock frequency                                |                                     | 500                                             |     | 500                                             |      | MHz  |
| t <sub>w</sub>     | Pulse duration, CLK, CLK high or low           |                                     | 1                                               |     | 1                                               |      | ns   |
| t <sub>act</sub>   | Differential inputs active time (see Note 6)   |                                     | 22                                              |     | 22                                              |      | ns   |
| t <sub>inact</sub> | Differential inputs inactive time (see Note 7) |                                     | 22                                              |     | 22                                              |      | ns   |
| t <sub>su</sub>    | Setup time                                     | Fast slew rate (see Notes 8 and 10) | Data before CLK↑, CLK↓                          |     | 0.65                                            | 0.65 | ns   |
|                    |                                                | Slow slew rate (see Notes 9 and 10) |                                                 |     | 0.75                                            | 0.75 |      |
| t <sub>h</sub>     | Hold time                                      | Fast slew rate (see Notes 8 and 10) | Data after CLK↑, CLK↓                           |     | 0.65                                            | 0.65 | ns   |
|                    |                                                | Slow slew rate (see Notes 9 and 10) |                                                 |     | 0.8                                             | 0.8  |      |

<sup>†</sup> For this test condition, V<sub>DDQ</sub> always is equal to V<sub>CC</sub>.

- NOTES: 6. V<sub>REF</sub> must be held at a valid input level, and data inputs must be held low for a minimum time of t<sub>act</sub> max, after RESET is taken high.  
7. V<sub>REF</sub>, data, and clock inputs must be held at valid voltage levels (not floating) for a minimum time of t<sub>inact</sub> max, after RESET is taken low.  
8. For data signal input slew rate ≥1 V/ns.  
9. For data signal input slew rate ≥0.5 V/ns and <1 V/ns.  
10. CLK, CLK signals input slew rates are ≥1 V/ns.

# SN74SSTVF16859

## 13-BIT TO 26-BIT REGISTERED BUFFER

### WITH SSTL 2 INPUTS AND OUTPUTS

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switching characteristics for TSSOP over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER         | FROM<br>(INPUT)                 | TO<br>(OUTPUT) | $V_{CC} = 2.5\text{ V}$<br>$\pm 0.2\text{ V}^\dagger$ |     | UNIT |
|-------------------|---------------------------------|----------------|-------------------------------------------------------|-----|------|
|                   |                                 |                | MIN                                                   | MAX |      |
| $f_{\max}$        |                                 |                | 500                                                   |     | MHz  |
| $t_{pd}^\ddagger$ | CLK and $\overline{\text{CLK}}$ | Q              | 1.1                                                   | 2.5 | ns   |
| $t_{PHL}$         | $\overline{\text{RESET}}$       | Q              |                                                       | 5   | ns   |

<sup>†</sup> For this test condition,  $V_{DDQ}$  always is equal to  $V_{CC}$ .

<sup>‡</sup> Single-bit switching

switching characteristics for QFN over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER         | FROM<br>(INPUT)                 | TO<br>(OUTPUT) | $V_{CC} = 2.5\text{ V}$<br>$\pm 0.2\text{ V}^\dagger$ |     | $V_{CC} = 2.6\text{ V}$<br>$\pm 0.1\text{ V}^\dagger$ |     | UNIT |
|-------------------|---------------------------------|----------------|-------------------------------------------------------|-----|-------------------------------------------------------|-----|------|
|                   |                                 |                | MIN                                                   | MAX | MIN                                                   | MAX |      |
| $f_{\max}$        |                                 |                | 500                                                   |     | 500                                                   |     | MHz  |
| $t_{pd}^\ddagger$ | CLK and $\overline{\text{CLK}}$ | Q              | 1.1                                                   | 2.5 | 1.1                                                   | 2.2 | ns   |
| $t_{PHL}$         | $\overline{\text{RESET}}$       | Q              |                                                       | 5   |                                                       | 5   | ns   |

<sup>†</sup> For this test condition,  $V_{DDQ}$  always is equal to  $V_{CC}$ .

<sup>‡</sup> Single-bit switching

output slew rates over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

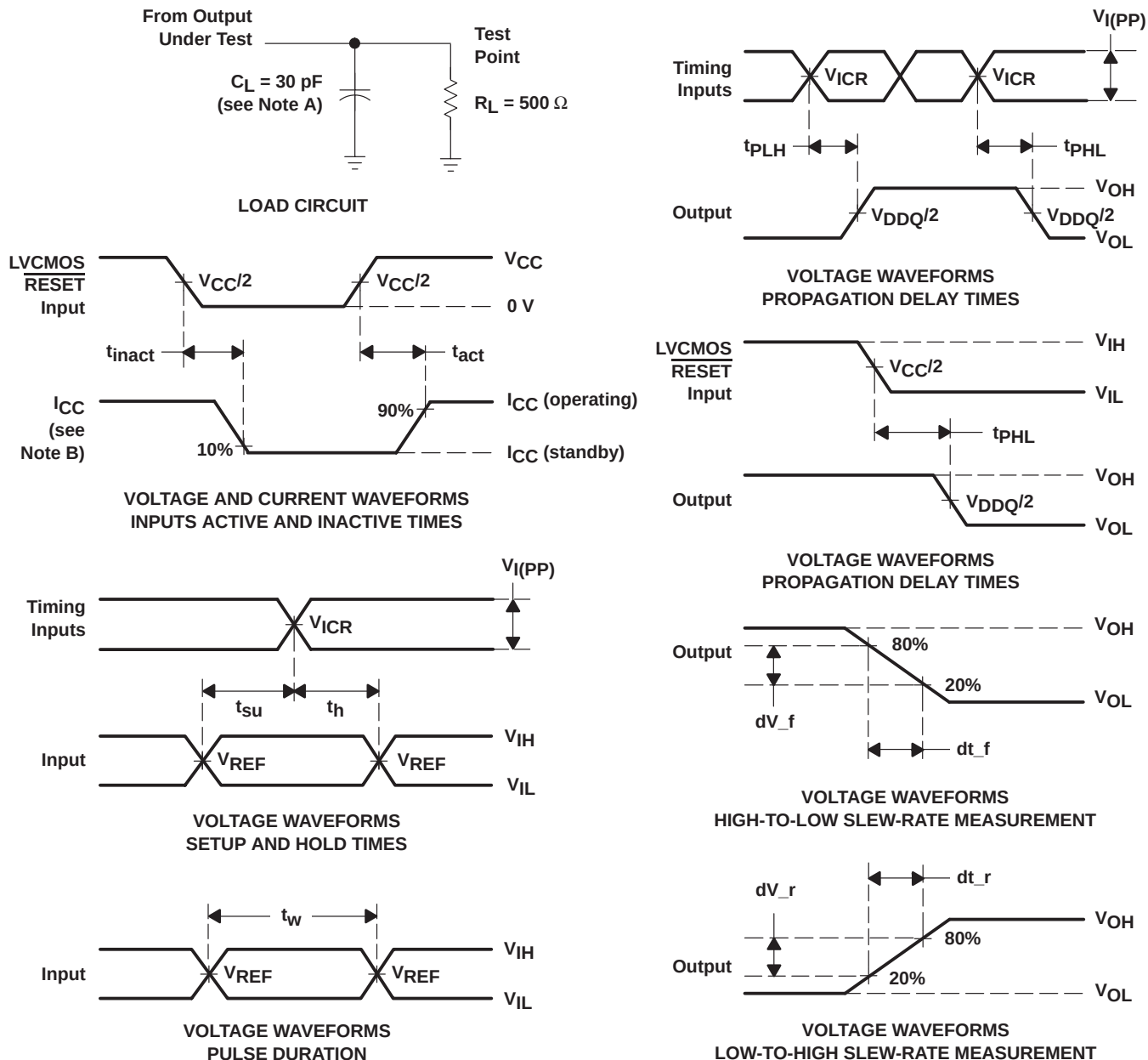
| PARAMETER           | FROM       | TO         | $V_{CC} = 2.5\text{ V}$<br>$\pm 0.2\text{ V}^\dagger$ |     | $V_{CC} = 2.6\text{ V}$<br>$\pm 0.1\text{ V}^\dagger$ |     | UNIT |
|---------------------|------------|------------|-------------------------------------------------------|-----|-------------------------------------------------------|-----|------|
|                     |            |            | MIN                                                   | MAX | MIN                                                   | MAX |      |
| $dV/dt_r$           | 20%        | 80%        | 1                                                     | 4   | 1                                                     | 4   | V/ns |
| $dV/dt_f$           | 80%        | 20%        | 1                                                     | 4   | 1                                                     | 4   | V/ns |
| $dV/dt_{\Delta}^\S$ | 20% or 80% | 80% or 20% |                                                       | 1   |                                                       | 1   | V/ns |

<sup>†</sup> For this test condition,  $V_{DDQ}$  always is equal to  $V_{CC}$ .

<sup>§</sup> Difference between  $dV/dt_r$  (rising edge rate) and  $dV/dt_f$  (falling edge rate).

## PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  AND  $V_{CC} = 2.6\text{ V} \pm 0.1\text{ V}$



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B.  $I_{CC}$  tested with clock and data inputs held at  $V_{CC}$  or GND, and  $I_O = 0\text{ mA}$ .
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ , input slew rate  $= 1\text{ V/ns} \pm 20\%$  (unless otherwise noted).
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $V_{TT} = V_{REF} = V_{DDQ}/2$
  - F.  $V_{IH} = V_{REF} + 310\text{ mV}$  (ac voltage levels) for differential inputs.  $V_{IH} = V_{CC}$  for LVC MOS input.
  - G.  $V_{IL} = V_{REF} - 310\text{ mV}$  (ac voltage levels) for differential inputs.  $V_{IL} = \text{GND}$  for LVC MOS input.
  - H.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device   | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|--------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| 74SSTVF16859G4RG4  | ACTIVE        | VQFN         | RGQ                | 56   | 2000           | Green (RoHS<br>& no Sb/Br) | CU                      | Level-3-260C-168 HR  | 0 to 70      | SSF859                  | <a href="#">Samples</a> |
| HPA00025S8         | ACTIVE        | VQFN         | RGQ                | 56   | 2000           | Green (RoHS<br>& no Sb/Br) | CU                      | Level-3-260C-168 HR  | 0 to 70      | SSF859                  | <a href="#">Samples</a> |
| SN74SSTVF16859G4R  | ACTIVE        | VQFN         | RGQ                | 56   | 2000           | Green (RoHS<br>& no Sb/Br) | CU                      | Level-3-260C-168 HR  | 0 to 70      | SSF859                  | <a href="#">Samples</a> |
| SN74SSTVF16859GR   | ACTIVE        | TSSOP        | DGG                | 64   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | 0 to 70      | SSTVF16859              | <a href="#">Samples</a> |
| SN74SSTVF16859GRG4 | ACTIVE        | TSSOP        | DGG                | 64   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | 0 to 70      | SSTVF16859              | <a href="#">Samples</a> |
| SN74SSTVF16859S8   | ACTIVE        | VQFN         | RGQ                | 56   | 2000           | Green (RoHS<br>& no Sb/Br) | CU                      | Level-3-260C-168 HR  | 0 to 70      | SSF859                  | <a href="#">Samples</a> |
| SN74SSTVF16859S8G3 | ACTIVE        | VQFN         | RGQ                | 56   | 2000           | Green (RoHS<br>& no Sb/Br) | CU                      | Level-3-260C-168 HR  | 0 to 70      | SSF859                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

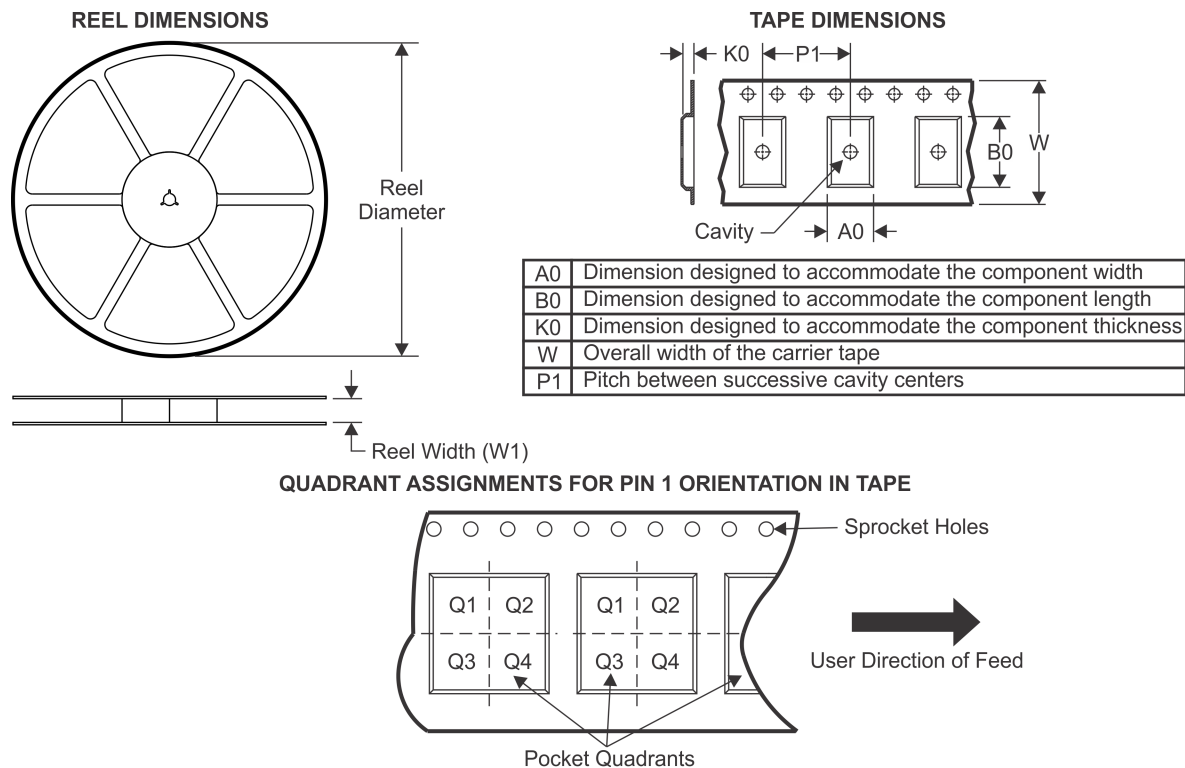
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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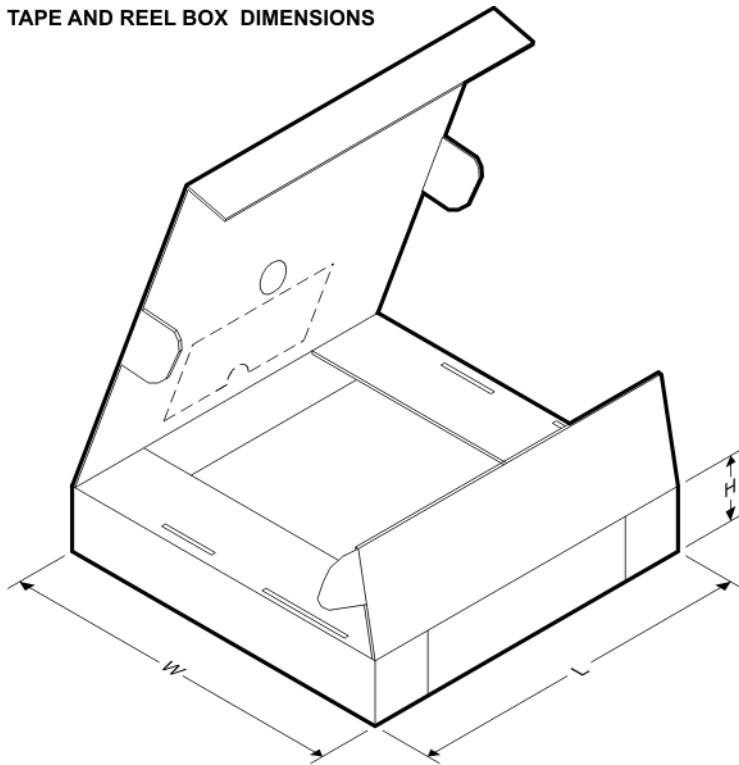
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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74SSTVF16859GR | TSSOP        | DGG             | 64   | 2000 | 330.0              | 24.4               | 8.4     | 17.3    | 1.7     | 12.0    | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

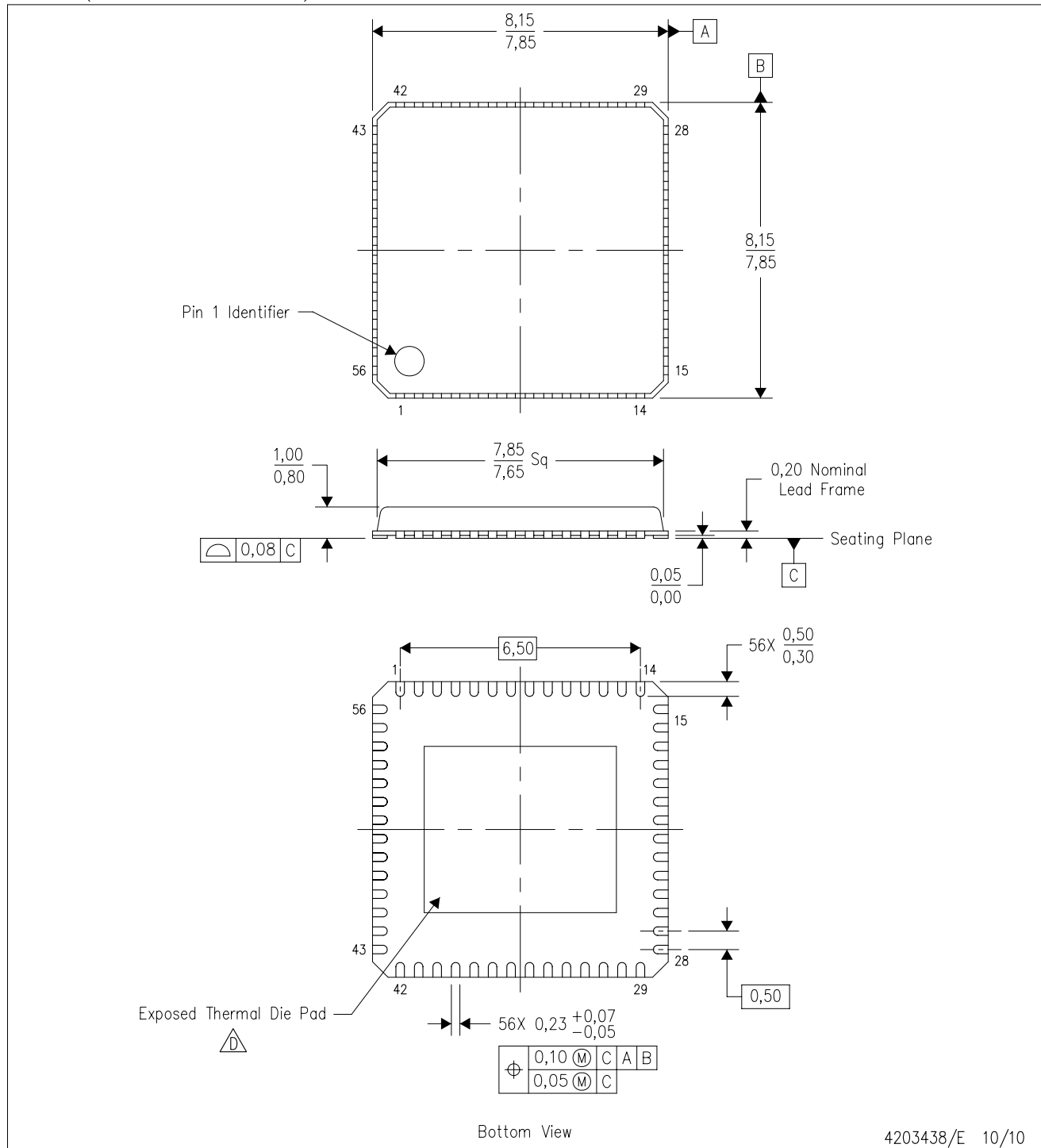


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74SSTVF16859GR | TSSOP        | DGG             | 64   | 2000 | 367.0       | 367.0      | 45.0        |

RGQ (S-PVQFN-N56)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) Package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Package complies to JEDEC MO-220 variation VLLD-2.

RGQ (S-PVQFN-N56)

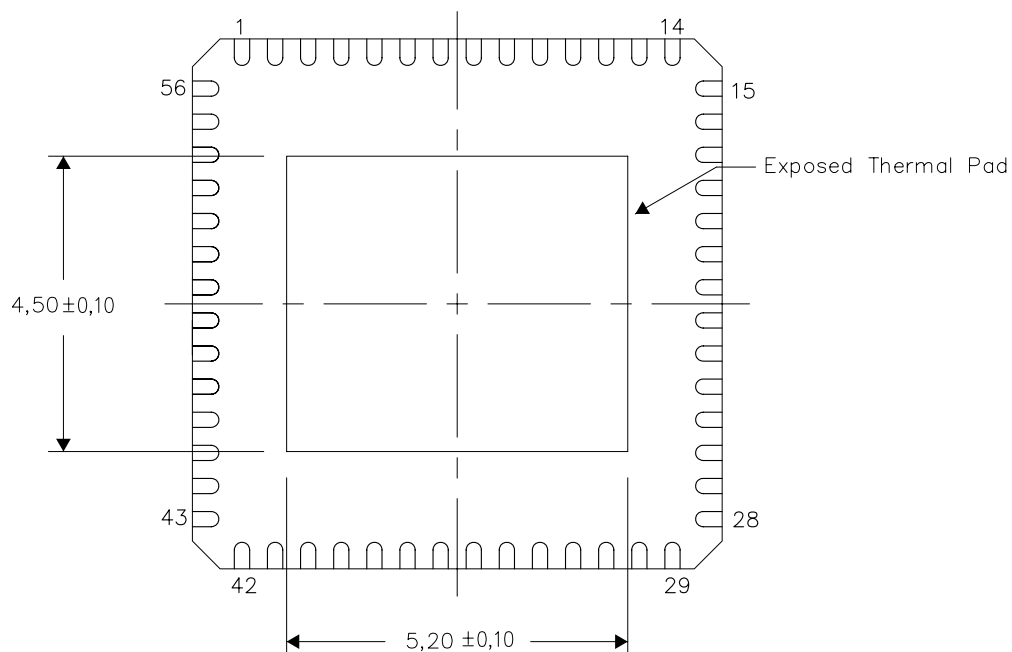
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206347/D 12/10

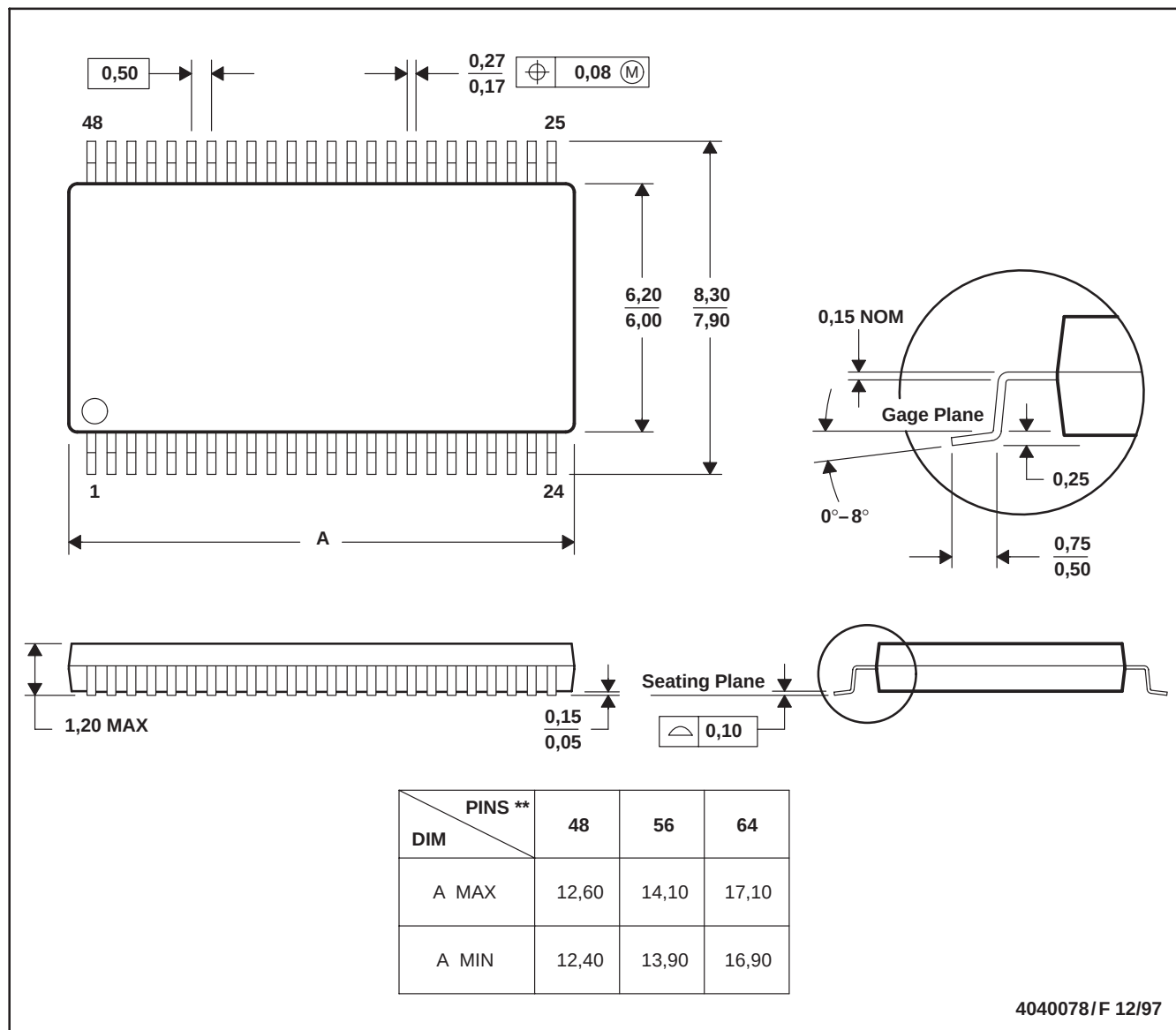
NOTE: A. All linear dimensions are in millimeters



## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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