Feature

- Logic Operating Voltage: 2.4V~5.5V
- Integrated oscillator circuitry
- Bias: 1/3 or 1/4
- Internal LCD bias generation with voltage-follower buffers
- External V_{LCD} pin to supply LCD operating voltage
- Support I^2C-bus serial interface
- Integrated voltage adjustment function for LCD driving voltage
- Up to 39×8 bits RAM for display data storage
- Display patterns
  - HT9B95A: 35×8 patterns - 35 segments and 8 commons
  - HT9B95B: 39×8 patterns - 39 segments and 8 commons
    43×4 patterns - 43 segments and 4 commons
  - HT9B95G: 39×8 patterns - 39 segments and 8 commons
    43×4 patterns - 43 segments and 4 commons
- Support Power Save Mode for low power consumption
- Package Type
  - HT9B95A: 48-pin TSSOP, 52-pin LQFP
  - HT9B95B: 52-pin LQFP
  - HT9B95G: COG

Selection Table

Part No.	COM	SEG	Package
HT9B95A	8	35	48TSSOP, 52LQFP
HT9B95B	8	39	52LQFP
	4	43	
HT9B95G	8	39	COG
	4	43	

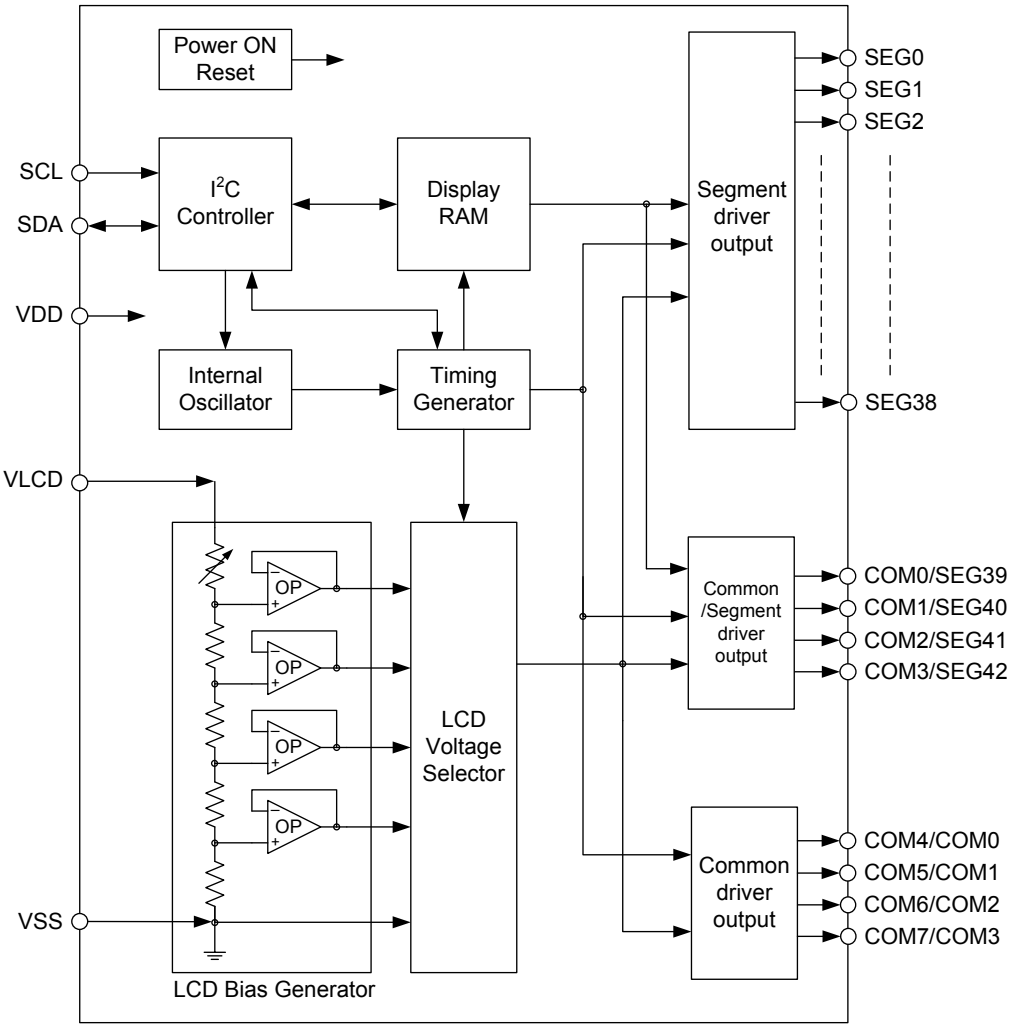
Applications

- Leisure products
- Telephone display
- Household appliance
- Consumer electronics

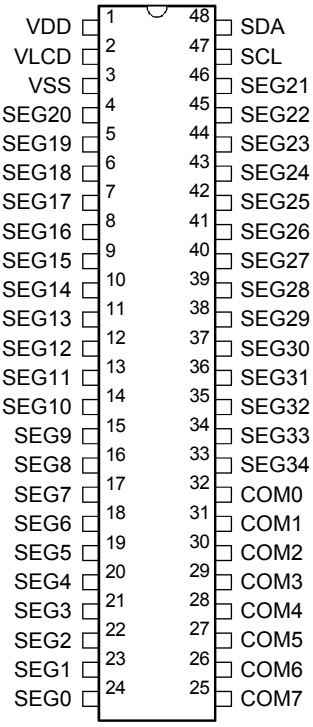
General Description

The HT9B95 is a memory mappling and multi-function LCD controller driver. The maximum display segments of the device are 312 patterns (39 segments and 8 commons) or 280 patterns (35 segments and 8 commons) display depending upon which device is selected. The software configuration feature of the HT9B95 device makes it suitable for multiple LCD applications including LCD modules and display subsystems. The HT9B95 device communicates with most microprocessors / microcontrollers via a two-wire bidirectional I^2C-bus interface.

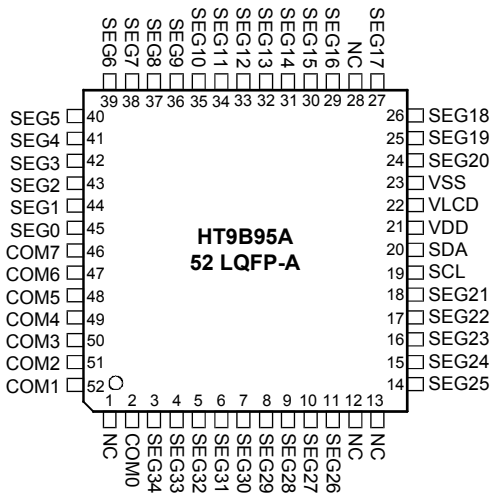
Block Diagram



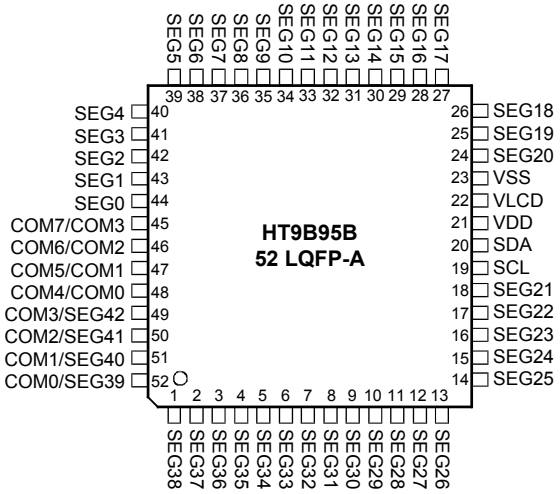
Pin Assignment



HT9B95A
48 TSSOP-A

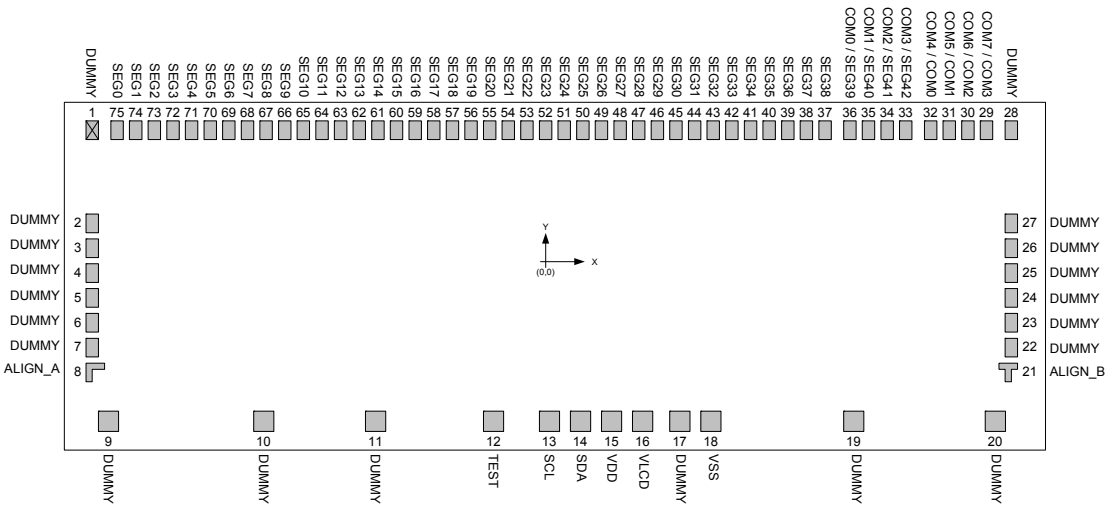


HT9B95A
52 LQFP-A



HT9B95B
52 LQFP-A

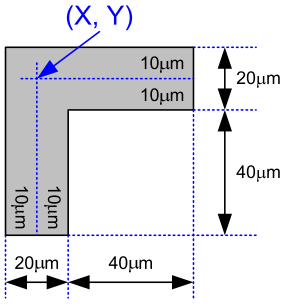
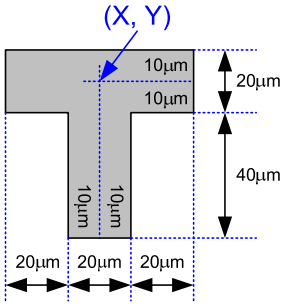
Pad Assignment for COG − HT9B95G



Pad Dimensions for COG

Item	Pad Number	Size		Unit
		X	Y	
Chip size	—	3108	1132	μm
Chip thickness	—	508		μm
Pad pitch	1, 28~75	60		μm
	2~7, 22~27	80		μm
	9~20	>80		μm
Bump size	1, 28~75	40	60	μm
	2~7, 22~27	40	60	μm
	9~20	67	67	μm
Bump height	All pad	18±3		μm

Alignment Mark Dimensions for COG

Item	Number	Size	Unit
ALIGN_A	8		μm
ALIGN_B	21		μm

Pad Coordinates for COG

Unit: μm

No.	Name	X	Y	No.	Name	X	Y
1	DUMMY	-1470.500	472.500	39	SEG36	762.700	472.500
2	DUMMY	-1470.500	136.340	40	SEG35	702.700	472.500
3	DUMMY	-1470.500	56.340	41	SEG34	642.700	472.500
4	DUMMY	-1470.500	-23.660	42	SEG33	582.700	472.500
5	DUMMY	-1470.500	-103.660	43	SEG32	522.700	472.500
6	DUMMY	-1470.500	-183.660	44	SEG31	462.700	472.500
7	DUMMY	-1470.500	-263.660	45	SEG30	402.700	472.500
8	ALIGN_A	-1477.000	-330.000	46	SEG29	342.700	472.500
9	DUMMY	-1457.000	-469.000	47	SEG28	282.700	472.500
10	DUMMY	-923.150	-469.000	48	SEG27	222.700	472.500
11	DUMMY	-552.600	-469.000	49	SEG26	162.700	472.500
12	TEST	-187.900	-469.000	50	SEG25	102.700	472.500
13	SCL	4.100	-468.000	51	SEG24	42.700	472.500
14	SDA	89.100	-468.000	52	SEG23	-17.300	472.500
15	VDD	182.900	-468.000	53	SEG22	-77.300	472.500
16	VLCD	270.950	-469.000	54	SEG21	-137.300	472.500
17	DUMMY	406.900	-469.000	55	SEG20	-197.300	472.500
18	VSS	490.950	-469.000	56	SEG19	-257.300	472.500
19	DUMMY	963.600	-469.000	57	SEG18	-317.300	472.500
20	DUMMY	1457.000	-469.000	58	SEG17	-377.300	472.500
21	ALIGN_B	1458.000	-330.000	59	SEG16	-437.300	472.500
22	DUMMY	1470.500	-260.810	60	SEG15	-497.300	472.500
23	DUMMY	1470.500	-180.810	61	SEG14	-557.300	472.500

No.	Name	X	Y	No.	Name	X	Y
24	DUMMY	1470.500	-100.810	62	SEG13	-617.300	472.500
25	DUMMY	1470.500	-20.810	63	SEG12	-677.300	472.500
26	DUMMY	1470.500	59.190	64	SEG11	-737.300	472.500
27	DUMMY	1470.500	139.190	65	SEG10	-797.300	472.500
28	DUMMY	1470.500	472.500	66	SEG9	-857.300	472.500
29	COM7/COM3	1396.300	472.500	67	SEG8	-917.300	472.500
30	COM6/COM2	1336.300	472.500	68	SEG7	-977.300	472.500
31	COM5/COM1	1276.300	472.500	69	SEG6	-1037.300	472.500
32	COM4/COM0	1216.300	472.500	70	SEG5	-1097.300	472.500
33	COM3/SEG42	1147.700	472.500	71	SEG4	-1157.300	472.500
34	COM2/SEG41	1087.700	472.500	72	SEG3	-1217.300	472.500
35	COM1/SEG40	1027.700	472.500	73	SEG2	-1277.300	472.500
36	COM0/SEG39	967.700	472.500	74	SEG1	-1337.300	472.500
37	SEG38	882.700	472.500	75	SEG0	-1397.300	472.500
38	SEG37	822.700	472.500				

Pin Description

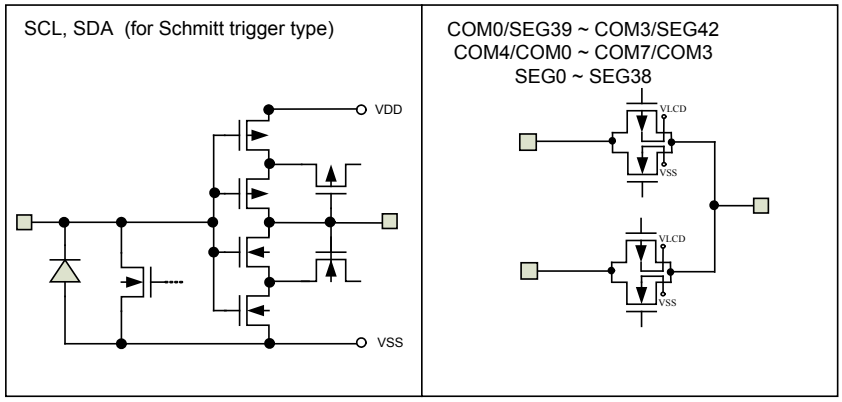
HT9B95A

Pin Name	Type	Description
SDA	I/O	Serial Data Input/Output pin Serial Data (SDA) Input/Output for 2-wire I^2C interface is an NMOS open drain structure.
SCL	I	Serial Clock Input pin Serial Data (SCL) is a clock input for 2-wire I^2C interface.
COM0~COM7	O	LCD Common outputs.
SEG0~SEG34	O	LCD Segment outputs.
VDD	—	Positive power supply.
VSS	—	Negative power supply, ground.
VLCD	—	LCD power supply pin

HT9B95B/HT9B95G

Pin Name	Type	Description
SDA	I/O	Serial Data Input/Output pin Serial Data (SDA) Input/Output for 2-wire I^2C interface is an NMOS open drain structure.
SCL	I	Serial Clock Input pin Serial Data (SCL) is a clock input for 2-wire I^2C interface.
COM0/SEG39 ~ COM3/SEG42	O	LCD common or segment outputs These pins are set to COM0 ~ COM3 when 1/8 duty is set These pins are set to SEG39 ~ SEG42 when 1/4 duty is set
COM4/COM0 ~ COM7/COM3	O	LCD Common outputs. These pins are set to COM4 ~ COM7 when 1/8 duty is set These pins are set to COM0 ~ COM3 when 1/4 duty is set
SEG0~SEG38	O	LCD Segment outputs.
VDD	—	Positive power supply.
VSS	—	Negative power supply, ground.
VLCD	—	LCD power supply pin
TEST	—	TEST pin in HT9B95G, keep floating. Only available in HT9B95G.
DUMMY	—	Dummy pin, keep floating. Only available in HT9B95G.

Approximate Internal Connections



Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V ~ V_{SS}+6.5V

Input Voltage ..... V_{SS}-0.3V ~ V_{DD}+0.3V

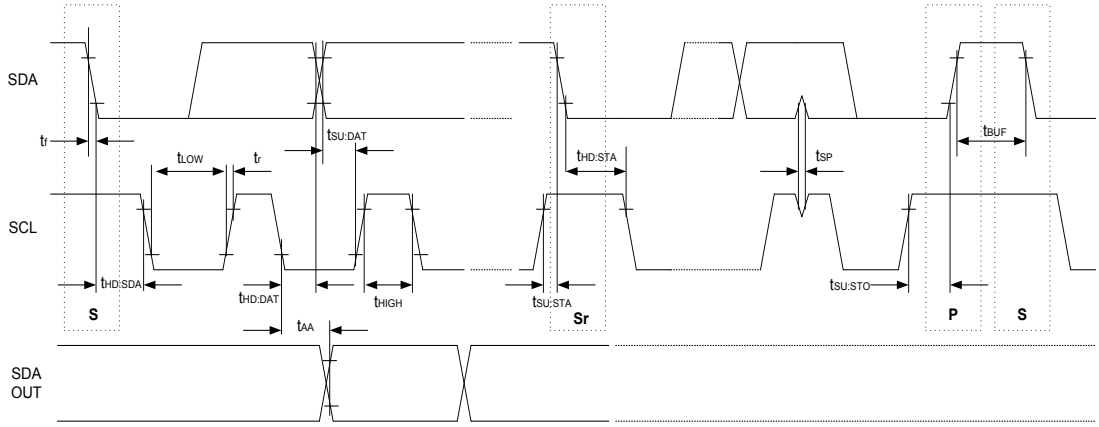
Storage Temperature ..... -55°C ~ 150°C

Operating Temperature ..... -40°C ~ 85°C

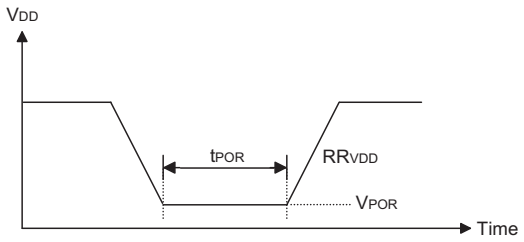
Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to these devices. Functional operation of these devices at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect devices reliability.

Timing Diagrams

I²C Timing



Power On Reset Timing



Note: 1. If the conditions of Reset timing are not satisfied in power ON/OFF sequence, the internal Power on Reset (POR) circuit will not operate normally.

2. If it is difficult to meet power on reset timing conditions, please execute software reset command after Power on.

D.C. Characteristics

V_{SS} = 0V; V_{DD} =2.4V to 5.5V; Ta = -40°C to +85°C

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	—	2.4	—	5.5	V
V_{LCD}	LCD Operating Voltage	—	—	2.5	—	5.5	V
V_{IH}	Input High Voltage	—	SCL, SDA	0.7V_{DD}	—	V_{DD}	V
V_{IL}	Input Low Voltage	—	SCL, SDA	0	—	0.3V_{DD}	V
I_{IL}	Input Leakage Current	—	V_{IN}=V_{SS} or V_{DD}	-1	—	1	μA
I_{OL}	Low Level Output Current	3.3V	V_{OL}=0.4V for SDA pin	6	—	—	mA
		5.0V		9	—	—	mA
I_{DD}	Operating Current	3.3V	V_{LCD}=V_{DD}, No load, Ta=25°C, LCD display on, f_{LCD}=80Hz, 1/4 bias, 1/8 duty, B type inversion, Power save mode = Low Current2 mode	—	3	10	μA
		5.0V		—	5	20	μA
I_{LCD}	Operating Current	3.3V	V_{LCD}=V_{DD}, No load, Ta=25°C, LCD display on, f_{LCD}=80Hz, 1/4 bias, 1/8 duty, B type inversion, Power save mode = Low Current2 mode	—	5	20	μA
		5.0V		—	6	30	μA
I_{STB}	Standby Current	3.3V	V_{LCD}=V_{DD}, No load, Ta=25°C, LCD display off, f_{LCD}=80Hz, 1/4 bias, 1/8 duty, B type inversion, Power save mode = Low Current2 mode	—	—	1	μA
		5.0V		—	—	2	μA
I_{OL1}	LCD Common Sink Current	—	V_{LCD}=3.3V, V_{OL}=0.33V	250	400	—	μA
			V_{LCD}=5V, V_{OL}=0.5V	500	800	—	μA
I_{OH1}	LCD Common Source Current	—	V_{LCD}=3.3V, V_{OH}=2.97V	-140	-230	—	μA
			V_{LCD}=5V, V_{OH}=4.5V	-300	-500	—	μA
I_{OL2}	LCD Segment Sink Current	—	V_{LCD}=3.3V, V_{OL}=0.33V	250	400	—	μA
			V_{LCD}=5V, V_{OL}=0.5V	500	800	—	μA
I_{OH2}	LCD Segment Source Current	—	V_{LCD}=3.3V, V_{OH}=2.97V	-140	-230	—	μA
			V_{LCD}=5V, V_{OH}=4.5V	-300	-500	—	μA

A.C. Characteristics

V_{SS} = 0V; V_{DD} =2.4V to 5.5V; Ta= -40°C to +85 °C

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
		V_{DD}	condition				
f_{LCD1}	LCD Frame Frequency	3.3V	Ta=25°C, internal oscillator is used, LCD frame frequency = 80 Hz	72	80	88	Hz
			Ta=25°C, internal oscillator is used, LCD frame frequency = 71 Hz	63.9	71	78.1	
			Ta=25°C, internal oscillator is used, LCD frame frequency = 64 Hz	57.6	64	70.4	
			Ta=25°C, internal oscillator is used, LCD frame frequency = 50Hz	45	50	55	
f_{LCD2}	LCD Frame Frequency	2.4~5.5V	Ta=-40 to 85°C, internal oscillator is used, LCD frame frequency = 80 Hz	56	80	104	Hz
			Ta=-40 to 85°C, internal oscillator is used, LCD frame frequency = 71 Hz	49.7	71	92.3	
			Ta=-40 to 85°C, internal oscillator is used, LCD frame frequency = 64 Hz	44.8	64	83.2	
			Ta=-40 to 85°C, internal oscillator is used, LCD frame frequency = 50Hz	35.2	50	65	
V_{POR}	V_{DD} Start Voltage to ensure Poewr-on Reset	—	—	—	—	100	mV
RR_{VDD}	V_{DD} Rise Rate to ensure Power-on Reset	—	—	0.05	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} to remain at V_{POR} to ensure Power-on Reset	—	—	10	—	—	ms

I²C Interface Characteristics

Unless otherwise specified, V_{SS} = 0 V; V_{DD} = 2.4V to 5.5V; Ta=-40 to +85°C

Symbol	Parameter	Condition	Min.	Max.	Unit
f_{SCL}	Clock frequency	—	—	400	kHZ
t_{BUF}	bus free time	Time in which the bus must be free before a new transmission can start	1.3	—	μs
$t_{HD: STA}$	Start condition hold time	After this period, the first clock pulse is generated.	0.6	—	μs
t_{LOW}	SCL Low time	—	1.3	—	μs
t_{HIGH}	SCL High time	—	0.6	—	μs
$t_{SU: STA}$	Start condition setup time	Only relevant for repeated START condition.	0.6	—	μs
$t_{HD: DAT}$	Data hold time	—	0	—	ns
$t_{SU: DAT}$	Data setup time	—	100	—	ns
t_R	SDA and SCL rise time	Note	—	0.3	μs
t_F	SDA and SCL fall time	Note	—	0.3	μs
$t_{SU: STO}$	Stop condition set-up time	—	0.6	—	μs
t_{AA}	Output Valid from Clock	—	—	0.9	μs
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	50	ns

Note: These parameters are periodically sampled but not 100% tested.

Functional Description

Power-On Reset

When the power is applied, the device is initialized by an internal power-on reset circuit. The status of the internal circuits after initialization is as follows:

- All common outputs are set to V_{SS}.
- All segment outputs are set to V_{SS}.
- LCD Driver Output Waveform: B-type inversion.
- Internal oscillator is selected.
- The 1/3 bias drive mode is selected.
- LCD bias generator is in an off state.
- LCD Display and internal oscillator are in off states.
- Power save mode is set to normal current.
- Frame Frequency is set to 80Hz.
- Blinking function is switched off

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

System Oscillator

The timing for the internal logic and the LCD drive signals are generated by the internal oscillator. The System Clock frequency (f_{SYS}) determines the LCD frame frequency. During initial system power on the System Oscillator will be in the stop state.

Segment Driver Outputs

The LCD drive section includes up to 43 segment outputs SEG0 ~ SEG42 which should be connected directly to the LCD panel. The segment output signals are generated in accordance with the multiplexed common signals and with the data resident in the display latch. The unused segment outputs should be left open-circuit.

Column Driver Outputs

The LCD drive section includes up to 8 column outputs COM0~COM7 which should be connected directly to the LCD panel. The column output signals are generated in accordance with the selected LCD drive mode. The unused column outputs should be left open-circuit if less than 8 column outputs are required.

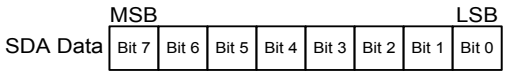
Address Pointer

The addressing mechanism for the display RAM is implemented using the address pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the address pointer by the Display Data Input command.

Display Memory – RAM Structure

The display RAM is static 39x8 bits RAM which stores the LCD data. Logic "1" in the RAM bit-map indicates the "on" state of the corresponding LCD segment; similarly, logic 0 indicates the 'off" state.

The contents of the RAM data are directly mapped to the LCD data. The first RAM column corresponds to the segments operated with respect to COM0. In multiplexed LCD applications the segment data from 2nd to 7th column of the display RAM are time-multiplexed with COM1 to COM7 respectively. The following diagram is a data transfer format for I^2C interface.



LCD Display Output Data Transfer Format for I^2C Bus

When the HT9B95A device is selected, the LCD RAM map is implemented as the following table shown.

Address	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7	Output
00H									SEG0
01H									SEG1
02H									SEG2
03H									SEG3
:	:	:	:	:	:	:	:	:	:
1FH									SEG31
20H									SEG32
21H									SEG33
22H									SEG34
RAM Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

RAM Mapping of 35x8 Display Mode

When the HT9B95B/HT9B95G device is selected with 1/8 duty, the LCD RAM map is implemented as the following table shown.

Address	COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7	Output
00H									SEG0
01H									SEG1
02H									SEG2
03H									SEG3
:	:	:	:	:	:	:	:	:	:
23H									SEG35
24H									SEG36
25H									SEG37
26H									SEG38
RAM Data	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

RAM Mapping of 39x8 Display Mode

When the HT9B95B/HT9B95G device is selected with 1/4 duty, the LCD RAM map is implemented as the following table shown.

Address	COM0	COM1	COM2	COM3	Output	COM0	COM1	COM2	COM3	Output
00H					SEG0					SEG1
01H					SEG2					SEG3
02H					SEG4					SEG5
03H					SEG6					SEG7
:	:	:	:	:	:	:	:	:	:	:
12H					SEG36					SEG37
13H					SEG38					SEG39
14H					SEG40					SEG41
15H					SEG42	—	—	—	—	—
RAM Data	Bit 7	Bit 6	Bit 5	Bit 4		Bit 3	Bit 2	Bit 1	Bit 0	

RAM Mapping of 43x4 Display Mode

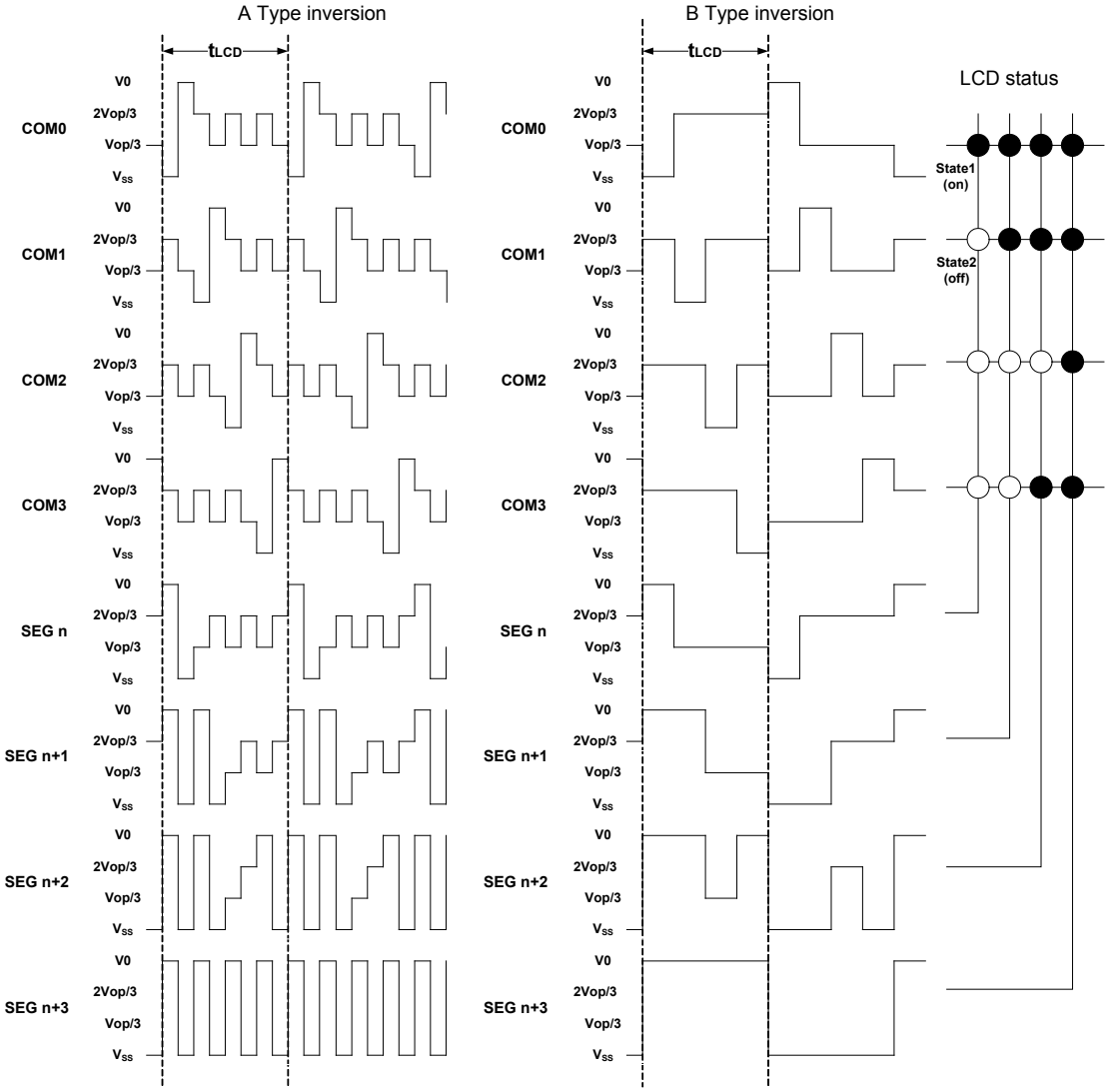
LCD Bias Generator

The max voltage level of the LCD driving voltage named as V0 can be adjusted through the LVA command setting. The full-scale LCD voltage, VOP, is obtained from (V0-VSS).

Fractional LCD biasing voltages, known as 1/3 or 1/4 bias voltage, are obtained from an internal voltage divider several of series resistors connected between V_{LCD} and V_{SS}. Certain resistors can be switched out of circuits to provide a 1/3 or 1/4 bias voltage level configuration.

LCD Drive Mode Waveforms

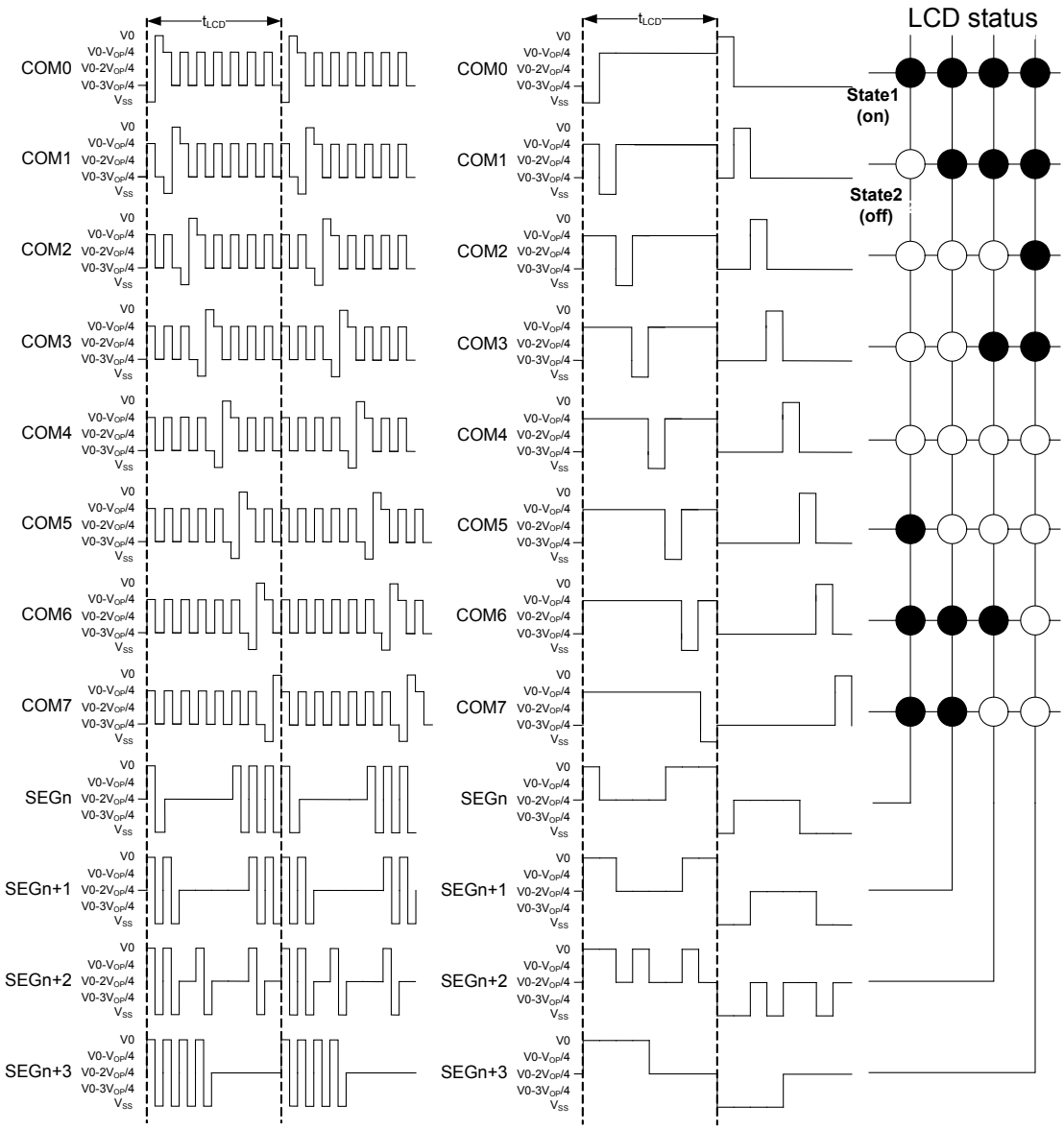
- When the LCD drive mode is selected as 1/4 duty and 1/3 bias, the waveform and LCD display is shown as follows:



Waveforms for 1/4 duty drive mode with 1/3 bias (V_{OP}=V0-V_{SS})

Note: $t_{LCD}=1/f_{LCD}$

- When the LCD drive mode is selected as 1/8 duty and 1/4 bias, the waveform and LCD display is shown as follows:



Waveforms for 1/8 duty drive mode with1/4 bias (V_{OP}= V0-V_{SS})

Note: $t_{LCD}=1/f_{LCD}$

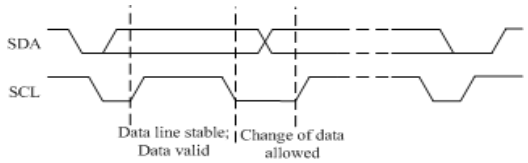
I²C Serial Interface

I²C Operation

The device supports I²C serial interface. The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to the positive supply via pull-up resistors with a typical value of 4.7kΩ. When the bus is free, both lines are high. Devices connected to the bus must have open-drain or open-collector outputs to implement a wired-or function. Data transfer is initiated only when the bus is not busy.

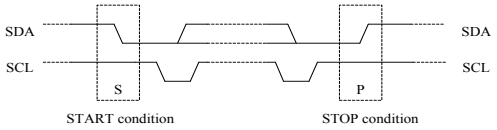
Data Validity

The data on the SDA line must be stable during the high period of the serial clock. The high or low state of the data line can only change when the clock signal on the SCL line is Low as shown in the diagram.



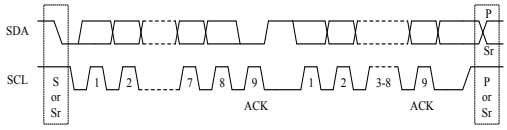
START and STOP Conditions

- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. In some respects, the START(S) and repeated START (Sr) conditions are functionally identical.



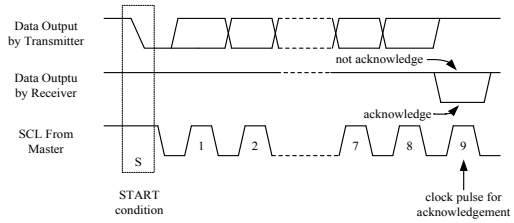
Byte Format

Every byte put on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit, MSB, first.



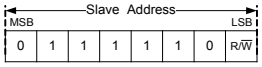
Acknowledge

- Each bytes of eight bits is followed by one acknowledge bit. This Acknowledge bit is a low level placed on the bus by the receiver. The master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an Acknowledge, ACK, after the reception of each byte.
- The device that acknowledges must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.
- A master receiver must signal an end of data to the slave by generating a not-acknowledge, NACK, bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse to not acknowledge. The master will generate a STOP or repeated START condition.



Slave Addressing

- The slave address byte is the first byte received following the START condition form the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines a read or write operation to be performed. When the R/$\overline{W}$ bit is "1", a read operation is selected. When the R/$\overline{W}$ bit is "0", a write operation is selected.
- The HT9B95 device address bits are "0111110". When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an Acknowledge on the SDA line.



I²C Interface Write Operation

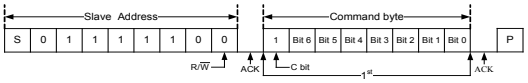
Write Operation

A Write operation requires a START condition, a slave address byte with a R/$\overline{W}$ bit, a command byte, a command byte or display RAM data byte and a STOP condition.

The MSB of the command byte is defined as "C" bit, the C bit is the command/data selection bit. When the C bit is set to "1", the next byte is a command byte. When the C bit is set to "0", the next byte is display RAM data. The data transfer format is shown in the accompanying diagram.

Once it enters display RAM data write mode, it can not be written any command. To write a command byte, it is necessary to generate a START condition again.

- **Single Command Type**
  A Single Command write operation requires a START condition, a slave address with a R/$\overline{W}$ bit, a command byte and a STOP condition for a single command write operation.

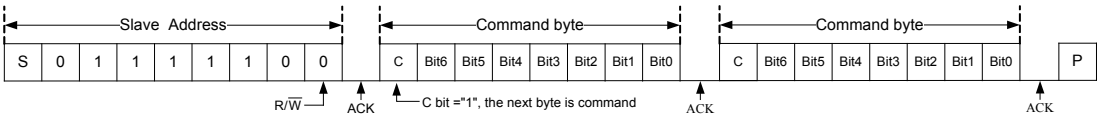


I²C Single Command Type Write Operation

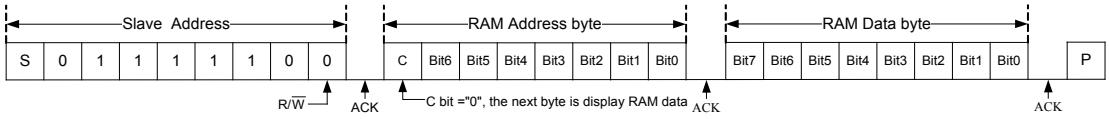
- **Compound Command Type**
  A Compound Command write operation requires a START condition, a slave address with a R/$\overline{W}$ bit followed by multiple command bytes and finally a STOP condition for a compound command write operation.

- **Display RAM Single Data Byte**
  A display RAM data byte write operation requires a START condition, a slave address with a R/$\overline{W}$ bit, a valid Register Address byte, a Data byte and a STOP condition.

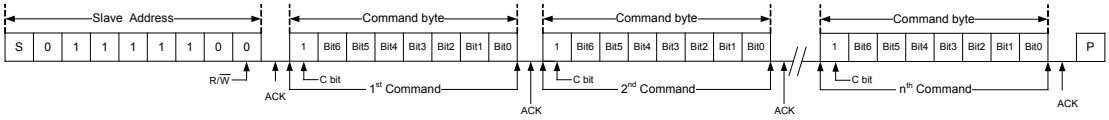
  The start address can only be set from 00H to the maximum available address, 22H, 15H or 26H, depending upon which device is used with different duty configurations. It is recommended that the start address should not be greater than the maximum available address.



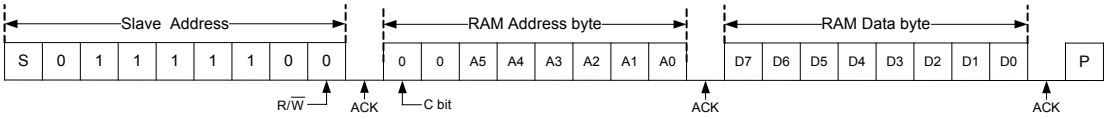
I²C Command Type Write Operation



I²C Display RAM Data Write Operation



I²C Compound Command Type Write Operation



I²C Display RAM Single Data Byte Write Operation

- **Display RAM Page Write Operation**

After a START condition the slave address with a R/$\overline{W}$ bit is placed on the bus followed with the specified display RAM Register Address of which the contents are written into the internal address pointer. The data to be written into the memory will be transmitted next. The internal address pointer will be incremented by 1 after a 8-bit data is shifted in. Then the acknowledge clock pulse will be received after an 8-bit data is shifted. After the internal address point reaches the maximum available address, 22H, 15H or 26H, the address pointer will be reset to 00H. It is strongly recommended to write the display RAM data from address 00H to maximum available address using the Display RAM Page Write Operation.

Part No.	Duty	Maximum Available Address
HT9B95A	1/8	22H
HT9B95B HT9B95G	1/4	15H
	1/8	26H

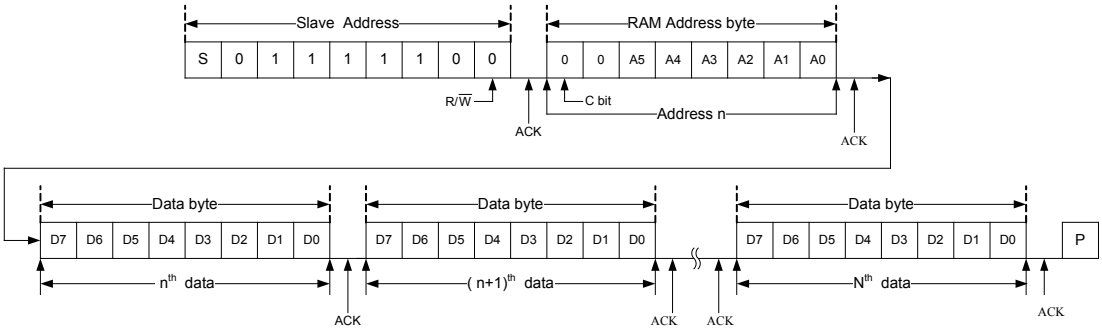
Display RAM Maximum Available Address

Read Operation

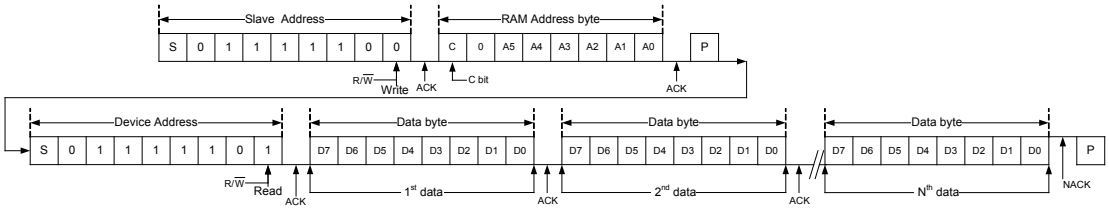
- **Display RAM Read Operation**

The master reads the display RAM data after setting the slave address. Following the R/$\overline{W}$ bit (="0") is an acknowledge bit and the register address byte which is written to the internal address pointer. After the start address of the read operation has been configured, another START condition and the slave address transferred on the bus followed by the R/$\overline{W}$ bit (="1"). Then the MSB of the data which was addressed is transmitted first on the I^2C bus. The address pointer is only incremented by 1 after the reception of an acknowledge clock. After reaching the maximum available address, the address pointer will be reset to 00H. The C bit in the register address byte can be set to "1" or "0".

This read operation will continue until the master sends a STOP condition. The maximum available address is summarized in the above section.



I^2C Interface N Bytes Display RAM Data Write Operation



Display RAM Read Operation

- **Command Register Read Operation**

The master reads the command register after setting the slave address. Following the R/$\overline{W}$ bit (="0") is an acknowledge bit and the register address byte which is written to the internal address pointer. After the start address of the read operation has been configured, another START condition and the slave address transferred on the bus followed by the R/$\overline{W}$ bit ("1"). Then the MSB of the data which was addressed is transmitted first on the I^2C bus. The C bit in the register address byte can be set to "1" or "0".

All command setting values are put together into two command registers with the register addresses of 23H and 24H or 27H and 28H when the Command Register Read Operation is executed. Each time the Command Register Read Operation is executed, only one command register can be read. To read all command registers, execute the Command Register Read Operation twice with the register address of 23H or 27H and 24H or 28H respectively. The two command registers contents are arranged in the following two registers and the detailed definition are described in the "Command Summary" section.

Part No.	Command Register 1 Address	Command Register 2 Address
HT9B95A	23h	24h
HT9B95B HT9B95G	27h	28h

Command Register Address

- **Command Register 1**

Bit	7	6	5	4	3	2	1	0
Name	—	DB	SR	LV4	LV3	LV2	LV1	LV0

Bit 6 **DB:** Duty and Bias setting

Bit 5 **SR:** Software Reset Operation

Bit 4~0 **LV4~LV0:** LCD Voltage Adjustment setting

- **Command Register 2**

Bit	7	6	5	4	3	2	1	0
Name	FR1	FR0	PS1	PS0	W	D	AP1	AP0

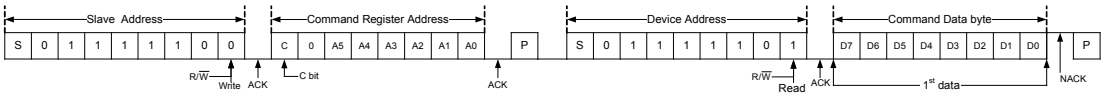
Bit 7~6 **FR1~FR0:** Frame Frequency setting

Bit 5~4 **PS1~PS0:** Power Save Mode setting

Bit 3 **W:** LCD Drive Waveform setting

Bit 2 **D:** Display On/Off setting

Bit 1~0 **AP1~AP0:** All pixels On/Off setting



Command Register Read Operation

Command Summary

The overall commands are summarized in this section. Note that the bit 7 denoted as "C" in the individual command here is the selection bit which is used to determine that the next byte is the display RAM data or command byte.

C bit	Description
0	Next byte is Display RAM data
1	Next byte is command

Command	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Function description
Display RAM Address setting	C	0	A5	A4	A3	A2	A1	A0	The display RAM address and command register setting.
LCD driving Voltage Adjustment (LVA)	C	1	0	LV4	LV3	LV2	LV1	LV0	Adjust the maximum voltage level of LCD driving voltage.
Display control	C	1	1	0	FR1	FR0	PS1	PS0	Frame frequency setting and power save mode setting
Drive mode setting and software reset	C	1	1	1	0	W	SR	D	LCD drive waveform select, display ON/OFF setting and software reset
All pixel control setting	C	1	1	1	1	0	AP1	AP0	All pixel control setting
Duty and Bias setting	C	1	1	1	1	1	0	DB	Duty and bias setting

Note: The "Duty and Bias setting" command is available in the HT9B95B and HT9B95G device.

Display RAM Address Setting Command

This command is used to define the accessed address of the display RAM or command register.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note
Address Pointer	C	0	A5	A4	A3	A2	A1	A0	Display RAM memory start address or Command register address.

Note:

- The display RAM address range is dependent upon the selected device with different duty setting.

Part No.	Duty	Maximum Available Address
HT9B95A	1/8	22H
HT9B95B HT9B95G	1/4	15H
	1/8	26H

- The command register address is dependent upon the selected device.

Part No.	Command Register 1 Address	Command Register 2 Address
HT9B95A	23H	24H
HT9B95B HT9B95G	27H	28H

- Power on status: the address will be set to 00H
- If the programmed command is not defined, the function will not be affected.

LCD Driving Voltage Adjustment Command – LVA

This command is used to adjust the maximum voltage level of the LCD driving voltage, V0.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note
LCD driving Voltage Adjustment (LVA)	C	1	0	LV4	LV3	LV2	LV1	LV0	—

Note: V0: The maximum voltage level of the LCD driving voltage.
The relationship between V0 and LVA setting is summarized as the following table shown.

LV4~LV0	Voltage ratio	V_{LCD} =5.5V	V_{LCD} =5V	V_{LCD} =3.5V	V_{LCD} =3V	V_{LCD} =2.5V
00000	V_{LCD}	V0=5.500V	V0=5.000V	V0=3.500V	V0=3.000V	V0=2.500V
00001	0.967 * V_{LCD}	V0=5.319V	V0=4.835V	V0=3.385V	V0=2.901V	V0=2.418V
00010	0.937 * V_{LCD}	V0=5.154V	V0=4.685V	V0=3.280V	V0=2.811V	V0=2.343V
00011	0.909 * V_{LCD}	V0=5.000V	V0=4.545V	V0=3.182V	V0=2.727V	V0=2.273V
00100	0.882 * V_{LCD}	V0=4.851V	V0=4.410V	V0=3.087V	V0=2.646V	V0=2.205V
00101	0.857 * V_{LCD}	V0=4.714V	V0=4.285V	V0=3.000V	V0=2.571V	V0=2.143V
00110	0.833 * V_{LCD}	V0=4.582V	V0=4.165V	V0=2.916V	V0=2.499V	V0=2.083V
00111	0.810 * V_{LCD}	V0=4.455V	V0=4.050V	V0=2.835V	V0=2.430V	V0=2.025V
01000	0.789 * V_{LCD}	V0=4.340V	V0=3.945V	V0=2.762V	V0=2.367V	V0=1.973V
01001	0.769 * V_{LCD}	V0=4.230V	V0=3.845V	V0=2.692V	V0=2.307V	V0=1.923V
01010	0.750 * V_{LCD}	V0=4.125V	V0=3.750V	V0=2.625V	V0=2.250V	V0=1.875V
01011	0.731 * V_{LCD}	V0=4.021V	V0=3.655V	V0=2.559V	V0=2.193V	V0=1.828V
01100	0.714 * V_{LCD}	V0=3.927V	V0=3.570V	V0=2.499V	V0=2.142V	V0=1.785V
01101	0.697 * V_{LCD}	V0=3.834V	V0=3.485V	V0=2.440V	V0=2.091V	V0=1.743V
01110	0.681 * V_{LCD}	V0=3.746V	V0=3.405V	V0=2.384V	V0=2.043V	V0=1.703V
01111	0.666 * V_{LCD}	V0=3.663V	V0=3.330V	V0=2.331V	V0=1.998V	V0=1.665V
10000	0.652 * V_{LCD}	V0=3.586V	V0=3.260V	V0=2.282V	V0=1.956V	V0=1.630V
10001	0.638 * V_{LCD}	V0=3.509V	V0=3.190V	V0=2.233V	V0=1.914V	V0=1.595V
10010	0.625 * V_{LCD}	V0=3.438V	V0=3.125V	V0=2.188V	V0=1.875V	V0=1.563V
10011	0.612 * V_{LCD}	V0=3.366V	V0=3.060V	V0=2.142V	V0=1.836V	V0=1.530V
10100	0.600 * V_{LCD}	V0=3.300V	V0=3.000V	V0=2.100V	V0=1.800V	V0=1.500V
10101	0.588 * V_{LCD}	V0=3.234V	V0=2.940V	V0=2.058V	V0=1.764V	V0=1.470V
10110	0.576 * V_{LCD}	V0=3.168V	V0=2.880V	V0=2.016V	V0=1.728V	V0=1.440V
10111	0.566 * V_{LCD}	V0=3.113V	V0=2.830V	V0=1.981V	V0=1.698V	V0=1.415V
11000	0.555 * V_{LCD}	V0=3.053V	V0=2.775V	V0=1.943V	V0=1.665V	V0=1.388V
11001	0.545 * V_{LCD}	V0=2.998V	V0=2.725V	V0=1.908V	V0=1.635V	V0=1.363V
11010	0.535 * V_{LCD}	V0=2.943V	V0=2.675V	V0=1.873V	V0=1.605V	V0=1.338V
11011	0.526 * V_{LCD}	V0=2.893V	V0=2.630V	V0=1.841V	V0=1.578V	V0=1.315V
11100	0.517 * V_{LCD}	V0=2.844V	V0=2.585V	V0=1.810V	V0=1.551V	V0=1.293V
11101	0.508 * V_{LCD}	V0=2.794V	V0=2.540V	V0=1.778V	V0=1.524V	V0=1.270V
11110	0.500 * V_{LCD}	V0=2.750V	V0=2.500V	V0=1.750V	V0=1.500V	V0=1.250V
11111	0.491 * V_{LCD}	V0=2.701V	V0=2.455V	V0=1.719V	V0=1.473V	V0=1.228V

Prohibit setting

- It is prohibited to set V0 voltage less than 2.5V and the condition “VLCD-V0>0.6V” must be met. If the voltage of (VLCD-V0) is equal to or less than 0.6V, the output voltage will be unstable.
- Power on status: V0=VLCD.
- If the programmed command is not defined, the function will not be affected.

Display Control Command

This command is used to select the current mode according to the characteristics of the LCD panel for achieving high display quality and frame frequency.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note
Display Control Setting	C	1	1	0	FR1	FR0	PS1	PS0	—

PS [1:0]	Power Save Mode	Current Consumption
00	Low Current2 Mode	x 0.5
01	Low Current1 Mode	x 0.67
10	Normal Current Mode	x 1 (default)
11	High Current Mode	x 1.8

FR [1:0]	Frame Frequency @V_{DD}=3.3V (Hz)
00	80 (default)
01	71
10	64
11	50

Note:

- The setting of the frame frequency, LCD output waveform and current mode will influence the display image qualities. Please select a proper display setting suitable for the current consumption and display image quality with LCD panel.

Mode	Flicker	Image Quality/Contrast
Frame Frequency	○	
LCD Driver Output Waveform	○	○
Power Save Mode		○

- Power on status: Normal current mode and Frame frequency is set to 80Hz.
- If the programmed command is not defined, the function will not be affected.

Drive Mode Setting and Software Reset Command

This command is used to control the LCD display On/Off, drive waveform and software reset.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note
Drive Mode setting and Software reset setting	C	1	1	1	0	W	SR	D	—

W	LCD drive output waveform
0	A type inversion
1	B type inversion (default)

SR	Software reset
0	No operation (default)
1	Software reset executed

D	Display On/Off
0	Display Off (default)
1	Display On

Note:

When the software reset is executed, the device is initialized by an internal power-on reset circuit. The status of the internal circuits after initialization is as follows:

- All common and segment outputs are set to V_{SS}.
- Display RAM address pointer is set to 00H.
- The maximum voltage level of the LCD driving voltage V0 is set to V_{LCD}.
- Frame Frequency is set to 80Hz.
- Power save mode is set to normal current.
- LCD Driver Output Waveform: B-type inversion.
- LCD Display is in the off state.
- LCD bias generator is off state.
- All pixel control is set to normal display.

If the programmed command is not defined, the function will not be affected.

All Pixels On/Off Setting Command

This command controls that all pixels are switched on or off when the LCD normally displays.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note
All Pixels Display setting	C	1	1	1	1	0	AP1	AP0	—

AP [1:0]	Display output status
00	Normal Display (default)
01	All Pixels Off
10	All Pixels On
11	All Pixels Off

Note:

- This command is only available when the LCD normally displays.
- The contents of the display RAM will not be affected in this duration.
- Power on status: Normal display.
- If the programmed command is not defined, the function will not be affected.

Duty and Bias Setting Command

This command controls the duty and bias setting and is available in the HT9B95B and HT9B95G device.

Function	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note
Duty and bias setting	C	1	1	1	1	1	0	DB	—

DB	Duty and Bias setting
0	1/8 duty, 1/4 bias (default)
1	1/4 duty, 1/3 bias

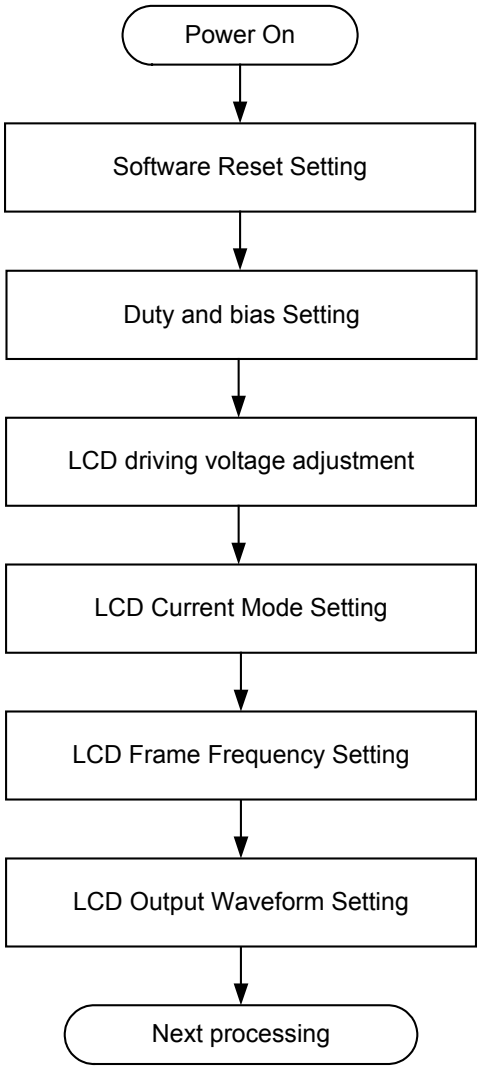
Note:

- This command is available in the HT9B95B and HT9B95G device.
- Power on status: 1/8 duty, 1/4 bias.
- If the programmed command is not defined, the function will not be affected.

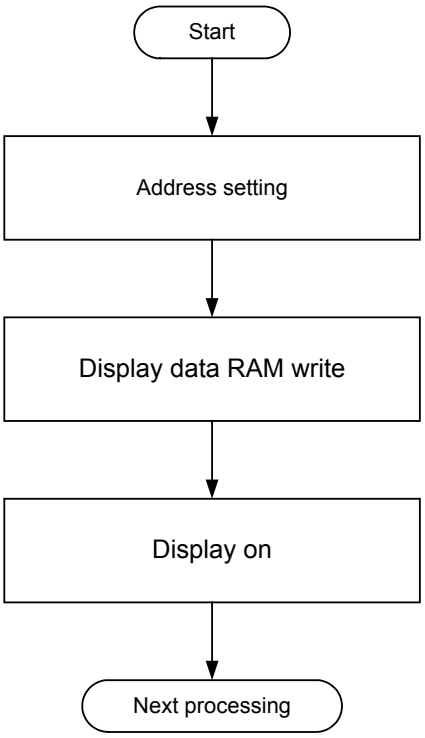
Operation Flow Chart

Access procedures are illustrated below using flowcharts.

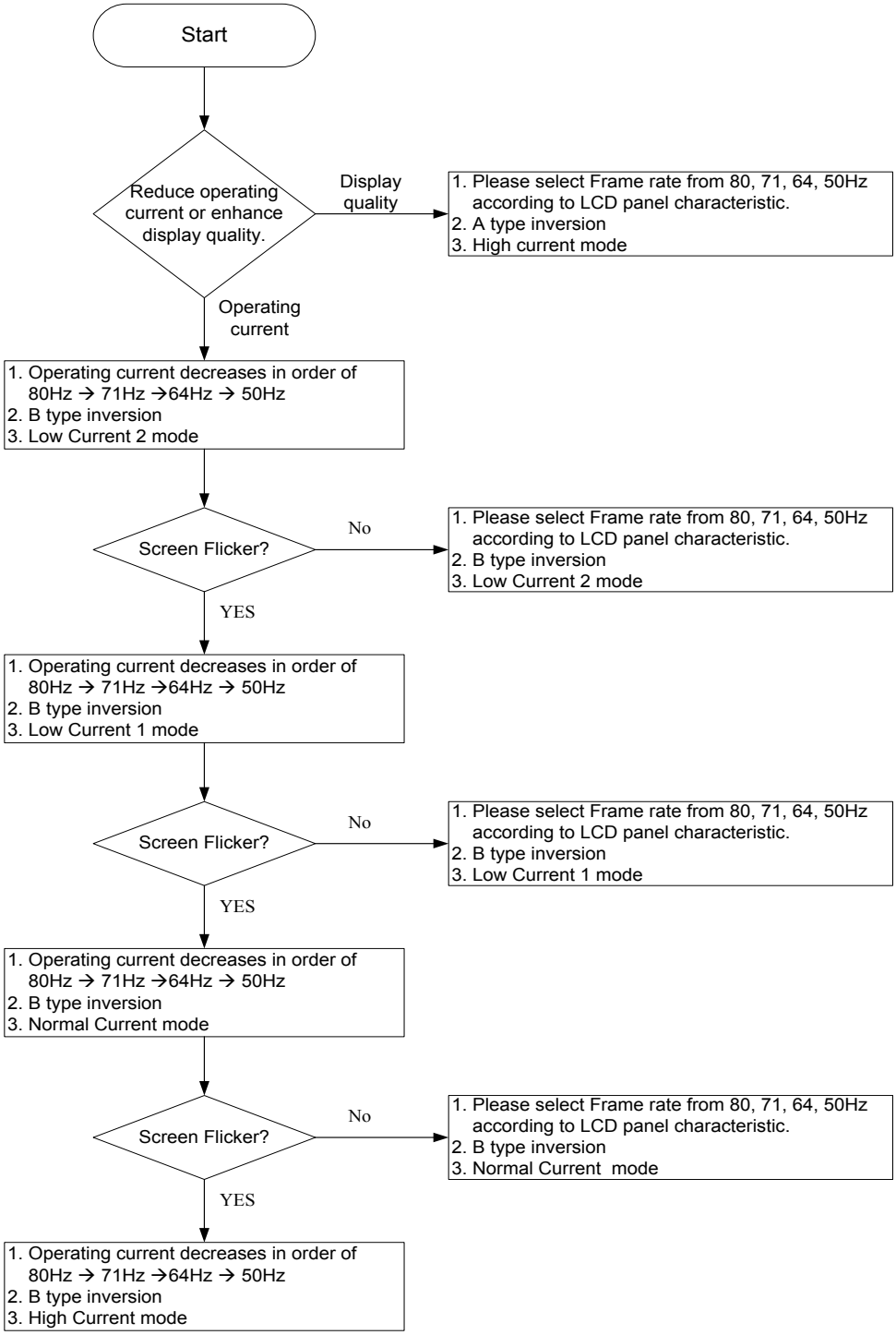
Initialization



Display Data Write (Address Setting)



Display Quality or Operating Current (Power Save Mode) Setting



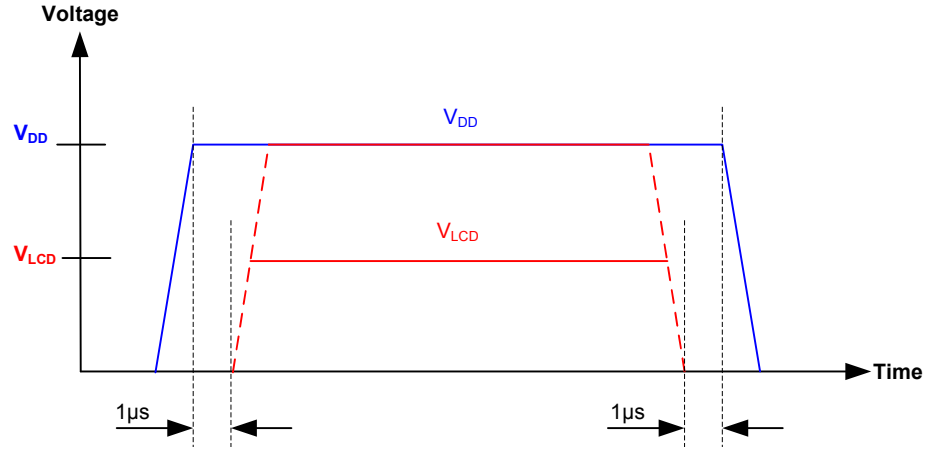
Power Supply Sequence

- If the power is individually supplied on the LCD and VDD pins, it is strongly recommended to follow the Holtek power supply sequence requirement.
- If the power supply sequence requirement is not followed, it may result in malfunction.

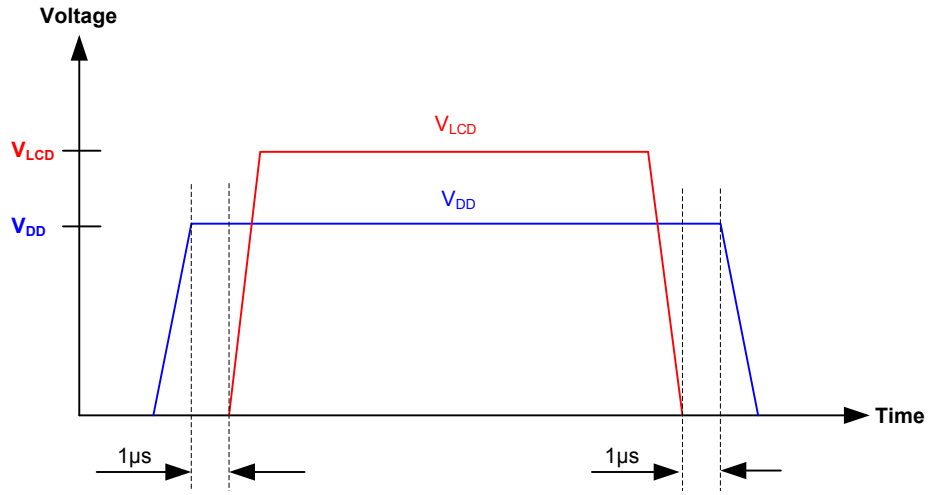
Holtek Power Supply Sequence Requirement:

1. Power-on sequence:
   Turn on the logic power supply V_{DD} first and then turn on the LCD driver power supply V_{LCD}.
2. Power-off sequence:
   Turn off the LCD driver power supply V_{LCD}. First and then turn off the logic power supply V_{DD}.
3. The Holtek Power Supply Sequence Requirement must be followed no matter whether the V_{LCD} voltage is higher than the V_{DD} voltage.

- When the V_{LCD} voltage is smaller than or is equal to V_{DD} voltage application

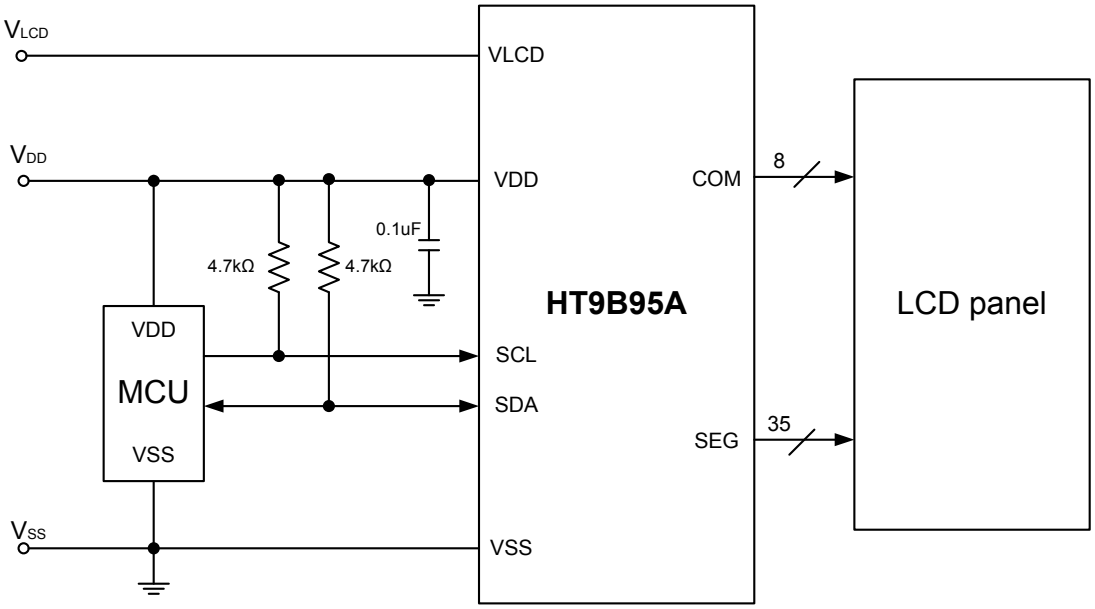


- When the V_{LCD} voltage is greater than V_{DD} voltage application

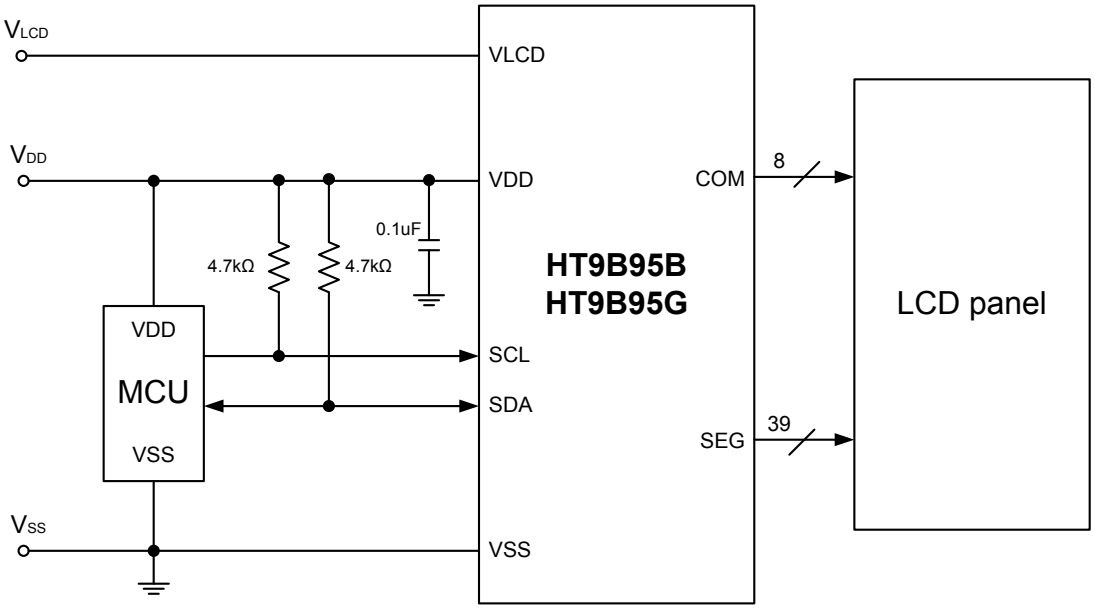


Application Circuit

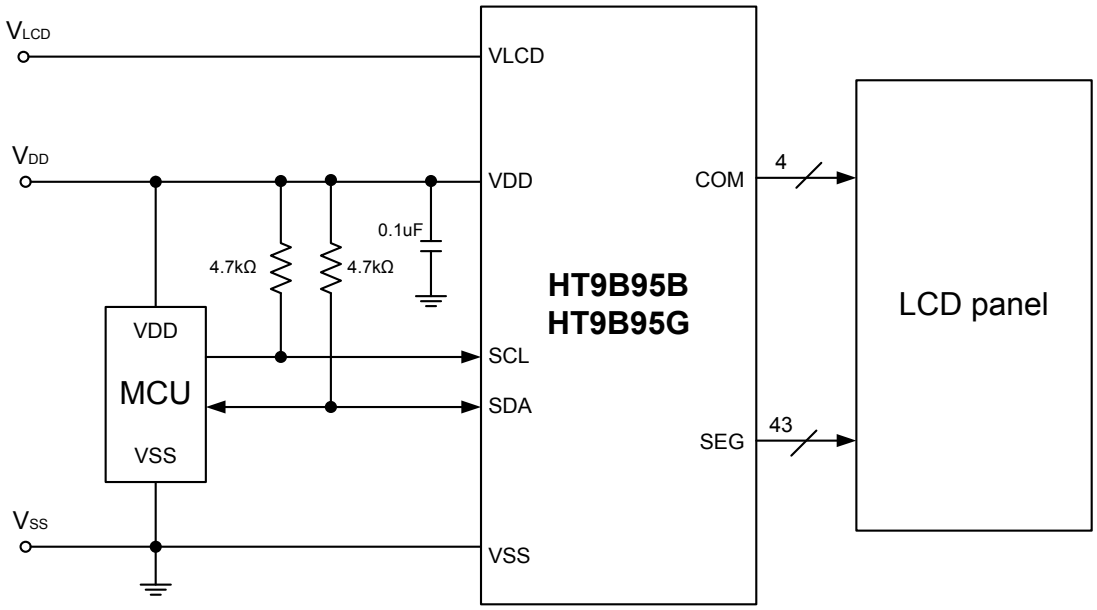
HT9B95A – 1/8 Duty and 1/4 Bias



HT9B95B/HT9B95G – 1/8 Duty and 1/4 Bias



HT9B95B/HT9B95G – 1/4 Duty and 1/3 Bias



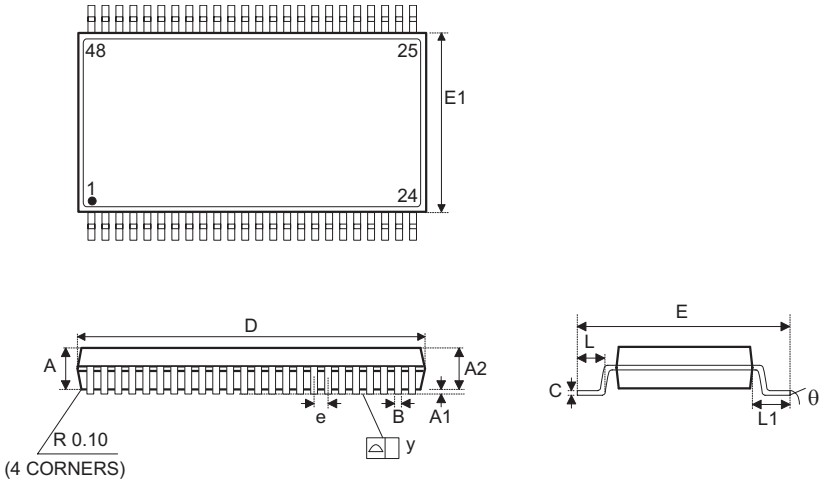
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the package information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

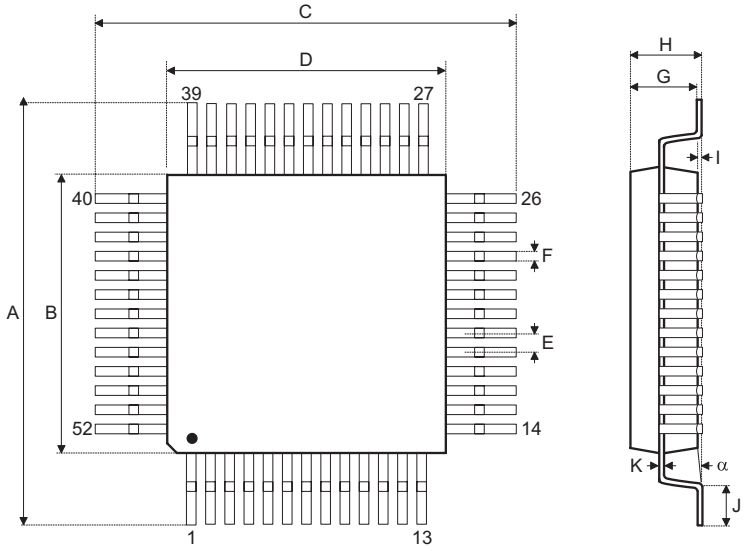
48-pin TSSOP Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	—	0.047
A1	0.002	—	0.006
A2	0.031	0.039	0.041
b	0.007	—	0.011
c	0.004	—	0.008
D	0.488	0.492	0.496
E	—	0.319 BSC	—
E1	0.236	0.240	0.244
e	—	0.020 BSC	—
L	0.018	0.024	0.030
L1	—	0.039 BSC	—
y	—	0.004	—
θ	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1	1.05
b	0.17	—	0.27
c	0.09	—	0.20
D	12.40	12.50	12.60
E	—	8.10 BSC	—
E1	6.00	6.10	6.20
e	—	0.50 BSC	—
L	0.45	0.60	0.75
L1	—	1.0 BSC	—
y	—	0.10	—
θ	0°	—	8°

52-pin LQFP (14mm×14mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.622	0.630	0.638
B	0.547	0.551	0.555
C	0.622	0.630	0.638
D	0.547	0.551	0.555
E	—	0.039 BSC	—
F	0.015	—	0.019
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.008
J	0.018	—	0.030
K	0.005	—	0.007
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	15.80	16.00	16.20
B	13.90	14.00	14.10
C	15.80	16.00	16.20
D	13.90	14.00	14.10
E	—	1.00 BSC	—
F	0.39	—	0.48
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.20
J	0.45	—	0.75
K	0.13	—	0.18
α	0°	—	7°

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