

Dual P-Channel 30-V (D-S) Common Drain MOSFET

■ Features

- Low $r_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SO-8 Surface Mount Package Saves Board Space
- High power and current handling capability
- Extended V_{GS} range (± 25) for battery pack applications

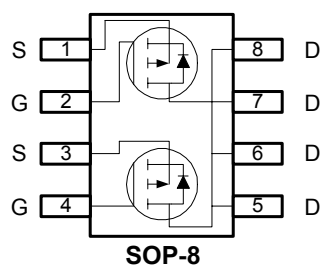
■ General Description

These miniature surface mount MOSFETs utilize High Cell Density process. Low $r_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWM DC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

■ Product Summary

V_{DS} (V)	$r_{DS(on)}$ (m Ω)	I_D (A)
-30	21@ $V_{GS}=-10V$	-9.5
	35@ $V_{GS}=-4.5V$	-7.0

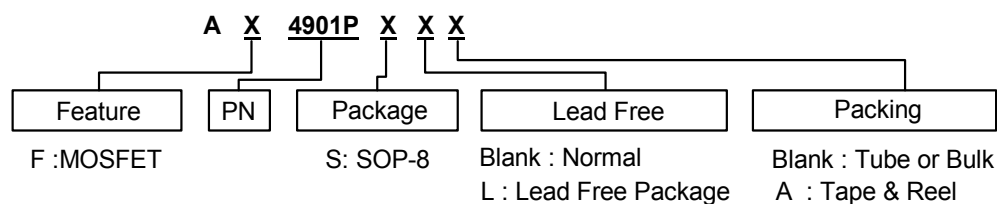
■ Pin Assignments



■ Pin Descriptions

Pin Name	Description
S	Source
G	Gate
D	Drain

■ Ordering information



**AF4901P****Dual P-Channel 30-V (D-S) Common Drain MOSFET****■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)**

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 25	V
I_D	Continuous Drain Current (Note 1)	$T_A=25^\circ\text{C}$	A
		$T_A=70^\circ\text{C}$	
I_{DM}	Pulsed Drain Current (Note 2)	± 30	A
I_S	Continuous Source Current (Diode Conduction) (Note 1)	-2.1	A
P_D	Power Dissipation (Note 1)	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

■ Thermal Resistance Ratings

Symbol	Parameter	Maximum	Units
$R_{\theta JC}$	Maximum Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$
$R_{\theta JA}$	Maximum Junction-to-Ambient (Note 1)	78	$^\circ\text{C/W}$

Note 1: surface Mounted on 1"x 1" FR4 Board.

Note 2: Pulse width limited by maximum junction temperature

■ Specifications ($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Static						
$V_{(BR)DSS}$	Drain-Source breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
$V_{GS(th)}$	Gate-Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-1.6	-3	V
I_{GSS}	Gate-Body Leakage	$V_{DS}=0V, V_{GS}=\pm 25V$	-	-	± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-24V, V_{GS}=0V$ $V_{DS}=-24V, V_{GS}=0V, T_J=55^{\circ}C$	-	-	-1 -5	μA
$I_{D(on)}$	On-State Drain Current (Note 3)	$V_{DS}=-5V, V_{GS}=-10V$	-30	-	-	A
$r_{DS(on)}$	Drain-Source On-Resistance (Note 3)	$V_{GS}=-10V, I_D=-9.5A$	-	19	21	m Ω
		$V_{GS}=-4.5V, I_D=-7.0A$	-	28	35	
		$V_{GS}=-10V, I_D=-7A, T_J=125^{\circ}C$	-	26	34	
g_{fs}	Forward Tranconductance (Note 3)	$V_{DS}=-5V, I_D=-13A$	-	19	-	S
V_{SD}	Diode Forward Voltage	$I_S=2.1A, V_{GS}=0V$	-	-0.7	-1.2	V
Dynamic (Note 4)						
Q_g	Total Gate Charge	$V_{DS}=-15V, V_{GS}=-5V, I_D=-7A$	-	15	22	nC
Q_{gs}	Gate-Source Charge		-	4.7	-	
Q_{gd}	Gate-Drain Charge		-	4.8	-	
Switching						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15, R_L=6\Omega, I_D=-1A, V_{GEN}=-10V$	-	14	23	nS
t_r	Rise Time		-	11	20	
$t_{d(off)}$	Turn-Off Delay Time		-	48	76	
t_f	Fall-Time		-	25	39	

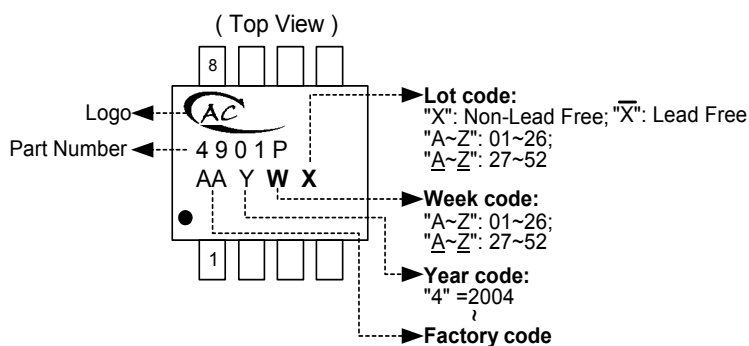
Note 3: Pulse test: $PW \leq 300\mu s$ duty cycle $\leq 2\%$.

Note 4: Guaranteed by design, not subject to production testing.

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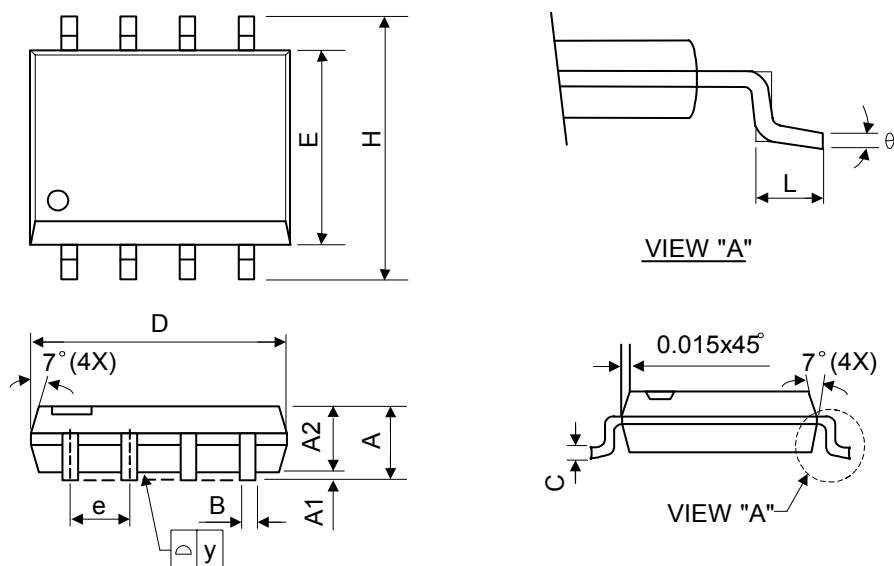
■ Marking Information

SOP-8L



■ Package Information

Package Type: SOP-8L



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10	-	0.25	0.040	-	0.100
A2	1.30	1.45	1.50	0.051	0.057	0.059
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	5.05	5.30	0.189	0.199	0.209
E	3.70	3.90	4.10	0.146	0.154	0.161
e	-	1.27	-	-	0.050	-
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
y	-	-	0.10	-	-	0.004
θ	0°	-	8°	0°	-	8°