

Si890x MASTER CONTROLLER RECOMMENDATIONS

1. Introduction

The Si890x isolated 10-bit monitoring ADCs integrate a 10-bit SAR ADC subsystem, supervisory state machine and isolated UART (Si8900), I²C/SMbus port (Si8901), or SPI Port (Si8902) into a single 16 SOW package. Based on Silicon Labs' proprietary CMOS isolation technology, the Si890x series offers isolation ratings of 2.5 or 5.0 kV and finds use across a wide range of low-frequency analog data acquisition applications including isolated ac line monitors, sensor interface circuits, power-delivery systems, and solar inverters. Si890x devices operate in slave mode and must be managed by an external master controller (typically an MCU). This application note provides useful recommendations for configuring the user's master controller for operation with the Si890x including serial port resynchronization and recovery from loss of VDD.

2. Si890x Overview

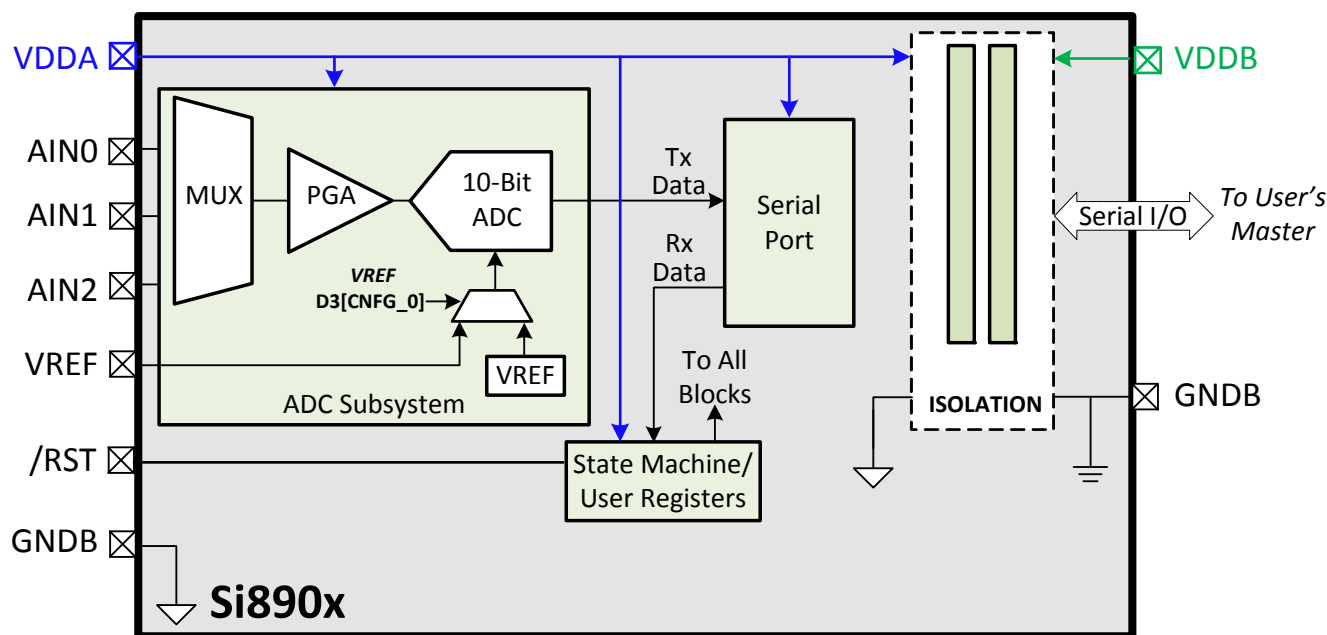


Figure 1. Si890x Generic Block Diagram

Figure 1 shows a generic block diagram representative of any member of the Si890x family. The Si890x family requires input and output VDD supplies that are isolated from each other. The input-side supply (VDDA) provides bias to the ADC subsystem, state machine, serial port, and the input side of the digital isolator. The VDDB supply powers the isolator output circuits and typically powers the user's master as well. The user's master controller sends a serial command byte to the Si890x that specifies the ADC operating mode, MUX channel address, and voltage reference source. Upon receipt of the command byte, the Si890x executes the specified ADC conversion(s) and makes conversion data available for the master to read at the isolated serial port interface. An understanding of the integrated CMOS digital isolator operation is necessary to understanding the overall Si890x operation. For detailed information on Si890x operation, see the Si890x data sheet available for download at www.silabs.com/isolation.

2.1. Integrated Galvanic Isolation

The CMOS isolation technology offers uniform, stable performance over operating voltage and temperature with none of the fundamental weaknesses of optocouplers. A block diagram of a CMOS digital isolator channel is shown in Figure 2.

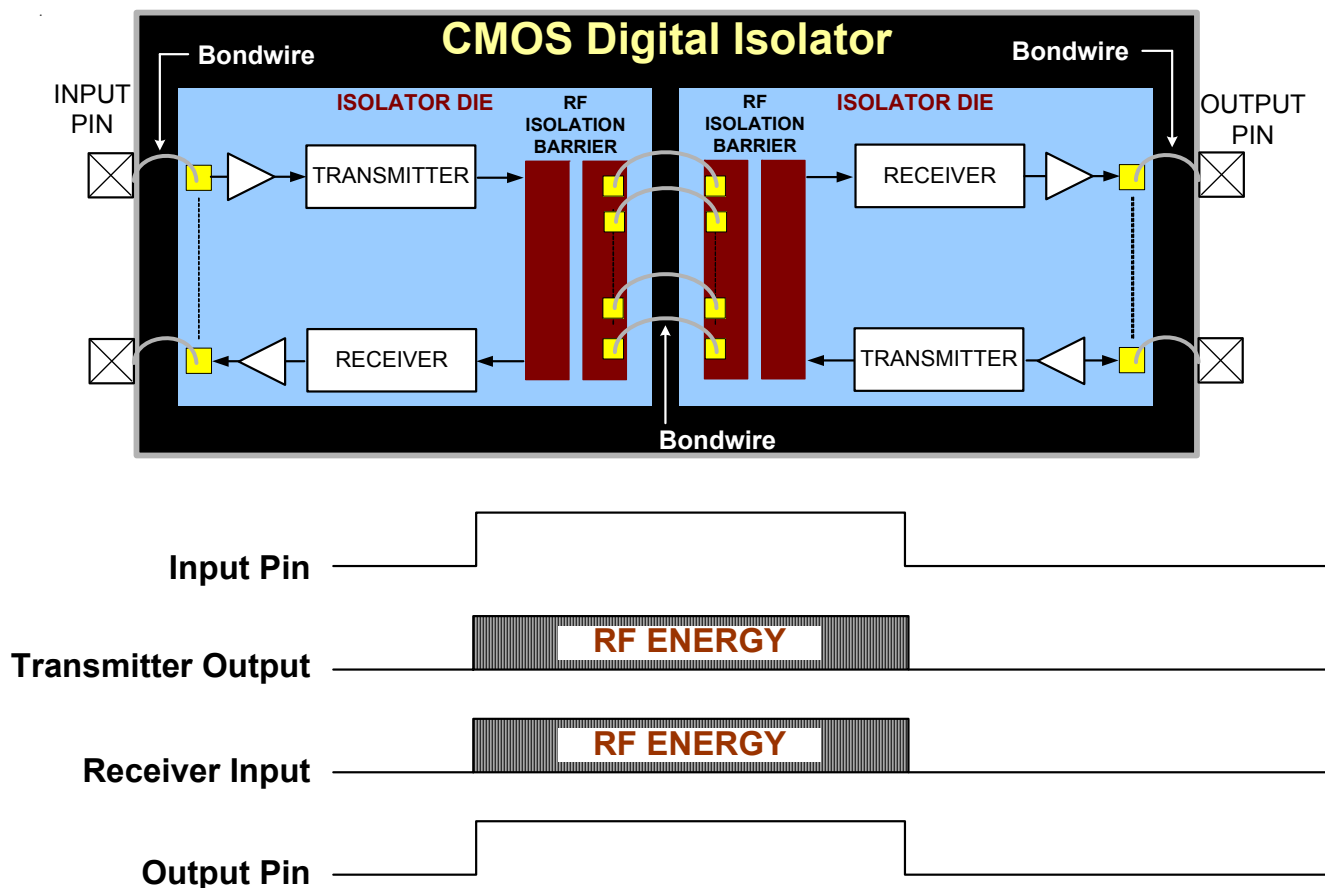


Figure 2. CMOS Isolator Block Diagram

The operation of the digital isolator is analogous to that of an optocoupler, except a high-frequency carrier is used instead of light. An isolator channel consists of two identical semiconductor dies in a standard IC package where each die contains both transmit and receive circuits. When they are wire-bonded together, the two dies form a high-frequency transmitter and receiver separated by a differential capacitive isolation barrier. Input/output data is transferred using simple on/off keying (OOK) modulation; when an input pin (VIN) is high, the transmitter generates a carrier that propagates across the isolation barrier to the receiver. The receiver asserts logic 1 on the output pin (VOUT) when sufficient in-band carrier energy is detected. When VIN is low, the transmitter is off, and the receiver drives VOUT low because no in-band RF energy is detected. Refer to Table 1 to determine outputs when one or both VDD supplies are not present. For more information, see the Si8660/1/2/3 data sheet for the CMOS digital isolator.

Table 1. CMOS Digital Isolator Operation

V_I Input ^{1,2}	VDDI State ^{1,3,4}	VDDO State ^{1,3,4}	V_O Output ^{1,2}	Comments
H	P	P	H	Normal operation.
L	P	P	L	
X	UP	P	L H	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 μ s.
X	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I within 1 μ s.
Notes: <ol style="list-style-type: none"> 1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals. 2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance. 3. "Powered" state (P) is defined as 2.5 V < VDD < 5.5 V. 4. "Unpowered" state (UP) is defined as VDD = 0 V. 				

3. Si8900 Auto Baud Master Controller Algorithm

Figure 3 shows the master/Si8900 adaptive automatic baud rate detection (“auto baud”). The Si8900 baud rate detection algorithm uses the master’s UART baud rate to determine the upper and lower baud rate boundaries and centers the operating baud rate between these two limits. Adaptive baud rate detection begins with the Si8900 setting its baud rate to its maximum value of 520 kbps and waiting for the master to send a stream of bytes (each having a hex value of 0xAA) to the Si8900. The Si8900 compares each received byte to 0xAA and decreases the baud rate when the received byte is other than 0xAA. This process continues until 0xAA is successfully received by the Si8900, at which time the upper baud rate limit value is stored in Si8900 memory.

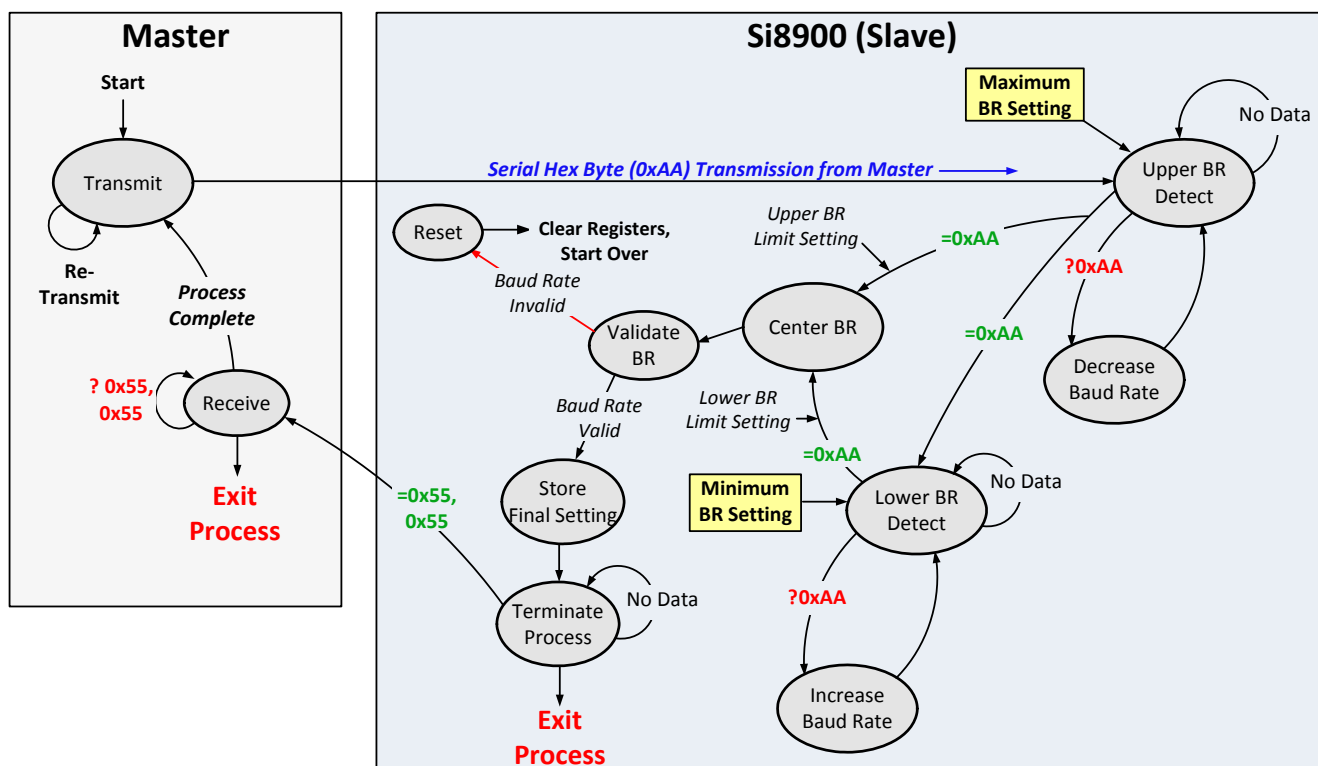


Figure 3. Si8900 Auto Baud Process Functional Flow Diagram

The Si8900 then discovers its lower baud rate limit by setting the baud rate to its minimum value of 58 kbps and again comparing each incoming byte to 0xAA, increasing the baud rate until 0xAA is successfully received and stored in Si8900 memory. The Si8900 then optimizes the baud rate by centering the operating baud rate half-way between the upper and lower baud rate limits. The Si8900 then terminates the adaptive baud rate sequence by transmitting two sequential 0x55 bytes to the master. Master controller C-code firmware examples for Figure 3 are available in the application note, “AN635: Si8900 Automatic Baud Rate Detection” available for download at www.silabs.com/isolation.

3.1. Si8900 Communication Recovery after VDD Failure

A VDD power failure after the adaptive baud rate process has been completed will halt communication between the Si8900 and the master. Referring to Table 2, loss of VDDB deprives the isolator output driver of bias voltage, causing the Tx and Rx pins to enter an “undetermined” state. That is, Tx and Rx may fall to zero or be pulled to arbitrary voltage by local parasitic coupling. (Tx and Rx can be made to be deterministic by attaching resistors from Tx and Rx to either ground or VDD.) Because VDDA is uninterrupted, the Si8900 memory still contains the previously calculated, valid baud rate setting. Consequently, the master need only resume communication with the Si8900 after VDDB is restored. Note that the auto baud algorithm should not be invoked because the 0xAA byte will be rejected by the Si8900 as an invalid command byte as input-side power was not interrupted. Loss of VDDA disables the ADC subsystem, state machine, and memory, serial port and input-side isolator bias voltage. In this case, the previously calculated baud rate setting is lost; so, the master must invoke the auto baud synchronization cycle after VDDA recovers.

Table 2. Si8900 Power Fail Behavior

VDDA Supply	VDDB Supply	ADC Status	State Machine/Memory	Si8900 Rx	Si8900 Tx	Invoke Auto Baud?
Powered	Powered	Enabled	Enabled	Enabled	Enabled	Yes
Powered	Unpowered	Enabled	Enabled	Undetermined	Undetermined	No
Unpowered	Powered	Disabled	Disabled	Low	High	Yes
Unpowered	Unpowered	Disabled	Disabled	Undetermined	Undetermined	N/A

Note that all Si890x devices return every command byte they receive to the master for verification. For more information, see “AN635: Si8900 Automatic Baud Rate Detection”, which contains master controller code examples for verifying returned Si8900 commands against the master's original transmission. If the master receives a returned command that differs from its original transmission, the Si8900 baud rate value is likely incorrect. This can be confirmed by having the master send the same command byte to the Si8900 three to five consecutive times and invoke auto baud for re-synchronization if the results are consistently incorrect. Note that if the Si8900 loses power, the master's command transmissions will not be returned to the Si8900, thus providing the master a way to distinguish between an incorrect baud rate and an unpowered Si8900 slave.

3.2. Si8901 and Si8902 Master Controller Recommendations

Unlike the Si8900 UART (asynchronous) communication port, the Si8901 I²C port is a synchronous port that is clocked by the master controller. This port uses an ACK/NAK (acknowledge/not acknowledge) scheme to indicate a successful or unsuccessful data transfer between the Si8901 and the master, respectively. Upon receipt of a NAK, the master should re-transmit the CNFG_0 command byte to the Si8901 to re-establish communication and should receive a copy of this byte back from the Si8901. Should the Si8901 repeatedly fail to return a copy of the master's Si8901 CNFG_0 command byte, the master can either continue trying to establish communication or service other unrelated tasks and return later to attempt communication. Loss of Si8901 input or output-side VDD results in the I²C bus lines being pulled high by the bus pull-up resistors (see Table 3). For more information about the operation of the Si8901 I²C port, see the Si890x data sheet available at www.silabs.com/isolation.

Table 3. Si8901 Power Fail Behavior

VDDA Supply	VDDDB Supply	ADC Status	State Machine/ Memory	Si8901 SDA	Si8901 SCL
Powered	Powered	Enabled	Enabled	Enabled	Enabled
Powered	Unpowered	Enabled	Enabled	Pulled High	Pulled High
Unpowered	Powered	Disabled	Disabled	Pulled High	Pulled High
Unpowered	Unpowered	Disabled	Disabled	Pulled High	Pulled High

The Si8902 SPI port is also a synchronous serial port. To ensure that the SPI port is reset, the master must toggle its /EN output each time a data byte is transmitted or received. As shown in Table 4, loss of output-side VDDDB or simultaneous power loss of VDDA and VDDDB will force all SPI port lines into a high-impedance state. Note that loss of VDDA alone causes all but the slave data output line (SDO) to retreat to a high-impedance state (SDO reverts to a logic-low state). Note that loss of VDDDB disables the isolator output driver, causing several SPI port pins to enter an undetermined state where a given pin may fall to zero or be pulled to arbitrary voltages by local parasitic coupling. These pins can be made to be deterministic by attaching resistors from the undetermined pins to either ground or VDD. Like the Si8901, repeated failures to return the CNFG_0 command byte to the master indicates that the Si8902 is either unpowered or otherwise off-line. In this case, the master can either continue trying to establish communication or service other unrelated tasks and return later to attempt communication.

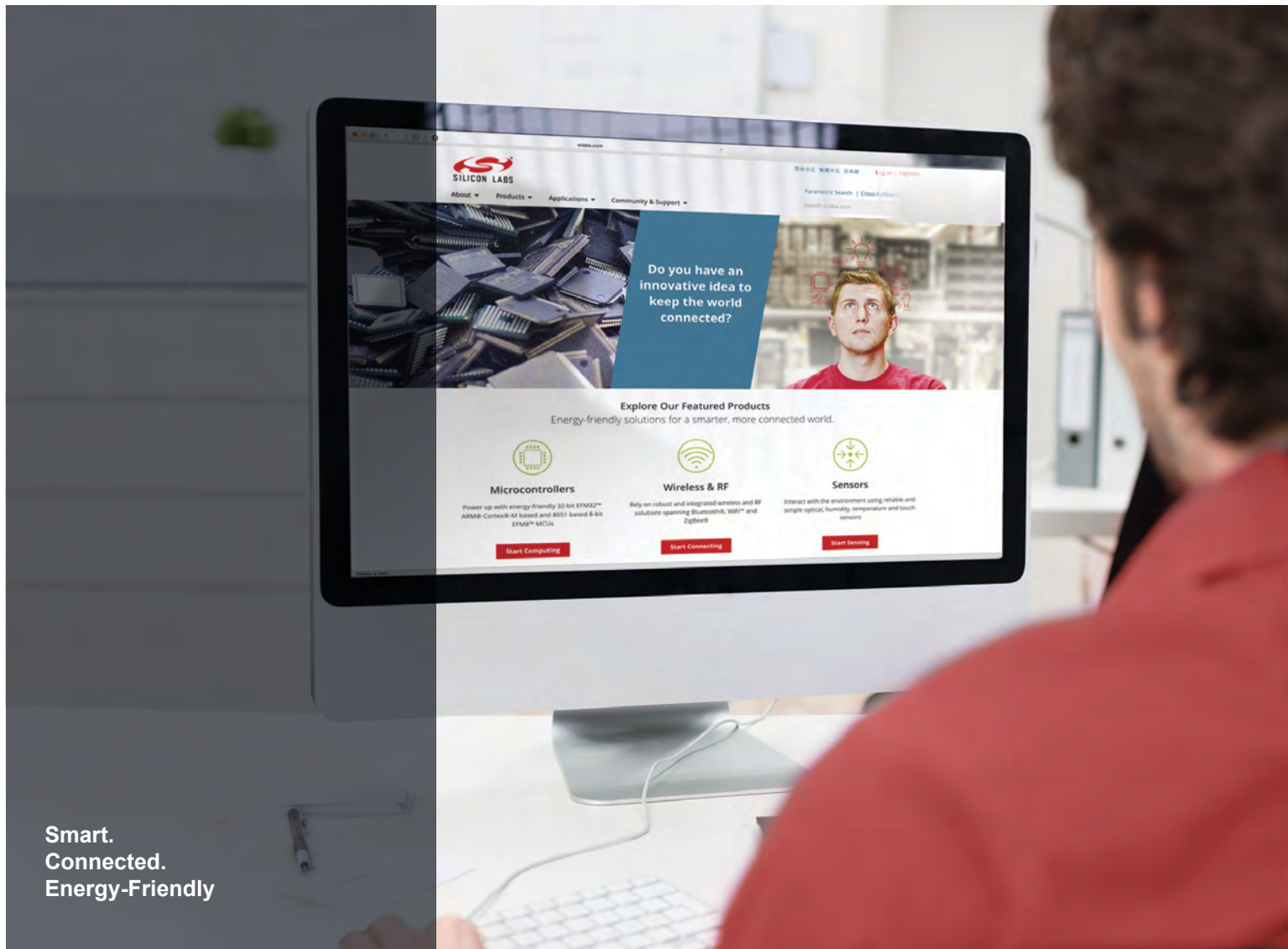
Table 4. Si8902 Power Fail Behavior

VDDA Supply	VDDDB Supply	ADC Status	State Machine/ Memory	Si8902 SDI	Si8902 SDO	Si8902 SCLK	Si8902 /EN
Powered	Powered	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled
Powered	Unpowered	Enabled	Enabled	Undetermined	Undetermined	Undetermined	Undetermined
Unpowered	Powered	Disabled	Disabled	Undetermined	Low	Undetermined	Undetermined
Unpowered	Unpowered	Disabled	Disabled	Undetermined	Undetermined	Undetermined	Undetermined

4. Related Documents

- Si890x Data Sheet
- AN635: Si8900 Auto Baud Rate Detection

NOTES:

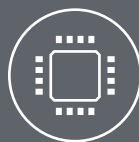


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