

FDMC3300NZA**Monolithic Common Drain N-Channel 2.5V Specified PowerTrench® MOSFET****8A, 20V, 26mΩ****General Description**

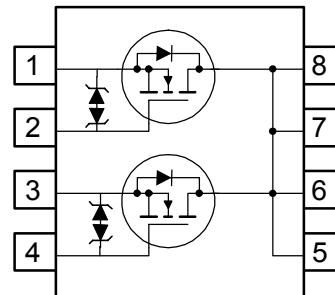
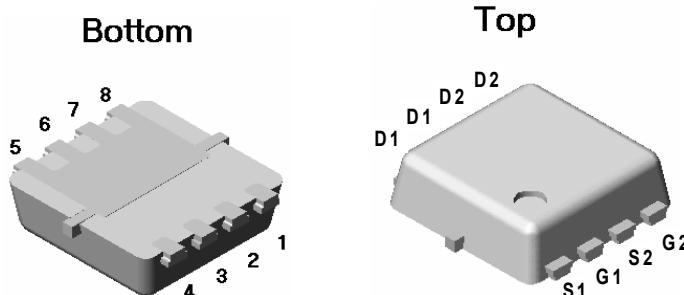
This Dual N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced Power Trench process to optimize the $R_{DS(on)}$ @ $V_{GS}=2.5V$ on special MicroFET leadframe with all the drains on one side of the package.

Applications

- Li-Ion Battery Pack

**Features**

- $R_{DS(ON)} = 26m\Omega$ @ $V_{GS} = 4.5 V$, $I_D = 8A$
- $R_{DS(ON)} = 34m\Omega$ @ $V_{GS} = 2.5 V$, $I_D = 7A$
- >2000V ESD protection
- Low Profile-1mm maximum-in the new package MicroFET 3.3x3.3 mm
- Pb-free and RoHS Compliant

**Absolute Maximum Ratings** $T_A = 25^\circ C$ unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|----------------|--|-------------|-------|
| V_{DSS} | Drain-Source Voltage | 20 | V |
| V_{GSS} | Gate-Source Voltage | ± 12 | V |
| I_D | Drain Current -Continuous -Pulsed | 8 | A |
| | | 40 | |
| P_D | Power dissipation (Steady State) | 2.4 | W |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | -55 to +150 | °C |

Thermal Characteristics

| | | | | |
|-----------------|---|-----------|-----|------|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 52 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1b) | 108 | |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 5 | |

Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape Width | Quantity |
|----------------|-------------|-----------|------------|------------|
| 3300A | FDMC3300NZA | 7" | 12mm | 3000 units |

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
|--------|-----------|-----------------|-----|-----|-----|-------|

Off Characteristics

| | | | | | | |
|-----------------------------------|---|---|----|------|----------|----------------------------|
| B_{VDSS} | Drain-Source Breakdown Voltage | $V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$ | 20 | - | - | V |
| ΔB_{VDSS} ΔT_J | Breakdown Voltage Temperature Coefficient | $I_D = 250\mu\text{A}$, Referenced to 25°C | - | 12.0 | - | $\text{mV}/^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 16\text{V}$, $V_{GS} = 0\text{V}$, | - | - | 1 | μA |
| I_{GSS} | Gate-Body Leakage, | $V_{GS} = \pm 12\text{V}$, $V_{DS} = 0\text{V}$ | - | - | ± 10 | μA |

On Characteristics (Note 2)

| | | | | | | |
|--|--|--|-----|------|-----|----------------------------|
| $V_{GS(\text{th})}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$ | 0.6 | - | 1.5 | V |
| $\Delta V_{GS(\text{th})}$ ΔT_J | Gate Threshold Voltage Temperature Coefficient | $I_D = 250\mu\text{A}$, Referenced to 25°C | - | -3.1 | - | $\text{mV}/^\circ\text{C}$ |
| $R_{DS(\text{ON})}$ | Static Drain-Source On-Resistance | $V_{GS} = 4.5\text{V}$, $I_D = 8\text{A}$ | - | 20 | 26 | $\text{m}\Omega$ |
| | | $V_{GS} = 2.5\text{V}$, $I_D = 7\text{A}$ | - | 25 | 34 | |
| | | $V_{GS} = 4.5\text{V}$, $I_D = 8\text{A}$, $T_J = 150^\circ\text{C}$ | - | 29 | 38 | |
| g_{FS} | Forward Transconductance | $V_{DS} = 5\text{V}$, $I_D = 8\text{A}$ | - | 29 | - | S |

Dynamic Characteristics

| | | | | | | |
|-----------|------------------------------|--|---|-----|---|----------|
| C_{iss} | Input Capacitance | $V_{DS} = 10\text{V}$, $V_{GS} = 0\text{V}$, $f = 1.0\text{MHz}$ | - | 610 | - | pF |
| C_{oss} | Output Capacitance | | - | 165 | - | pF |
| C_{rss} | Reverse Transfer Capacitance | | - | 115 | - | pF |
| R_G | Gate Resistance | $f = 1.0\text{MHz}$ | - | 1.7 | - | Ω |

Switching Characteristics (Note 2)

| | | | | | | |
|--------------|---------------------|---|---|----|----|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = 10\text{V}$, $I_D = 1\text{A}$ $V_{GS} = 4.5\text{V}$, $R_{GEN} = 6\Omega$ | - | 8 | 16 | ns |
| t_r | Turn-On Rise Time | | - | 8 | 16 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | - | 19 | 34 | ns |
| t_f | Turn-Off Fall Time | | - | 9 | 18 | ns |
| Q_g | Total Gate Charge | $V_{DS} = 10\text{V}$, $I_D = 8\text{A}$, $V_{GS} = 4.5\text{V}$ | - | 8 | - | nC |
| Q_{gs} | Gate-Source Charge | | - | 1 | - | nC |
| Q_{gd} | Gate-Drain Charge | | - | 2 | - | nC |

Drain-Source Diode Characteristics and Maximum Ratings

| | | | | | | |
|----------|------------------------------------|---|---|-----|-----|----|
| V_{SD} | Drain-Source Diode Forward Voltage | $V_{GS} = 0\text{V}$, $I_S = 2\text{A}$ (Note 2) | - | 0.7 | 1.2 | V |
| t_{rr} | Diode Reverse Recovery Time | $I_F = 8\text{A}$, | - | - | 21 | ns |
| Q_{rr} | Diode Reverse Recovery Charge | $dI_F/dt = 100\text{A}/\mu\text{s}$ | - | - | 6 | nC |

Notes:

- R_{0JA} is determined with the device mounted on a 1in² oz.copper pad on a 1.5x1.5 in board of FR-4 material . R_{0JC} are guaranteed by design while R_{0JA} is determined by the user's board design.



a. 52°C/W when mounted on a 1 in² pad of 2 oz



b. 108°C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

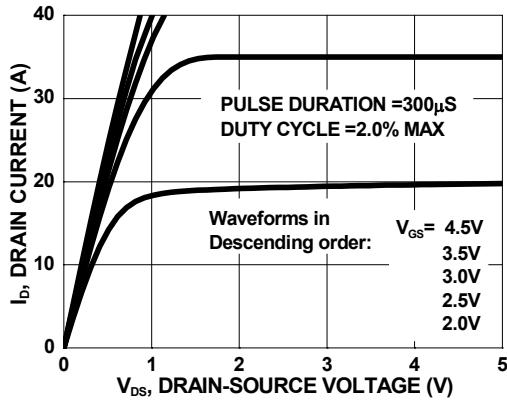


Figure 1. On Region Characteristics

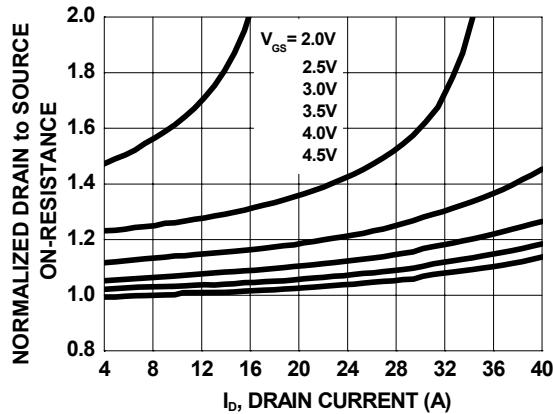


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

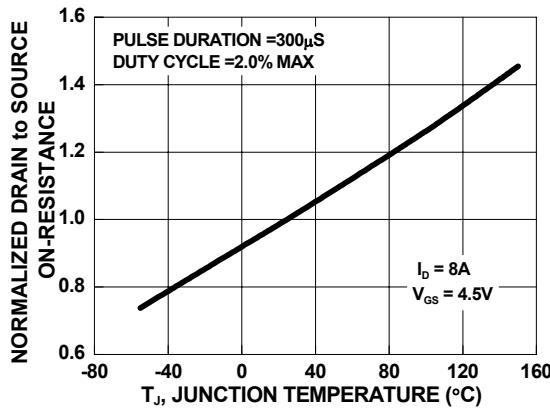


Figure 3. On Resistance Variation with Temperature

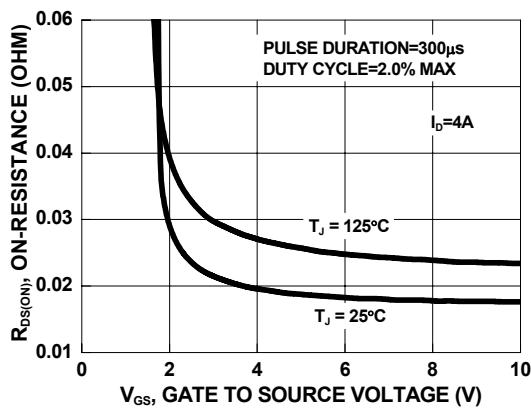


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

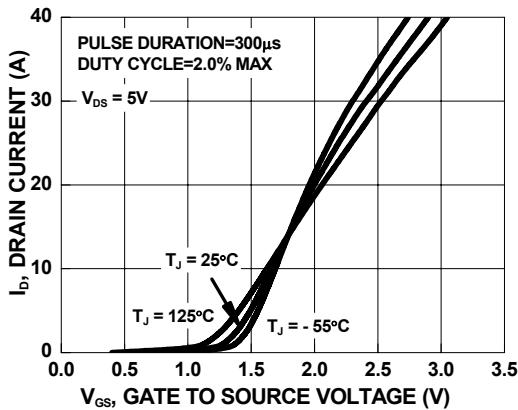


Figure 5. Transfer Characteristics

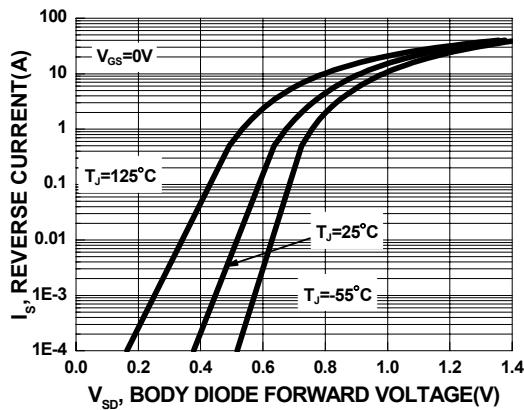


Figure 6. Body Diode Forward Voltage Variation With Source Current and Temperature

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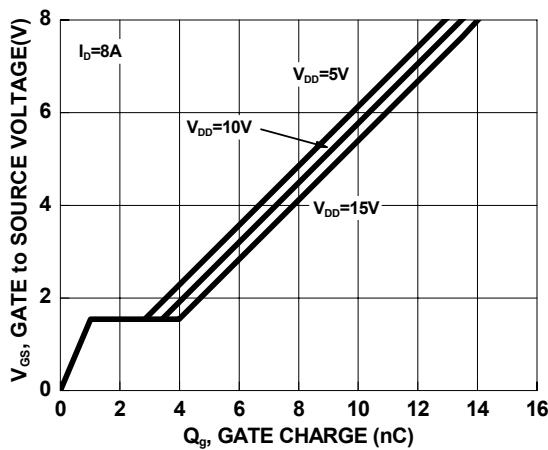


Figure 7. Gate Charge Characteristics

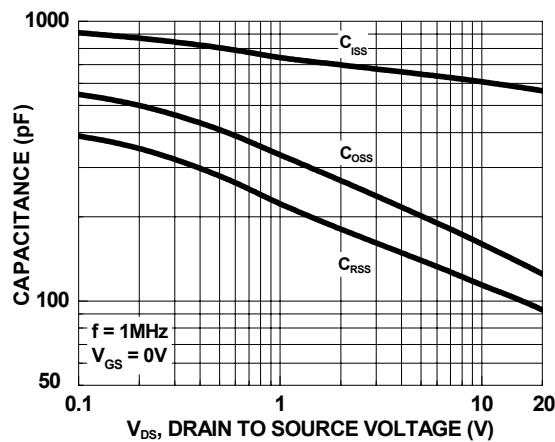


Figure 8. Capacitance Characteristics

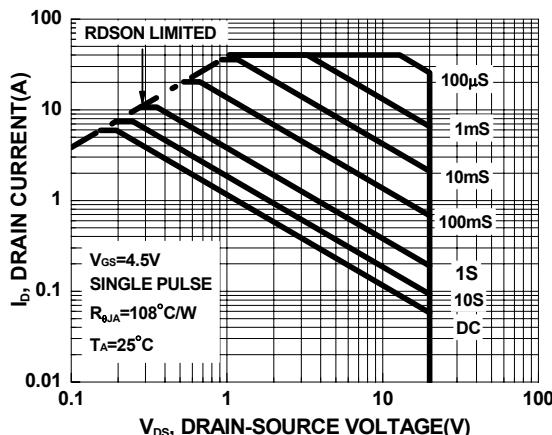


Figure 9. Safe Operating Area

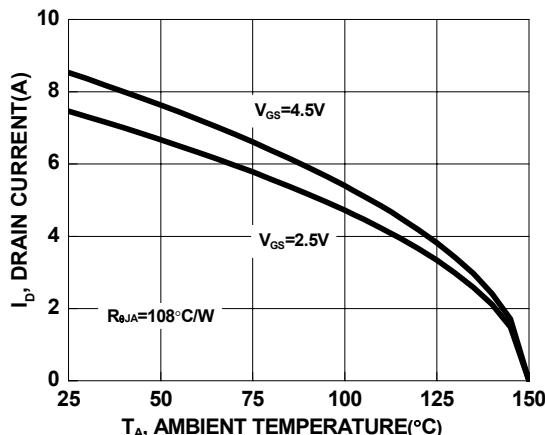


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

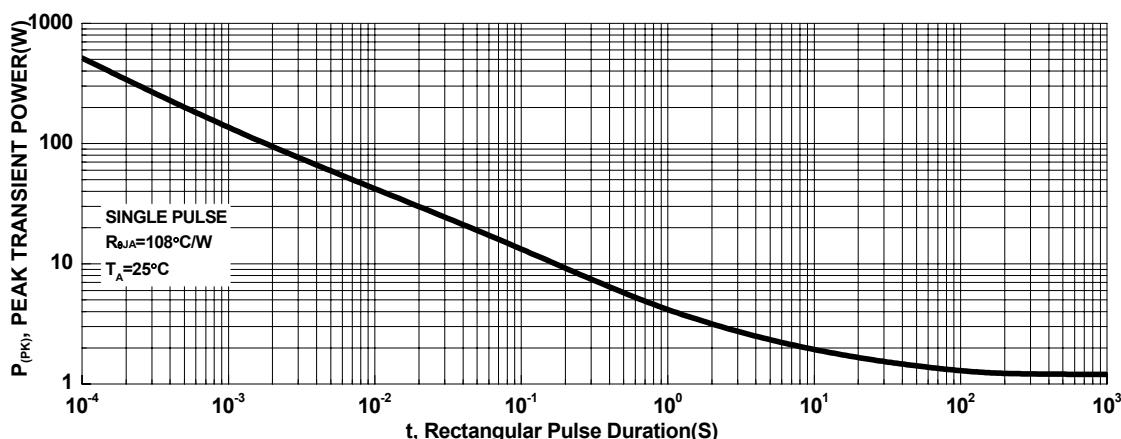


Figure 11. Single Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

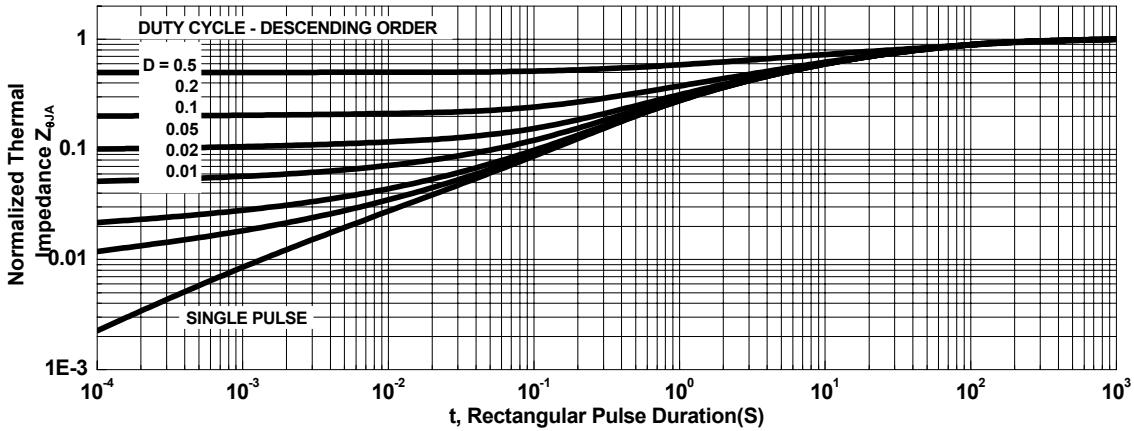
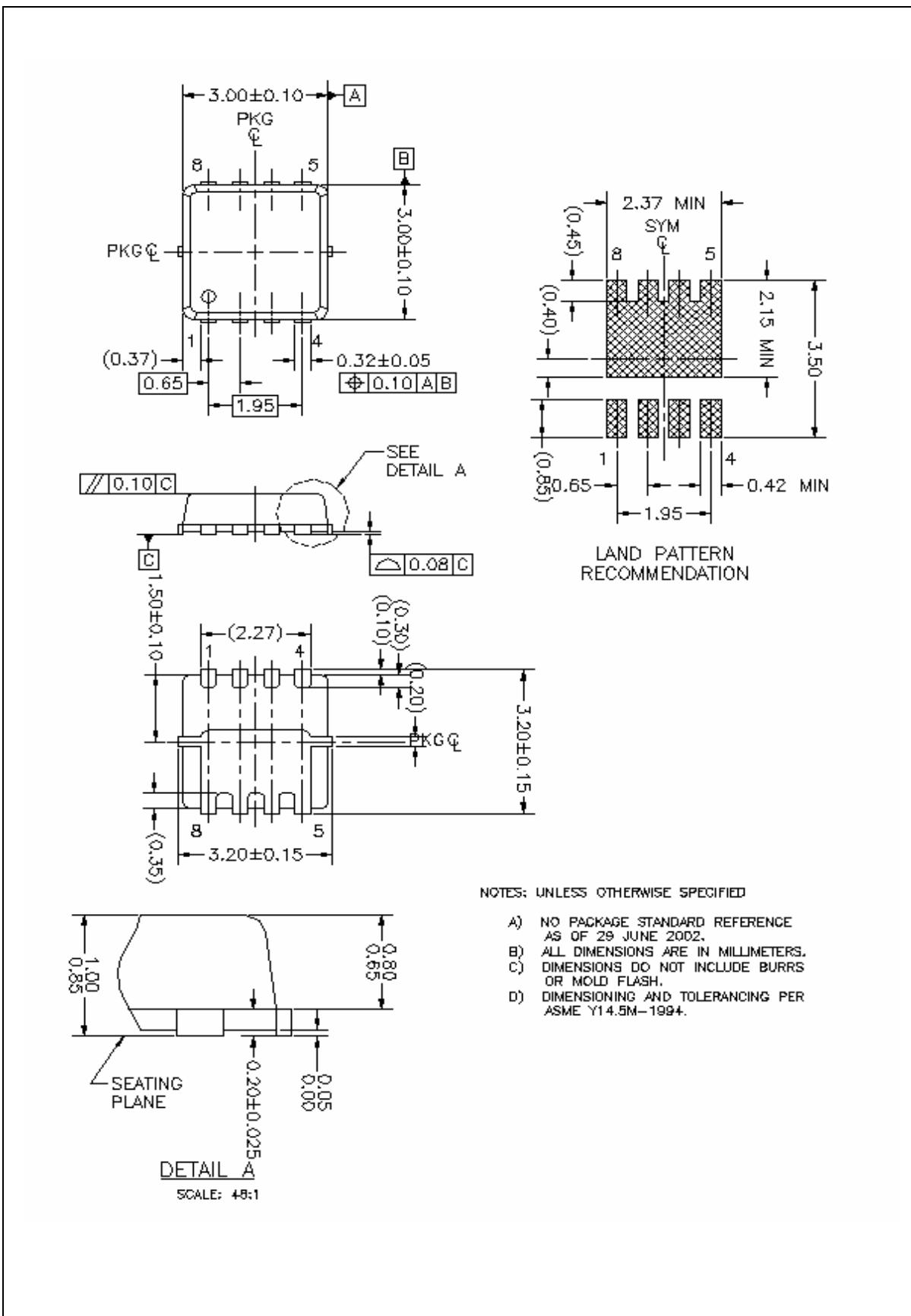


Figure 12. Transient Thermal Response Curve

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