SGM4582
High Voltage, CMOS Analog Multiplexer

GENERAL DESCRIPTION

The SGM4582 is a high voltage, CMOS analog IC configured as two 4-channel multiplexers. This CMOS device can operate from ±1.8V to ±5.5V dual power supplies or from +3.6V to +11V single supplies. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 10nA at +25℃.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single +5V or dual ±5V supplies.

SGM4582 is available in Green SOIC-16, SSOP-16, TSSOP-16 and TQFN-3×3-16L packages. It operates over an ambient temperature range of -40℃ to +85℃.

APPLICATIONS

Battery-Operated Equipment
Audio and Video Signal Routing
Low-Voltage Data-Acquisition Systems
Communications Circuits
Automotive

FEATURES

- **Guaranteed On-Resistance**
  51Ω with ±5V Supplies
  84Ω with Single +5V Supply
- **Guaranteed On-Resistance Match Between Channels**
- **Low Off-Leakage Current 10nA at +25℃**
- **Low On-Leakage Current 10nA at +25℃**
- **±1.8V to ±5.5V Dual-Supply Operation**
  +3.6V to +11V Single-Supply Operation
- **TTL/CMOS-Logic Compatible**
- **Low Distortion: 0.08% (R_L = 600Ω, f = 20Hz to 20kHz)**
- **High Off-Isolation: -66dB (R_L = 50Ω, f = 1MHz)**
- **Low Crosstalk: -100dB (R_L = 50Ω, f = 1MHz)**
- **Extended Industrial Temperature Range:**
  -40℃ to +85℃
- **Available in Green SOIC-16, SSOP-16, TSSOP-16 and TQFN-3×3-16L Packages**

PACKAGE/ORDERING INFORMATION

MODEL	PIN-PACKAGE	ORDERING NUMBER	PACKAGE MARKING	PACKAGE OPTION
SGM4582	SOIC-16	SGM4582YS16G/TR	SGM4582YS16 XXXXX	Tape and Reel, 2500
	SSOP-16	SGM4582YQS16G/TR	SGM4582 YQS16 XXXXX	Tape and Reel, 3000
	TSSOP-16	SGM4582YTS16G/TR	SGM4582 YTS16 XXXXX	Tape and Reel, 3000
	TQFN-3×3-16L	SGM4582YTQ16G/TR	4582TQ XXXXX	Tape and Reel, 3000

NOTE: **XXXXX** = Date Code and Vendor Code.

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V_{EE}
V_{CC}.....-0.3V to 13.2V
GND……..……. -0.3V to 6V
Voltage into Any Terminal (1)
……(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Continuous Current into Any Terminal.....±20mA
Peak Current, X_, Y_
(pulsed at 1ms, 10% duty cycle) .....±40mA
Operating Temperature Range.....-40℃ to +85℃
Junction Temperature.....150℃
Storage Temperature Range.....-65℃ to +150℃
Lead Temperature (soldering, 10s).....260℃
ESD Susceptibility
HBM.....3000V
MM..... 200V

NOTES:
1. Voltages exceeding V_{CC} or V_{EE} on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

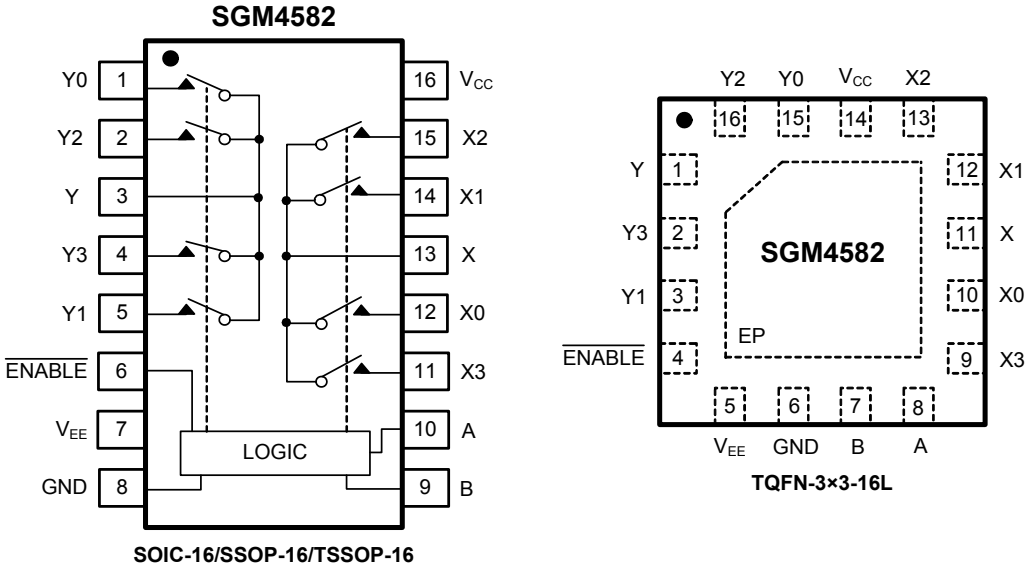
2. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SGMICRO reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SGMICRO sales office to get the latest datasheet.

PIN CONFIGURATIONS (TOP VIEW)



FUNCTION TABLE

$\overline{\text{ENABLE}}$ INPUT	SELECT INPUTS		ON SWITCHES
	B	A	
H	*X*	*X*	All Switches Open
L	L	L	X-X0, Y-Y0
L	L	H	X-X1, Y-Y1
L	H	L	X-X2, Y-Y2
L	H	H	X-X3, Y-Y3

X = Don't care

NOTE:
Input and output pins are identical and interchangeable. Either may be considered an input or output; signals pass equally well in either direction.

PIN DESCRIPTION

SOIC-16, SSOP-16, TSSOP-16	TQFN-3×3-16L	NAME	FUNCTION
13	11	X	Analog Switch “X” Output.
12, 14, 15, 11	10, 12, 13, 9	X0, X1, X2, X3	Analog Switch “X” Inputs 0-3.
1, 5, 2, 4	15, 3, 16, 2	Y0, Y1, Y2, Y3	Analog Switch “Y” Inputs 0-3.
3	1	Y	Analog Switch “Y” Output.
16	14	V_{CC}	Positive Analog and Digital Supply Voltage Input.
10	8	A	Digital Address “A” Input.
9	7	B	Digital Address “B” Input.
8	6	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V_{CC} and V_{EE}.)
7	5	V_{EE}	Negative Analog Supply Voltage Input. Connect to GND for single-supply operation.
6	4	$\overline{ENABLE}$	Digital Enable Input. Normally connected to GND.
—	Exposed Pad	EP	Exposed Pad. Connect EP to V_{EE}.

NOTE:
Input and output pins are identical and interchangeable. Any may be considered an input or output; signals pass equally well in both directions.

ELECTRICAL CHARACTERISTICS (Dual Supplies)

(V_{CC} = 4.5V to 5.5V, V_{EE} = -4.5V to -5.5V, Full = -40℃ to +85℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{X_}$, $V_{Y_}$, V_X, V_Y		Full	V_{EE}		V_{CC}	V
On-Resistance	R_{ON}	V_{CC} = 4.5V, V_{EE} = -4.5V, I_X, I_Y = 1mA	+25℃		36	51	Ω
			Full			62	
On-Resistance Match Between Channels	ΔR_{ON}	V_{CC} = 4.5V, V_{EE} = -4.5V, I_X, I_Y = 1mA	+25℃		3	11	Ω
			Full			12.7	
On-Resistance Flatness	$R_{FLAT(ON)}$	V_{CC} = 4.5V, V_{EE} = -4.5V, I_X, I_Y = 1mA	+25℃		15	25	Ω
			Full			29	
X_, Y_ Off Leakage Current	$I_{X_(OFF)}$, $I_{Y_(OFF)}$	V_{CC} = 5.5V, V_{EE} = -5.5V, $V_{X_}$, $V_{Y_}$ = ±4.5V, V_X, V_Y = ∓4.5V	+25℃		10		nA
X, Y Off Leakage Current	$I_{X(OFF)}$, $I_{Y(OFF)}$	V_{CC} = 5.5V, V_{EE} = -5.5V, $V_{X_}$, $V_{Y_}$ = ±4.5V, V_X, V_Y = ∓4.5V	+25℃		10		nA
X, Y On Leakage Current	$I_{X(ON)}$, $I_{Y(ON)}$	V_{CC} = 5.5V, V_{EE} = -5.5V, V_X, V_Y = ±4.5V	+25℃		10		nA
DIGITAL I/O							
Logic Input Logic Threshold High	V_{AH}, V_{BH}, $V_{\overline{ENABLEH}}$		+25℃	2.4			V
Logic Input Logic Threshold Low	V_{AL}, V_{BL}, $V_{\overline{ENABLEL}}$		+25℃			0.8	V
Input-Current High	I_{AH}, I_{BH}, $I_{\overline{ENABLEH}}$	V_A, V_B, $V_{\overline{ENABLE}}$ = V_{CC}	+25℃		10		nA
Input-Current Low	I_{AL}, I_{BL}, $I_{\overline{ENABLEL}}$	V_A, V_B, $V_{\overline{ENABLE}}$ = 0V	+25℃		10		nA
DYNAMIC CHARACTERISTICS							
Address Transition Time	t_{TRANS}	$V_{X_}$, $V_{Y_}$ = ±3V, R_L = 300Ω, C_L = 35pF, Test Circuit 1	+25℃		70		ns
$\overline{ENABLE}$ Turn-On Time	t_{ON}	$V_{X_}$, $V_{Y_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 2	+25℃		60		ns
$\overline{ENABLE}$ Turn-Off Time	t_{OFF}	$V_{X_}$, $V_{Y_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 2	+25℃		60		ns
Break-Before-Make Time	t_D	$V_{X_}$, $V_{Y_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 3	+25℃		20		ns
Charge Injection	Q	R_S = 0Ω, C = 1nF, V_S = 0V, Test Circuit 4	+25℃		15		pC
Channel-to-Channel Crosstalk	V_{CT}	R_L = 50Ω, f = 1MHz, Test Circuit 5	+25℃		-100		dB
Off Isolation	V_{ISO}	R_L = 50Ω, f = 1MHz, Test Circuit 5	+25℃		-66		dB
Input Off-Capacitance	$C_{X_(OFF)}$, $C_{Y_(OFF)}$	f = 1MHz, Test Circuit 6	+25℃		9		pF
Output Off-Capacitance	$C_{X(OFF)}$, $C_{Y(OFF)}$	f = 1MHz, Test Circuit 6	+25℃		20		pF
Output On-Capacitance	$C_{X(ON)}$, $C_{Y(ON)}$	f = 1MHz, Test Circuit 6	+25℃		40		pF
-3dB Bandwidth	BW	R_L = 50Ω	+25℃		120		MHz
Total Harmonic Distortion	THD	R_L = 600Ω, $5V_{P-P}$, f = 20Hz to 20kHz	+25℃		0.08		%
POWER SUPPLY							
Power Supply Range	V_{CC}, V_{EE}		Full	±1.8		±5.5	V
Power Supply Current	I_{CC}, I_{EE}	V_{CC} = 5.5V, V_{EE} = -5.5V, V_A, V_B, $V_{\overline{ENABLE}}$ = V_{CC} or 0	+25℃		0.01	20	μA

ELECTRICAL CHARACTERISTICS (Single Supply at +5V)

(V_{CC} = 4.5V to 5.5V, V_{EE} = 0V, Full = -40℃ to +85℃, typical values are at T_A = +25℃, unless otherwise noted.)

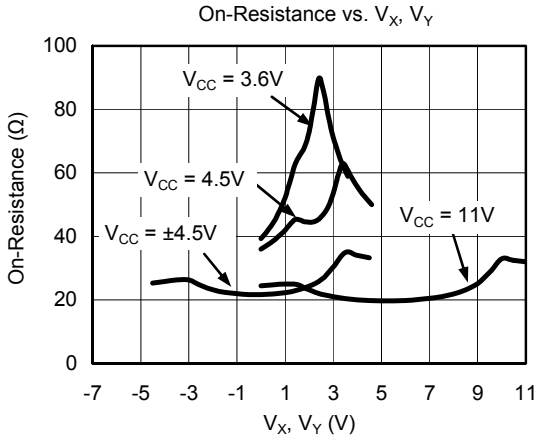
PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{X_}$, $V_{Y_}$, V_X, V_Y		Full	V_{EE}		V_{CC}	V
On-Resistance	R_{ON}	V_{CC} = 4.5V, I_X, I_Y = 1mA	+25℃		66	84	Ω
			Full			97	
On-Resistance Match Between Channels	ΔR_{ON}	V_{CC} = 4.5V, I_X, I_Y = 1mA	+25℃		3	11	Ω
			Full			14	
X_, Y_ Off Leakage Current	$I_{X_(OFF)}$, $I_{Y_(OFF)}$	V_{CC} = 5.5V, $V_{X_}$, $V_{Y_}$ = 1V, 4.5V, V_X, V_Y = 4.5V, 1V	+25℃		10		nA
X, Y Off Leakage Current	$I_{X(OFF)}$, $I_{Y(OFF)}$	V_{CC} = 5.5V, $V_{X_}$, $V_{Y_}$ = 1V, 4.5V, V_X, V_Y = 4.5V, 1V	+25℃		10		nA
X, Y On Leakage Current	$I_{X(ON)}$, $I_{Y(ON)}$	V_{CC} = 5.5V, V_X, V_Y = 4.5V, 1V	+25℃		10		nA
DIGITAL I/O							
Logic Input Logic Threshold High	V_{AH}, V_{BH}, $V_{\overline{ENABLEH}}$		+25℃	2.4			V
Logic Input Logic Threshold Low	V_{AL}, V_{BL}, $V_{\overline{ENABLEL}}$		+25℃			0.8	V
Input-Current High	I_{AH}, I_{BH}, $I_{\overline{ENABLEH}}$	V_A, V_B, $V_{\overline{ENABLE}}$ = V_{CC}	+25℃		10		nA
Input-Current Low	I_{AL}, I_{BL}, $I_{\overline{ENABLEL}}$	V_A, V_B, $V_{\overline{ENABLE}}$ = 0V	+25℃		10		nA
DYNAMIC CHARACTERISTICS							
Address Transition Time	t_{TRANS}	$V_{X_}$, $V_{Y_}$ = 3V/0V, R_L = 300Ω, C_L = 35pF, Test Circuit 1	+25℃		110		ns
$\overline{ENABLE}$ Turn-On Time	t_{ON}	$V_{X_}$, $V_{Y_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 2	+25℃		85		ns
$\overline{ENABLE}$ Turn-Off Time	t_{OFF}	$V_{X_}$, $V_{Y_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 2	+25℃		65		ns
Break-Before-Make Time	t_D	$V_{X_}$, $V_{Y_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 3	+25℃		40		ns
-3dB Bandwidth	BW	R_L = 50Ω	+25℃		140		MHz
Charge Injection	Q	R_S = 0Ω, C = 1nF, V_S = 2.5V, Test Circuit 4	+25℃		2		pC
POWER SUPPLY							
Power Supply Range	V_{CC}, V_{EE}		Full	3.6		11	V
Power Supply Current	I_{CC}, I_{EE}	V_{CC} = 5.5V, V_A, V_B, $V_{\overline{ENABLE}}$ = V_{CC} or 0	+25℃		0.01	20	μA

ELECTRICAL CHARACTERISTICS (Single Supply at +3.6V)

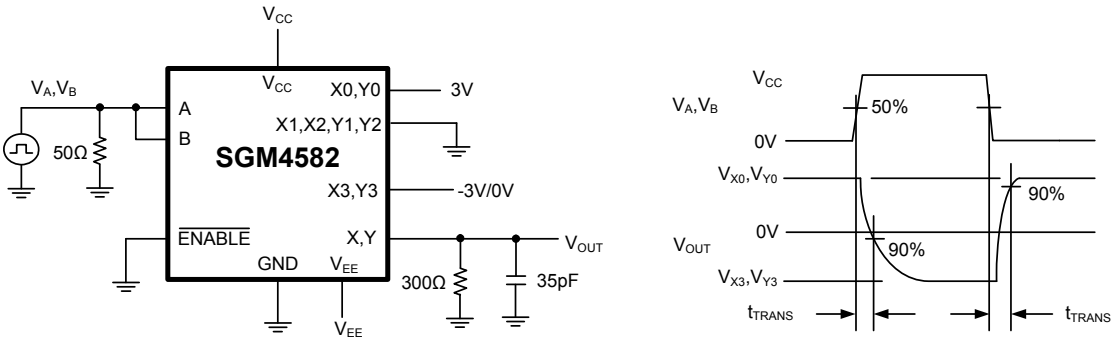
(V_{CC} = 3.6V, V_{EE} = 0V, Full = -40℃ to +85℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{X_}$, $V_{Y_}$, V_X, V_Y		Full	V_{EE}		V_{CC}	V
On-Resistance	R_{ON}	I_X, I_Y = 1mA	+25℃		100	130	Ω
			Full			140	
X_, Y_ Off Leakage Current	$I_{X_(OFF)}$, $I_{Y_(OFF)}$	$V_{X_}$, $V_{Y_}$ = 1V, 3V, V_X, V_Y = 3V, 1V	+25℃		10		nA
X, Y Off Leakage Current	$I_{X(OFF)}$, $I_{Y(OFF)}$	$V_{X_}$, $V_{Y_}$ = 1V, 3V, V_X, V_Y = 3V, 1V	+25℃		10		nA
X, Y On Leakage Current	$I_{X(ON)}$, $I_{Y(ON)}$	V_X, V_Y = 3V, 1V	+25℃		10		nA
DIGITAL I/O							
Logic Input Logic Threshold High	V_{AH}, V_{BH}, $V_{\overline{ENABLEH}}$		+25℃	2			V
Logic Input Logic Threshold Low	V_{AL}, V_{BL}, $V_{\overline{ENABLEL}}$		+25℃			0.5	V
Input-Current High	I_{AH}, I_{BH}, $I_{\overline{ENABLEH}}$	V_A, V_B, $V_{\overline{ENABLE}}$ = V_{CC}	+25℃		10		nA
Input-Current Low	I_{AL}, I_{BL}, $I_{\overline{ENABLEL}}$	V_A, V_B, $V_{\overline{ENABLE}}$ = 0V	+25℃		10		nA
DYNAMIC CHARACTERISTICS							
Address Transition Time	t_{TRANS}	$V_{X_}$, $V_{Y_}$ = 3V/0V, R_L = 300Ω, C_L = 35pF, Test Circuit 1	+25℃		170		ns
$\overline{ENABLE}$ Turn-On Time	t_{ON}	$V_{X_}$, $V_{Y_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 2	+25℃		140		ns
$\overline{ENABLE}$ Turn-Off Time	t_{OFF}	$V_{X_}$, $V_{Y_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 2	+25℃		80		ns
Break-Before-Make Time	t_D	$V_{X_}$, $V_{Y_}$ = 3V, R_L = 300Ω, C_L = 35pF, Test Circuit 3	+25℃		70		ns
-3dB Bandwidth	BW	R_L = 50Ω	+25℃		140		MHz
Charge Injection	Q	R_S = 0Ω, C = 1nF, V_S = 2.5V, Test Circuit 4	+25℃		1		pC
POWER SUPPLY							
Power Supply Current	I_{CC}, I_{EE}	V_{CC} = 3.6V, V_A, V_B, $V_{\overline{ENABLE}}$ = V_{CC} or 0	+25℃		0.01	20	μA

TYPICAL PERFORMANCE CHARACTERISTICS

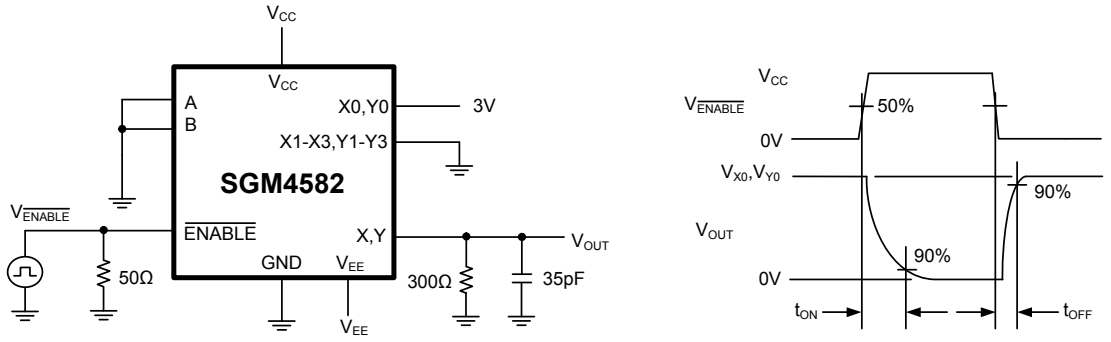


TEST CIRCUITS



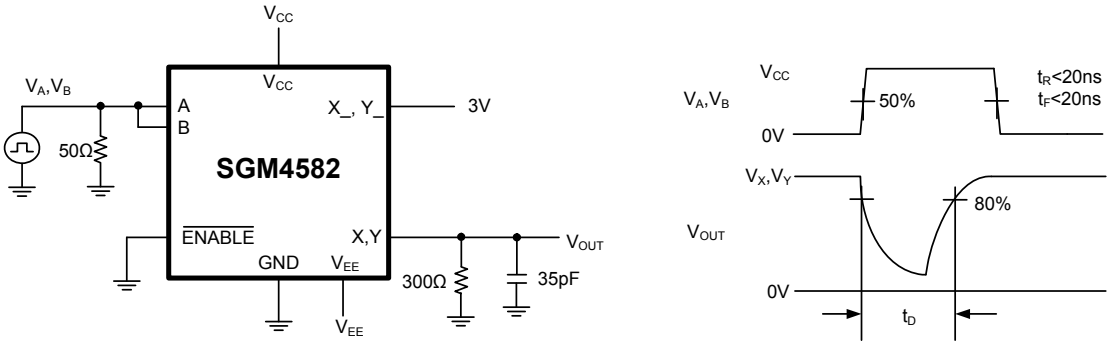
V_{EE} = 0V FOR SINGLE-SUPPLY OPERATION.
TEST EACH SECTION INDIVIDUALLY.

Test Circuit 1. Address Transition Times (t_{TRANS})



V_{EE} = 0V FOR SINGLE-SUPPLY OPERATION.
TEST EACH SECTION INDIVIDUALLY.

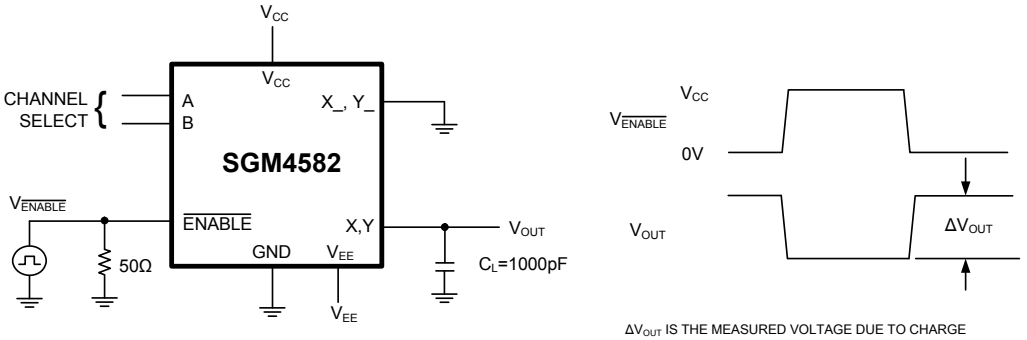
Test Circuit 2. Switching Times (t_{ON}, t_{OFF})



V_{EE} = 0V FOR SINGLE-SUPPLY OPERATION.
TEST EACH SECTION INDIVIDUALLY.

Test Circuit 3. Break-Before-Make Time (t_D)

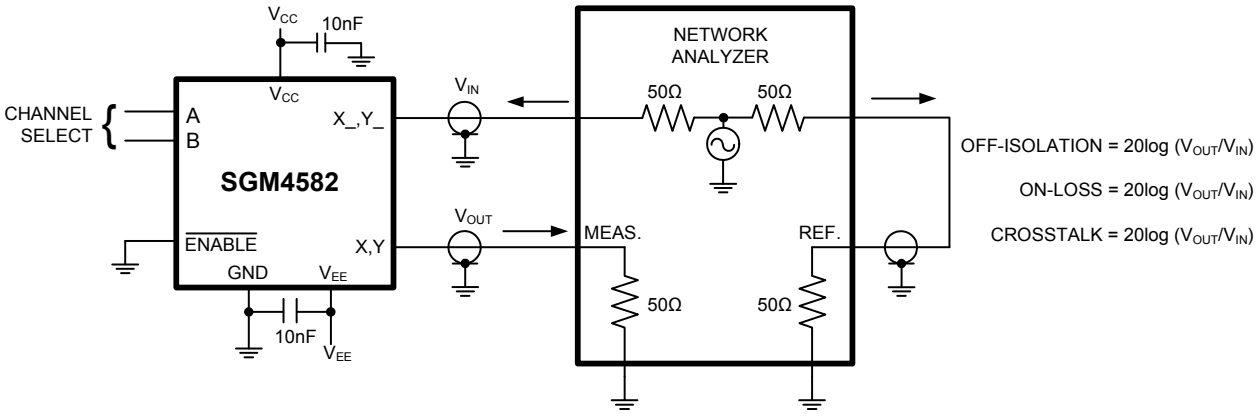
TEST CIRCUITS



V_{EE} = 0V FOR SINGLE-SUPPLY OPERATION.
TEST EACH SECTION INDIVIDUALLY.

ΔV_{OUT} IS THE MEASURED VOLTAGE DUE TO CHARGE TRANSFER ERROR Q WHEN THE CHANNEL TURNS OFF.
$Q = \Delta V_{OUT} \times C_L$

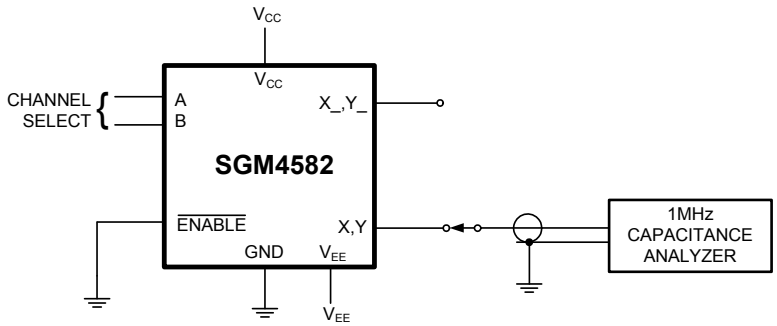
Test Circuit 4. Charge Injection (Q)



MEASUREMENTS ARE STANDARDIZED AGAINST SHORT AT SOCKET TERMINALS.
OFF-ISOLATION IS MEASURED BETWEEN COM AND "OFF" NO TERMINAL ON EACH SWITCH.
ON-LOSS IS MEASURED BETWEEN COM AND "ON" NO TERMINAL ON EACH SWITCH.
CROSSTALK IS MEASURED FROM ONE CHANNEL (A, B) TO ALL OTHER CHANNELS.

SIGNAL DIRECTION THROUGH SWITCH IS REVERSED; WORST VALUES ARE RECORDED.

Test Circuit 5. Off Isolation, On Loss and Crosstalk



V_{EE} = 0V FOR SINGLE-SUPPLY OPERATION.
TEST EACH SECTION INDIVIDUALLY.

Test Circuit 6. Capacitance

APPLICATION INFORMATION

Power-Supply Considerations

Overview

The SGM4582 construction is typical of most CMOS analog switch. It has three supply pins: V_{CC}, V_{EE}, and GND. V_{CC} and V_{EE} are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD protection diodes are internally connected between each analog-signal pin and both V_{CC} and V_{EE}. If any analog signal exceeds V_{CC} or V_{EE}, one of these diodes will conduct. During normal operation, these and other reverse-biased ESD diodes leak, forming the only current drawn from V_{CC} or V_{EE}.

Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V_{CC} or V_{EE} and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V_{CC} and V_{EE} pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog-signal paths and GND. V_{CC} and GND power the internal logic and logic-level translators, and set the input logic limits. The logic-level translators convert the logic levels into switched V_{CC} and V_{EE} signals to drive the gates of the analog signals. This drive signal is the only connection between the logic supplies and signals and the analog supplies. V_{CC} and V_{EE} have ESD-protection diodes to GND.

Bipolar Supplies

This device operates with bipolar supplies between ±1.8V and ±5.5V. The V_{CC} and V_{EE} supplies need not be symmetrical, but their sum cannot exceed the +13.2V absolute maximum rating.

Single Supply

This device operates from a single supply between +3.6V and +11V when V_{EE} is connected to GND. All of the bipolar precautions must be observed. At room temperature, it actually “works” with a single supply near or below +2.5V, although as supply voltage decreases, switch on-resistance and switching times become very high.

Over-Voltage Protection

Proper power-supply sequencing is recommended for the CMOS device. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V_{CC} on first, then V_{EE}, followed by the logic inputs and analog signals. If power-supply sequencing is not possible, add two small signal diodes (D1, D2) in series with the supply pins for over-voltage protection (Figure 1). Adding diodes reduces the analog-signal range to one diode drop below V_{CC} and one diode drop above V_{EE}, but does not affect the device’s low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V_{CC} and V_{EE} should not exceed 13.2V. These protection diodes are not recommended when using a single supply if signal levels must extend to ground.

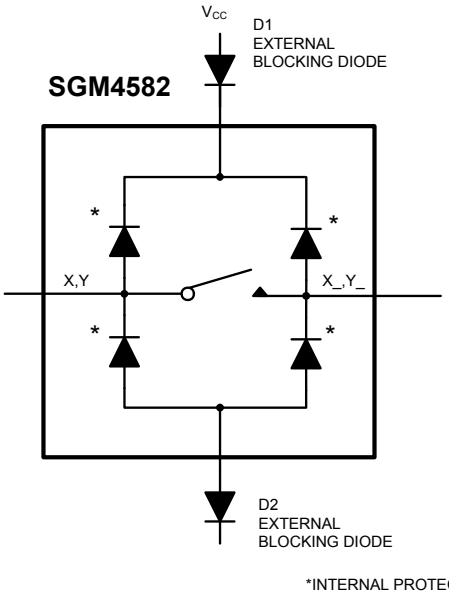
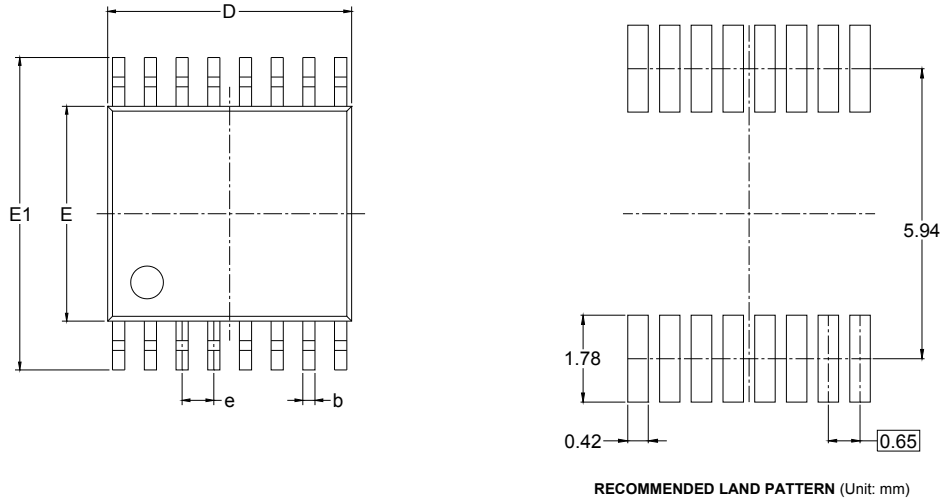


Figure 1. Over-Voltage Protection Using External Blocking Diodes

PACKAGE OUTLINE DIMENSIONS

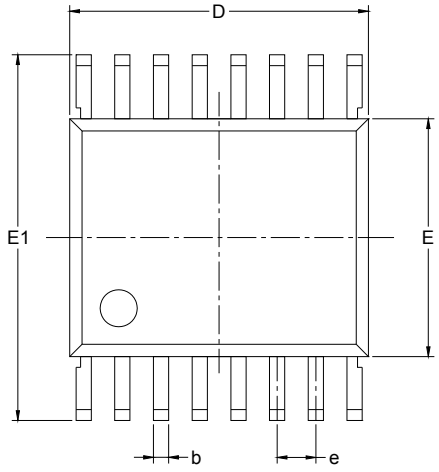
TSSOP-16

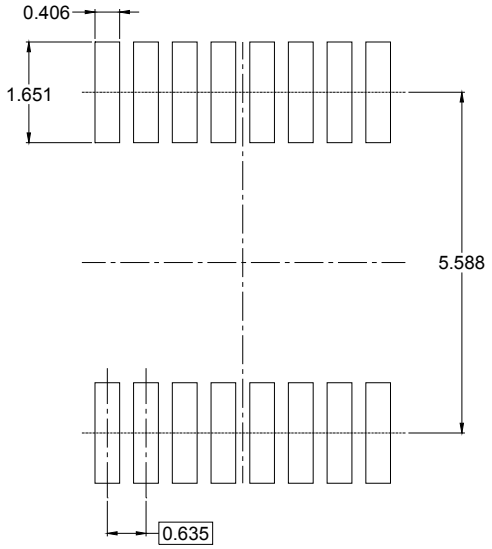


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.100		0.043
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

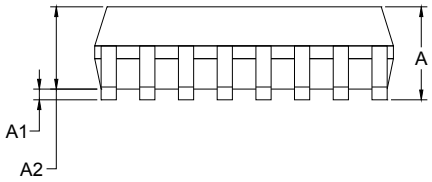
PACKAGE OUTLINE DIMENSIONS

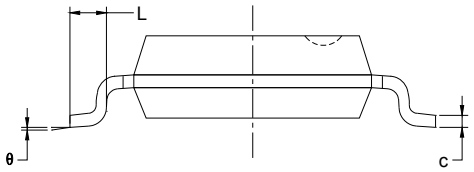
SSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)

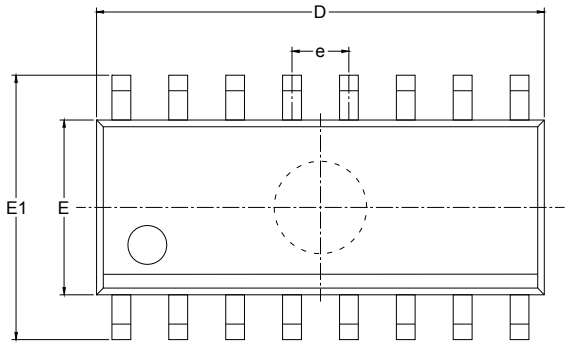


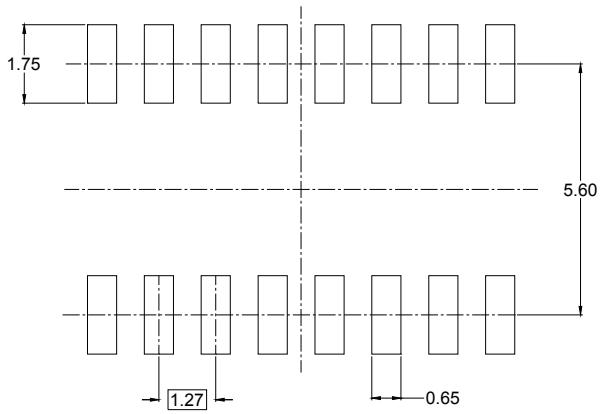


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.200	0.300	0.008	0.012
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	0.635 BSC		0.025 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

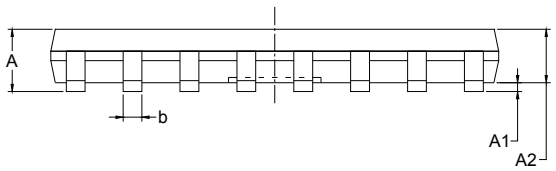
PACKAGE OUTLINE DIMENSIONS

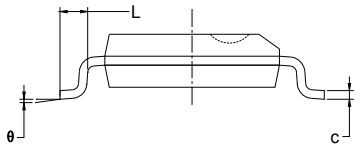
SOIC-16





RECOMMENDED LAND PATTERN (Unit: mm)

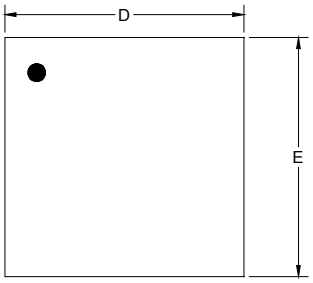




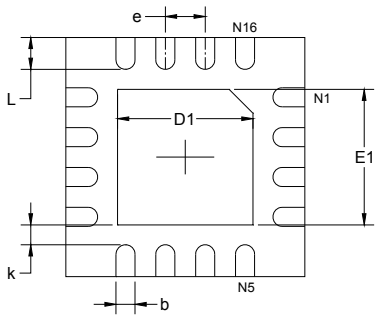
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

PACKAGE OUTLINE DIMENSIONS

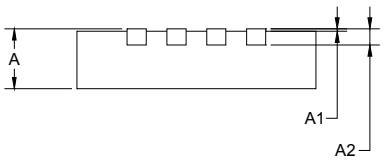
TQFN-3×3-16L



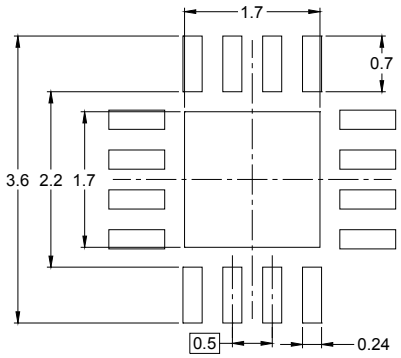
TOP VIEW



BOTTOM VIEW



SIDE VIEW

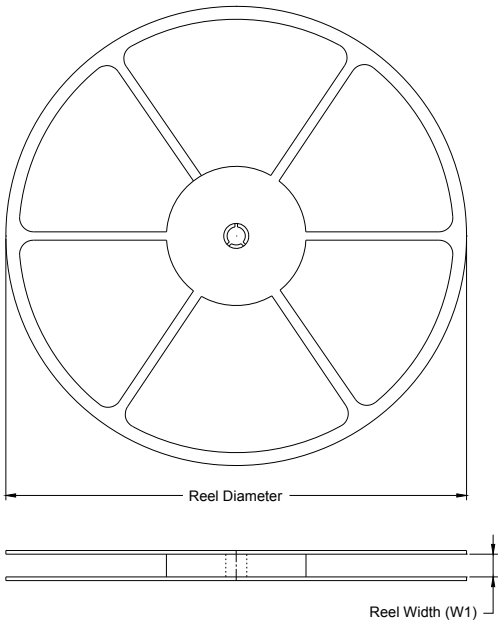


RECOMMENDED LAND PATTERN (Unit: mm)

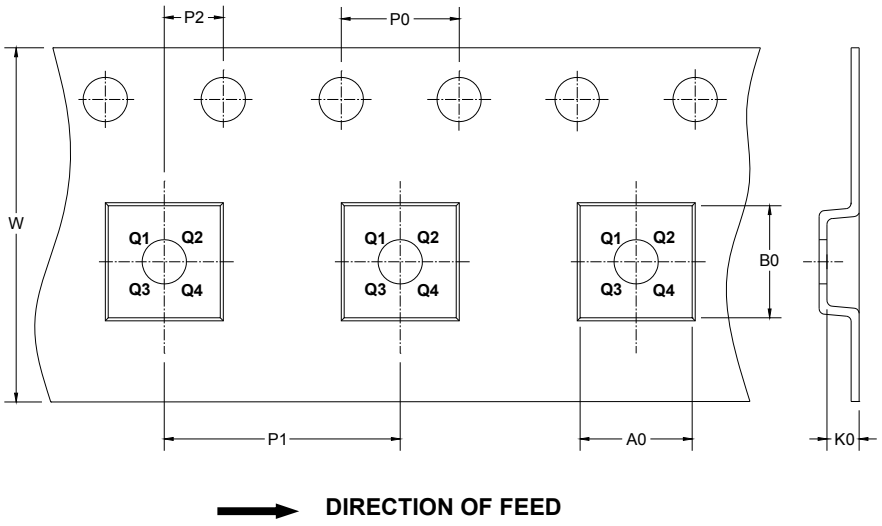
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E1	1.600	1.800	0.063	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS

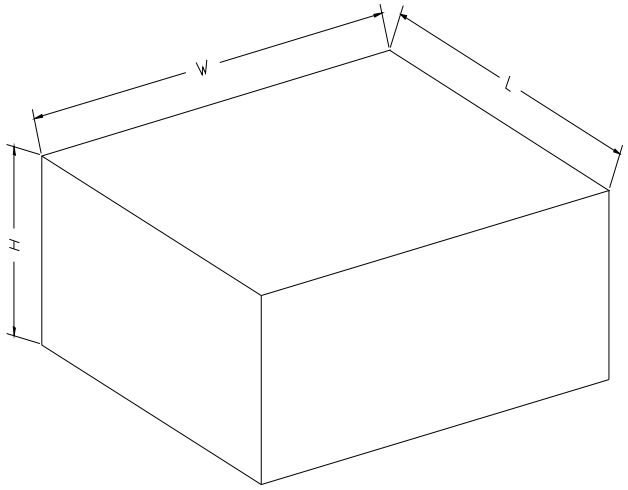


NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-16	13″	16.4	6.5	10.3	2.1	4.0	8.0	2.0	16.0	Q1
SSOP-16	13″	12.4	6.4	5.4	2.1	4.0	8.0	2.0	12.0	Q1
TSSOP-16	13″	12.4	6.9	5.6	1.2	4.0	8.0	2.0	12.0	Q1
TQFN-3×3-16L	13″	12.40	3.35	3.35	1.13	4.00	4.00	2.00	12.00	Q1

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5