## FEATURES

- 5-phase dual output PWM Controller
- Phases are flexibly assigned between Loops 1 & 2
- Intel® VR12, AMD® 400kHz & 3.4MHz SVI and Memory modes
- Dual OCP support for I-spike enhanced AMD CPUs
- SMB_Alert Pin for Servers
- PMBus Address pin or Variable Gate Drive (IR3541/CHL8325A)
- 2nd Temperature Sense for VR12 Desktop (CHL8325B)
- Overclocking & Gaming Mode with Vmax setting
- Switching frequency from 200kHz to 1.2MHz per phase
- IR Efficiency Shaping Features including Variable Gate Drive (IR3541/CHL8325A only) and Dynamic Phase Control
- Programmable 1-phase or 2-phase for Light Loads and Active Diode Emulation for Very Light Loads
- IR Adaptive Transient Algorithm (ATA) on both loops minimizes output bulk capacitors and system cost
- Auto-Phase Detection with auto-compensation
- Per-Loop Fault Protection: OVP, UVP, OCP, OTP, CFP
- I2C/SMBus/PMBus system interface for telemetry of Temperature, Voltage, Current & Power for both loops
- Non-Volatile Memory (NVM) for custom configuration
- Compatible with IR ATL and 3.3V Tri-state Drivers
- +3.3V supply voltage; -20ºC to 85ºC ambient operation
- Pb-Free, RoHS, 6x6 40-pin QFN, MSL2 package

## APPLICATIONS

- Intel ® VR12 & AMD® SVI based systems
- DDR Memory with Vtt tracking
- Overclocked & Gaming platforms

## DESCRIPTION

The IR3541 and CHL8325A/B are dual-loop digital multi-phase buck controllers that drive up to 5 phases. The IR3541 and CHL8325A/B are fully Intel® VR12 and AMD® SVI compliant on both loops and provides a Vtt tracking function for DDR memory.

NVM storage saves pins and enables a small package size.

The IR3541 and CHL8325A/B include the IR Efficiency Shaping Technology to deliver exceptional efficiency at minimum cost across the entire load range. IR Variable Gate Drive optimizes the MOSFET gate drive voltage as a function of real-time load current. IR Dynamic Phase Control adds/drops active phases based upon load current. The IR3541 and CHL8325A/B can be configured to enter 1-phase operation and active diode emulation mode automatically or by command.

IR's unique Adaptive Transient Algorithm (ATA), based on proprietary non-linear digital PWM algorithms, minimizes output bulk capacitors.

The I2C/PMBus interface can communicate with up to 16 IR3541 and CHL8325A/B based VR loops. Device configuration and fault parameters are easily defined using the IR Intuitive Power Designer (DPDC) GUI and stored in on-chip NVM.

The IR3541 and CHL8325A/B also include numerous features like register diagnostics for fast design cycles and platform differentiation, truly simplifying VRD design and enabling fastest time-to-market with its "set-and-forget" methodology.

## PIN DIAGRAM

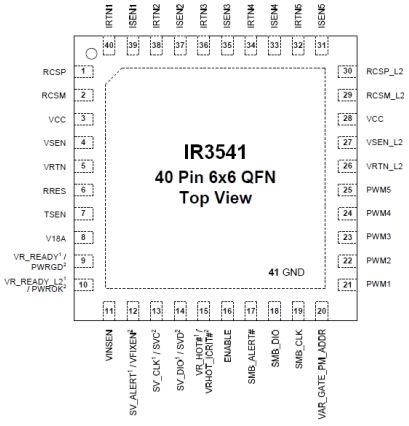
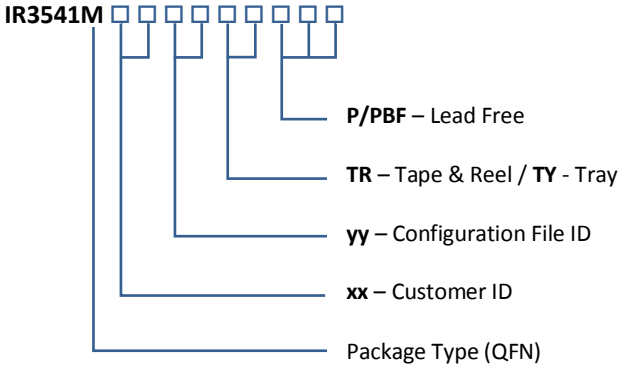



Figure 1: IR3541 Package Top View

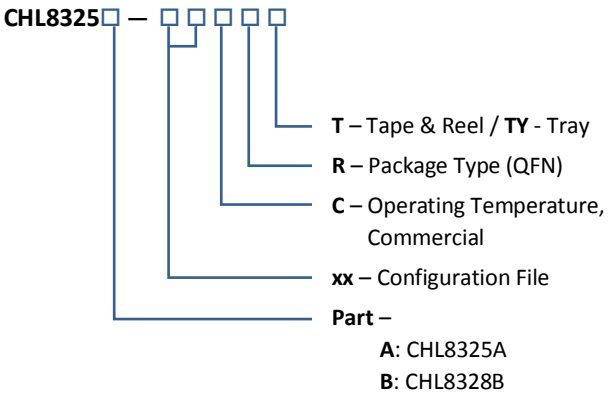
## ORDERING INFORMATION




| Package | Packing Qty | Part Number | Programming |
|---|---|---|---|
| QFN | TR=3000<br>TY=4900 | IR3541MTRPBF<br>IR3541MTYPBF | Default |
| QFN | TR=3000 | IR3541MxxyyTRP[1] | Customer Configuration |

**Notes:**

**1.** Customer Specific Configuration File, where xx = Customer ID and yy = Configuration File (Codes assigned by IR Marketing).




| Package | Packing Qty | Part Number |
|---|---|---|
| QFN | T=3000<br>TY=4900 | CHL8325A-00CRT<br>CHL8325A-00CRTY |
| QFN | T=3000 | CHL8325A-xxCRT[1] |
| QFN | T=3000<br>TY=4900 | CHL8325B-00CRT<br>CHL8325B-00CRTY |
| QFN | T=3000 | CHL8325B-xxCRT[1] |

**Notes:**

**1.** "xx" indicates a customer specific configuration file.

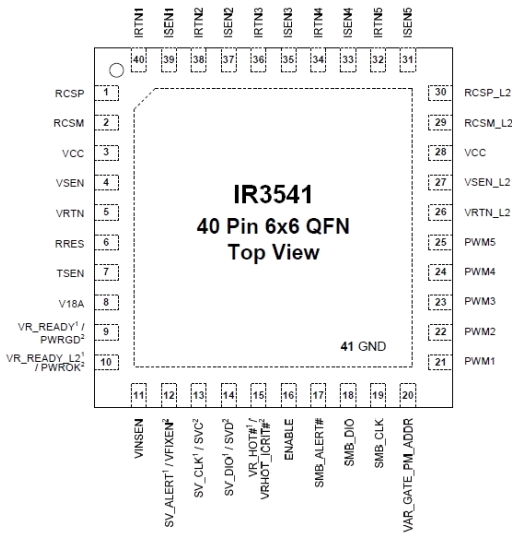



Figure 2: IR3541 Package Top View, Enlarged

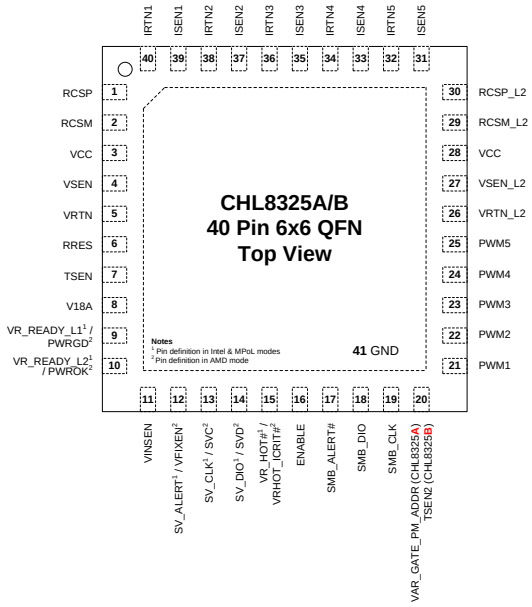



Figure 3: CHL8325A/B Package Top View, Enlarged

## FUNCTIONAL BLOCK DIAGRAM

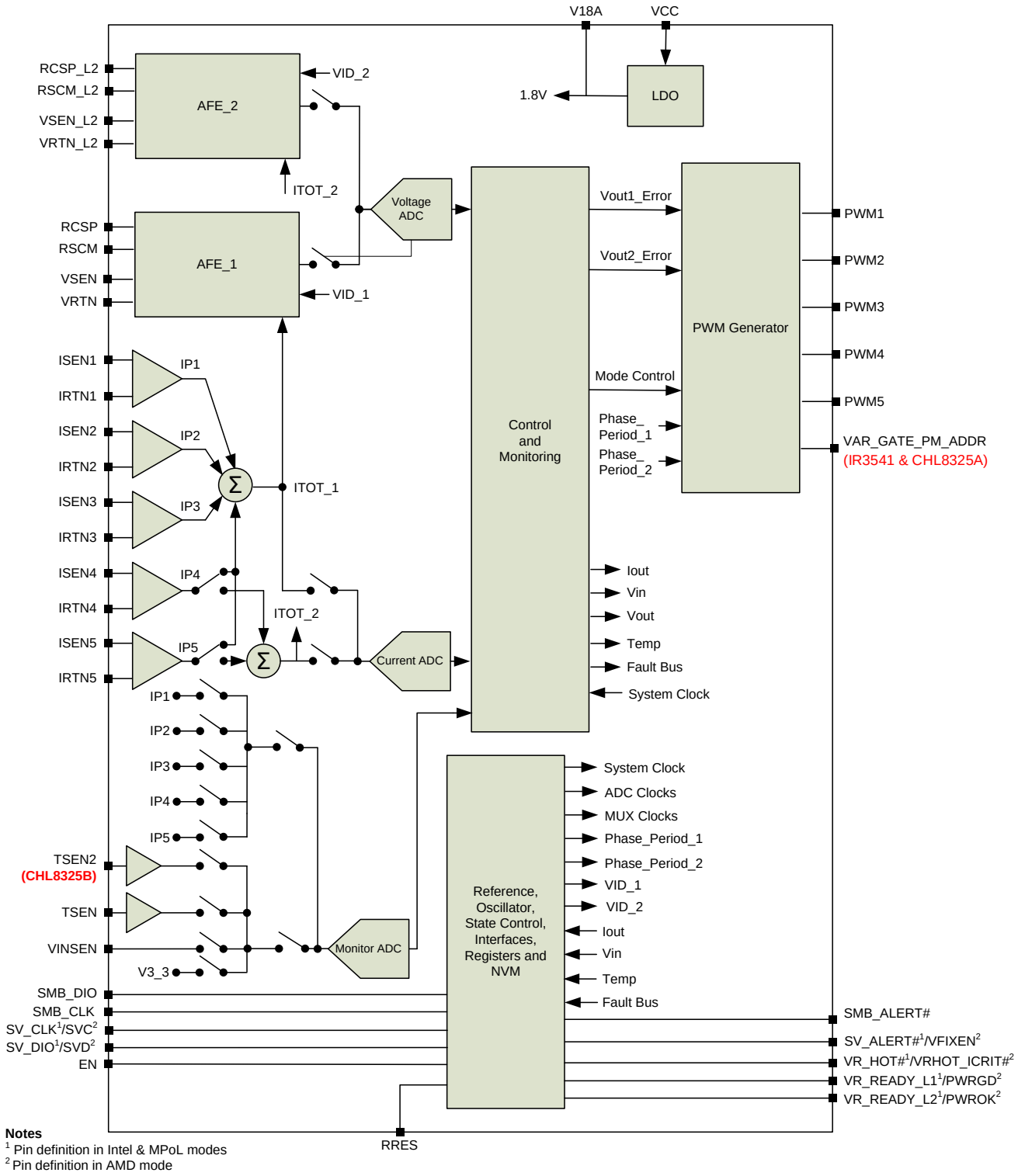



Figure 4: IR3541 and CHL8325A/B Functional Block Diagram