1. General Description

The DM9601 is a fully integrated and cost-effective single chip USB to Fast Ethernet MAC controller with 10/100 PHY. It is designed with the low power and high performance process. It is a 3.3V device with 5V tolerance and it supports 3.3V and 5V signaling.

The DM9601 provides USB transceiver which is compliant with USB1.1, 10/100M PHY, MAC controller, memory controller and an external MII interface, to connect HPNA device or other transceivers that support MII interface. This chip already integrates into 16K byte SRAM. The DM9601 has interfaces to the UTP3, 4, 5 in 10Base-T and UTP5 in 100Base-TX. It is fully compliant with the IEEE 802.3u Spec. Its auto-negotiation function will automatically configure the DM9601 to take the maximum advantage of its abilities. The DM9601 also supports IEEE 802.3x full-duplex flow control.

The DM9601 supports 3 wake-up event to wake-up system from suspend mode. There are 7 GPIO pins (General purpose I/O) for user's application.

2. Block Diagram

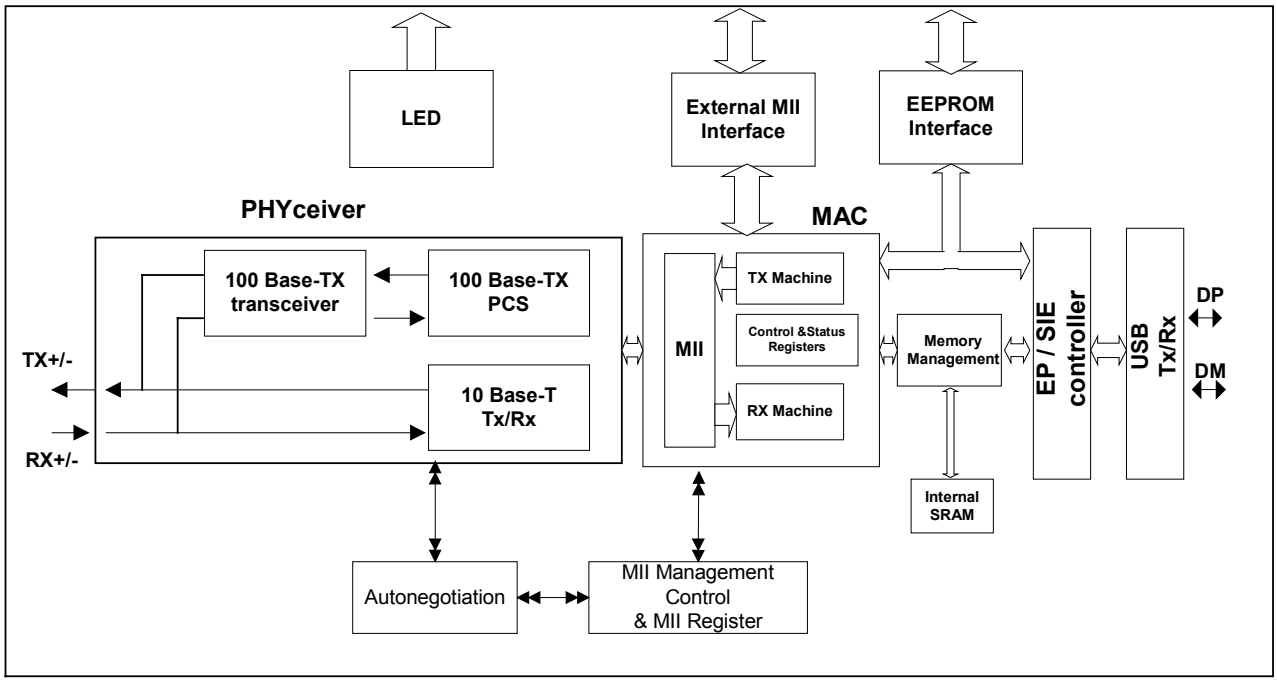


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3. Features

3.1 USB Characteristics

- USB Specification revision 1.1 compliant
- Supports 12MHz Full-Speed operation
- Supports suspend mode and remote wake up resume
- Supports USB standard commands
- Supports vendor specific commands
- Supports test-mode for memory test.
- Efficient TX/RX FIFO auto management.

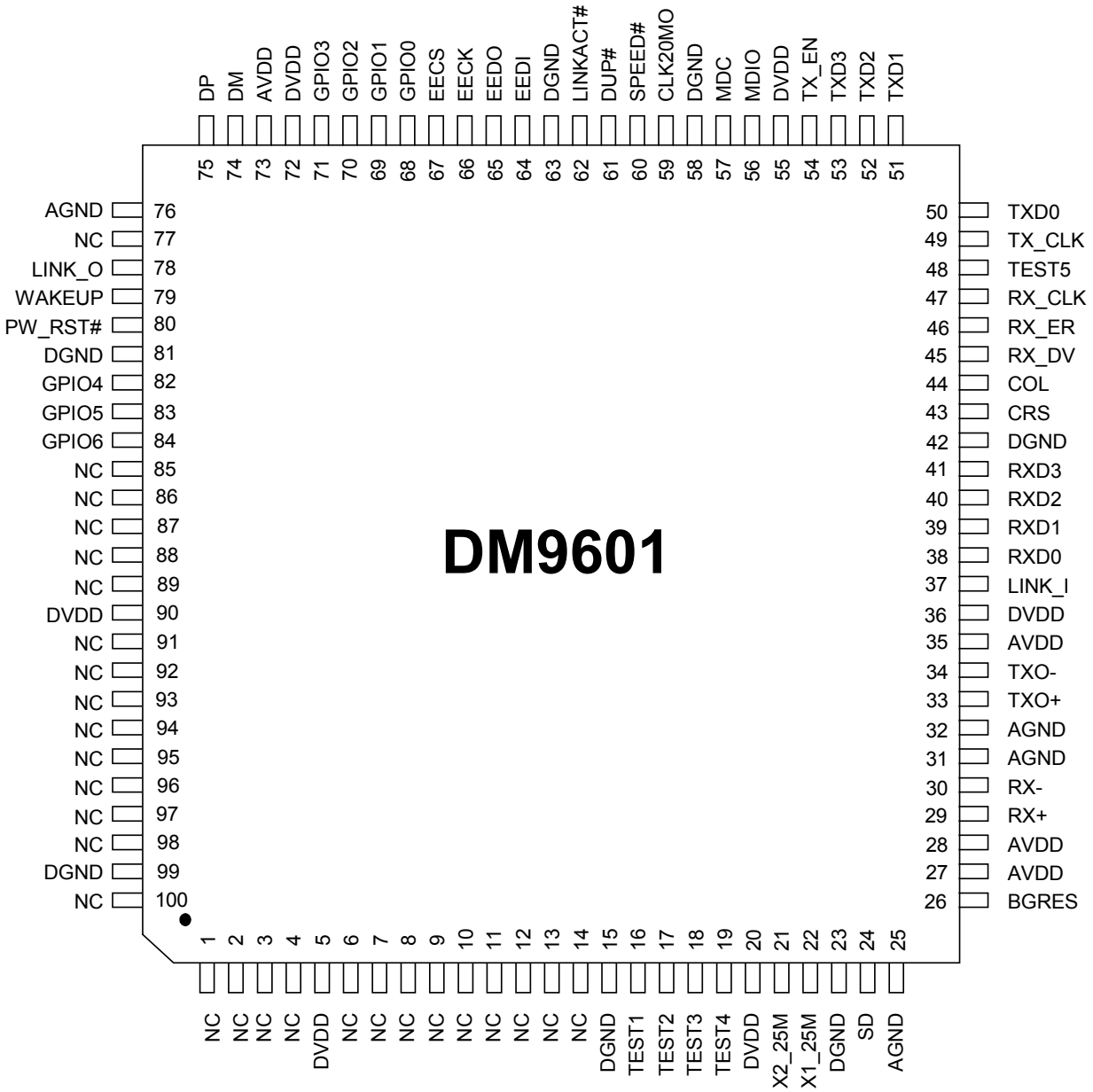
3.2 Transceiver

- 10/100M PHY
- USB 1.1

3.3 Other

- Supports large internal 16K byte SRAM
- Supports automatically load vendor ID and product ID from EEPROM
- Supports MII and the reverse MII interface
- IEEE802.3x flow control for full-duplex mode
- Back Pressure Mode for half-duplex mode flow control
- Supports wakeup frame, link status change and Magic packet events for remote wake-up
- Low-Power, Single-Supply 3.3V CMOS technology
- Very Low Power Consumption mode
  - Power Reduced mode(cable detection)
  - Power Down mode
  - Selectable TX drivers for 1:1 or 1.25:1 transformers for additional power reduction.
- Compatible with 3.3V and 5.0V tolerant I/O
- 100-pin LQFP

4. Pin Configuration: 100 Pin LQFP & with MII Interface Mode



5. Pin Description

I= Input, O=Output, I/O= Input/Output, O/D= Open Drain, P= Power,

LI= reset Latch Input, #= asserted low

5.1 MII Interface

Pin No.	Pin Name	Type	Description
37	LINK_I	I/O	External MII Device Link Status
38,39,40, 41	RXD[3:0]	I/O	External MII Receive Data
43	CRS	I/O	External MII Carrier Sense
44	COL	I/O	External MII Collision Detect
45	RX_DV	I/O	External MII Receive Data Valid
46	RX_ER	I/O	External MII Receive Error
47	RX_CLK	I/O	External MII Receive Clock
49	TX_CLK	I/O	External MII Transmit Clock
50,51,52, 53	TXD[3:0]	I/O	External MII Transmit Data
54	TX_EN	I/O	External MII Transmit Enable
56	MDIO	I/O	MII Serial Management Data
57	MDC	I/O	MII Serial Management Data Clock

5.2 EEPROM Interface

EEPROM Interface			
64	EEDI	I/O	Data from EEPROM
65	EEDO	I/O	Data to EEPROM
66	EECK	I/O	Clock to EEPROM
67	EECS	O	Chip Select to EEPROM This pin is used as a strap pin to define the LED modes When it is pulled high, the LED mode is the mode 1, Otherwise it is mode 0

5.3 USB Interface

74	DM	I/O	USB Data Minus
75	DP	I/O	USB Data Plus

5.4 Clock Interface

21	X2_25M	I/O	Crystal 25MHz Out
22	X1_25M	I/O	Crystal 25MHz In
59	CLK20MO	I/O	20Mhz Clock Output

5.5 LED Interface

60	SPEED100#	O	Speed LED It's low output indicates that the internal PHY is operated in 100M speed, or it is floating for the 10M mode of the internal PHY.
61	DUP#	O	Full-duplex LED In LED mode 1, It's low output indicates that the internal PHY is operated in full-duplex mode, or it is floating for the half-duplex mode of the internal PHY. In LED mode 0, It's low output indicates that the internal PHY is operated in 10M mode, or it is floating for the 100M mode of the internal PHY.
62	LINK&ACT#	O	Link LED In LED mode 1, it is the combined LED of link and carrier sense signal of the internal PHY. In LED mode 0, it is the LED of the carrier sense signal of the internal PHY only.

5.6 10/100 PHY/Fiber

24	SD	I	Fiber-optic Signal Detect PECL signal indicates whether or not the fiber-optic receives pair is receiving valid levels.
25	AGND		Bandgap Ground.
26	BGRES	I/O	Bandgap Pin.
27	AVDD		Bandgap and Guard Ring Power
28	AVDD		RX Power
29	RX+	I	TP RX Input
30	RX-	I	TP RX Input
31	AGND		RX Ground
32	AGND		TX Ground
33	TXO+	O	TP TX Output
34	TXO-	O	TP TX Output
35	AVDD		TX Power

5.7 Miscellaneous

16	MII MODE	I	Tie to DVDD if connects with Ethernet's PHY through External MII. Otherwise tie it to ground.
48	TEST5	I	It Must be Ground
68,69,70, 71,82,83, 84	GPIO0~6	I/O	General I/O Ports Registers GPCR and GPR can program these pins The GPIO0 is an output mode with output data high at default to power

			down internal PHY and other external MII device GPIO1~6 default are input ports
78	LINK_O	O	Cable Link Status Output. Active High This pin is also used as a strap pin to define the MII interface is the reversed MII interface (pulled high) or the normal MII interface (not pulled high)
79	WAKEUP	O	Issue a wake-up signal when wake-up event happens
80	PW_RST#	I	Hardware Reset Active low signal to initiate the DM9601
1,2,3,4,6,7, 8,9,10,11, 12,13,14, 77,85,86, 87,88,89, 91,92,93, 94,95,96, 97,98,100	NC		Not Connected

5.8 Power Pins

5,20,36,55, 72,90,	DVDD		Digital VCC
15,17,18, 19,23,42, 48,58,63, 81,99	DGND		Digital GND
73	AVDD		Analog VCC
76	AGND		Analog GND

6. USB Standard Command

6.1 Supported Standard Command

Setup Stage					Data Stage
BmReqType	BRequest	wValue	wIndex	wLength	Data
00000000B	CLEAR_FEATURE	Feature Selector	Zero	Zero	None
00000001B			Interface		
00000010B			Endpoint		
10000000B	GET_CONFIGURATION	Zero	Zero	One	Configuration value
10000000B	GET_DESCRIPTOR	Descriptor type/index	Zero/LID	Length	Descriptor
10000001B	GET_INTERFACE	Zero	Interface	One	Alternate Interface
10000000B	GET_STATUS	Zero	Zero	Two	Status
10000001B			Interface		
10000010B			Endpoint		
00000000B	SET_ADDRESS	Device address	Zero	Zero	None
00000000B	SET_CONFIGURATION	Configuration value	Zero	Zero	None
00000000B	SET_DESCRIPTOR	Descriptor type/index	Zero/LID	Length	Descriptor
00000000B	SET_FEATURE	Feature Selector	Zero	Zero	None
00000001B			Interface		
00000010B			Endpoint		
00000001B	SET_INTERFACE	Alternate setting	Interface	Zero	None
10000010B	SYNCH_FRAME	Zero	Endpoint	Two	Frame Number

6.2 Not Supported Standard Commands

- Clear_Feature (Interface)
- Set_Feature (Interface)
- Set_Descriptor ( )
- Sync_Frame ( )

7. Vendor commands

There are two types of vendor's command. We can access internal register maximum 256 bytes, and can access external maximum memory 16KB/32KB/64KB/128KB.

7.1 Register Type

READ_REGISTER( )

Setup Stage

BmReqType	bReq	WValue		WIndex		wLength	
Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
C0H	00H	00H	00H	RegOffset [7:0]	00H	BC[7:0]	00H

WRITE_REGISTER( )

Setup Stage

BmReqType	bReq	WValue		wIndex		wLength	
Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
40H	01H	00H	00H	RegOffset[7:0]	00H	BC[7:0]	00H

WRITE1_REGISTER( )

Setup Stage

BmReqType	bReq	Wvalue		wIndex		wLength	
Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
40H	03H	Data[7:0]	00H	RegOffset[7:0]	00H	0000H	

7.2 Memory Type

These kinds of commands are valid when the bit "MEM_MODE " is set, otherwise the device will respond with request error when receiving these commands.

READ_MEMORY( )

Setup Stage

BmReqType	Breq	Wvalue		Windex		wLength	
Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
C0H	02H	00H	00H	MemOff[7:0]	MemOff[15:8]	BC[7:0]	00H

WRITE_MEMORY( )

Setup Stage

BmReqType	BReq	Wvalue		Windex		wLength	
Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
40H	05H	00H	00H	MemOff[7:0]	MemOff[15:8]	BC[7:0]	00H

WRITE1_MEMORY( )

Setup Stage

BmReqType	Breq	Wvalue		Windex		wLength	
Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
40H	07H	Data[7:0]	00H	MemOff[7:0]	MemOff[15:8]	0000H	

Note:

There are advantages (for USB 1.1) when we define "WRITE_XXXXX" and "WRITER1_XXXXX" as two different commands. There will be only "set up stage" and "status stage", but no "data stage" in USB bus for WRITE1_XXXXX command.

8. Interface 0 Configuration

8.1 Endpoint 1

Type: Bulk In
Packet Load: 64-byte
When host is accessing EP1.
If IN-FIFO is full, device will send 64-byte data.
If IN-FIFO isn't full and Ethernet packet isn't end, device will send a NAK.
If IN-FIFO isn't full and Ethernet packet is end, device will send the surplus data in IN-FIFO.

Data Format

Fist byte : Packet Status
Second byte : Packet byte count low
Third byte : Packet byte count high
The others : Packet

8.2 Endpoint 2

Type: Bulk Out
Packet Load: 64-byte
When host is accessing EP2.
If OUT-FIFO is empty, host sends data, device responds to ACK.
If OUT-FIFO isn't empty, host sends data, device responds to NAK.
If host sends data less then 64-byte or zero byte, it means Ethernet packet ends.

Data Format

First byte : Packet byte count low
Second byte : Packet byte count high
The others : Packet

8.3 Endpoint 3

Type: Interrupt In
Packet Load: 8-byte
When host accessing EP3.
If there is no interrupt condition, device responds to NAK.
If interrupt condition, device will send content back to host.

Data Format

Offset	Name	Description
Byte 0	NSR	Network Status Register
Byte 1	TSR1	TX Status Register1
Byte 2	TSR2	TX Status Register2
Byte 3	RSR	RX Status Register
Byte 4	ROCR	Received Overflow Counter Register
Byte 5	RXC	Received Packet Counter
Byte 6	TXC	Transmit Packet Counter
Byte 7	GPR	General Purpose Register

9. Descriptor Values

All descriptors are stored in it's default values. Values which are "?" in the table below are under define.

9.1 Device Descriptor/18-Byte

Offset	Field	Size	Value	Description
0	bLength	1	12H	Size of descriptor in bytes
1	bDescriptorType	1	01H	DEVICE Descriptor Type
2	bcdUSB	2	0110H	USB BCD version
4	bDeviceClass	1	00H	Class code, assign by USB
				Zero: No device level class
				01H~FEH : Valid device class
				FFH : Vender-specific
5	bDeviceSubClass	1	00H	SubClass code, assign by USB
6	bDeviceProtocol	1	00H	Protocol code, assign by USB
7	bMaxPacketSize0	1	08H	Maximum PL for EP0(8,16,32,64)
8	idVender	2	0A46H	Vendor ID(2630)
10	idProduce	2	9601H	Product ID(9601)
12	bcdDevice	2	0101H	Device release number
14	iManufacturer	1	01H	Index of string descriptor for manufacturer
15	iProduct	1	02H	Index of string descriptor for product
16	iSerialNumber	1	03H	Index of string descriptors for serial number
17	bNumConfigurations	1	01H	Number of configurations

9.2 Configuration0 Descriptor/9-Byte

Offset	Field	Size	Value	Description
0	bLength	1	09H	Size of descriptors
1	bDescriptorType	1	02H	CONFIGURATION Descriptor Type
2	wTotalLength	2	0027H	Total descriptor length
4	bNumInterfaces	1	01H	Number of interfaces
5	bConfigurationValue	1	00H	Value of this configuration
6	iConfiguration	1	00H	Index of string descriptor for configuration
7	bmAttributes	1	A0H	Configuration characteristics
				D7:Reserved (set to 1)
				D6: Self-powered
				D5: Remote WakeUp
				D4: Reserved (reset to 0)
8	MaxPower	1	3CH	Maximum power, 2mA units

9.3 Interface0 Descriptor/9-Byte

Offset	Field	Size	Value	Description
0	bLength	1	09H	Size of this descriptor
1	bDescriptorType	1	04H	INTERFACE Descriptor Typr
2	bInterfaceNumber	1	00H	Number of interface
3	bAlternateSetting	1	00H	Value used to select alternate setting
4	bNumEndpoints	1	03H	Number of ednpoints
5	bInterfaceClass	1	00H	Class code
6	bInterfaceSubClass	1	00H	SunClass code
7	bInterfaceProtocol	1	00H	Protocol code
8	iInterface	1	00H	Index of string for this interface

9.4 Endpoint1 Descriptor/6-Byte

Offset	Field	Size	Value	Description
0	bLength	1	07H	Size of this descriptor
1	bDescriptorType	1	05H	ENDPOINT Descriptor Type
2	bEndpointAddress	1	81H	Address of the endpoint
				Bit3~0: The endpoint number
				Bit 6~4: Reserved(0)
				Bit7 : Direction(Control EP exclude)
				0 = OUT endpoint
				1 = IN endpoint
3	bmAttributes	1	02H	EP's attributes
				Bit1~0: Transfer Type
				00 = Control
				01 = Isochronous
				10 = Bulk
				11 = Interrupt
4	wMaxPacketSize	2	0040H	Maximum packet size of this EP
6	bInterval	1	00H	Interval for polling (periodical pipe)
				Interrupt Tpye = 1 ~ 255 (ms)
				Isochronoous Type = 1 (ms)

9.5 Endpoint3 Descriptor/6-Byte

Offset	Field	Size	Value	Description
0	bLength	1	07H	Size of this descriptor
1	bDescriptorType	1	05H	ENDPOINT Descriptor Typr
2	bEndpointAddress	1	83H	Address of the endpoint
				Bit3~0: The endpoint number
				Bit 6~4: Reserved(0)
				Bit7 : Direction(Control EP exclude)
				0 = OUT endpoint
				1 = IN endpoint
3	bmAttributes	1	03H	EP's attributes
				Bit1~0: Transfer Type
				00 = Control
				01 = Isochronous
				10 = Bulk
				11 = Interrupt
4	wMaxPacketSize	2	0008H	Maximum packet size of this EP
6	bInterval	1	01H	Interval for polling (periodical pipe)
				Interrupt Tpye = 1 ~ 255 (ms)
				Isochronoous Type = 1 (ms)

9.6 String0 Descriptor/Code array

Offset	Field	Size	Value	Description
0	bLength	1	04H	Size of this descriptor
1	bDescriptorType	1	03H	STRING Descriptor Type
2	wLANGID[1]	2	0409H	LANGID code(Eng.)

9.7 String0 Descriptor1/2/3 are loaded from EEPROM

String1 Descriptor/UNICODE String

Offset	Field	Size	Value	Description
0	bLength	1		Descriptor length loading from EEPROM
1	bDescriptorType	1	03H	STRING Descriptor Typr
2~	bString	n		Manufacture

String2 Descriptor/UNICODE String

Offset	Field	Size	Value	Description
0	bLength	1		Descriptor length loading from EEPROM
1	bDescriptorType	1	03H	STRING Descriptor Typr
2~	bString	n		Product

String3 Descriptor/UNICODE String

Offset	Field	Size	Value	Description
0	bLength	1		Descriptor length loading from EEPROM
1	bDescriptorType	1	03H	STRING Descriptor Typr
2~	bString	n		Serial Number

10. Vendor Control and Status Register Set

The DM9601 implements several control and status registers, which can be accessed by the USB vendor register type commands. All CRs are set to their default values by hardware or software reset unless they are specified.

Register	Description	Offset	Default value after reset
NCR	Network Control Register	00H	00H
NSR	Network Status Register	01H	00H
TCR	TX Control Register	02H	00H
TSR I	TX Status Register I	03H	00H
TSR II	TX Status Register II	04H	00H
RCR	RX Control Register	05H	00H
RSR	RX Status Register	06H	00H
ROCR	Receive Overflow Counter Register	07H	00H
BPTR	Back Pressure Threshold Register	08H	37H
FCTR	Flow Control Threshold Register	09H	38H
FCR	RX Flow Control Register	0AH	00H
EPCR	EEPROM & PHY Control Register	0BH	00H
EPAR	EEPROM & PHY Address Register	0CH	40H
EPDRL	EEPROM & PHY Low Byte Data Register	0DH	Unknown
EPDRH	EEPROM & PHY High Byte Data Register	0EH	Unknown
WCR	Wake Up Control Register	0FH	00H
PAR	Physical Address Register	10H-15H	Determined by EEPROM
MAR	Multicast Address Register	16H-1DH	Unknown
GPCR	General Purpose Control Register	1EH	01H
GPR	General Purpose Register	1FH	Unknown
TWPAL	TX SRAM write pointer address low byte	20H	00H
TWPAH	TX SRAM write pointer address high byte	21H	00H
TRPAL	TX SRAM read pointer address low byte	22H	00H
TRPAH	TX SRAM read pointer address high byte	23H	00H
RWPAL	RX SRAM write pointer address low byte	24H	04H
RWPAH	RX SRAM write pointer address high byte	25H	0CH
RRPAL	RX SRAM read pointer address low byte	26H	00H
RRPAH	RX SRAM read pointer address high byte	27H	0CH
VID	Vendor ID	28H-29H	0A46H
PID	Product ID	2AH-2BH	9601H
CHIPR	CHIP revision	2CH	00H
USBDA	USB device address register	F0H	00H
RXC	Received packet counter register	F1H	00H
TXC/USBS	Transmit packet counter/USB status register	F2H	10H
USBC	USB control register	F4H	00H

Key to Default

In the register description that follows, the default column takes the form:
<Reset Value>, <Access Type>
Where：
<Reset Value>:
1 Bit set to logic one
0 Bit set to logic zero
X No default value

<Access Type>:
RO = Read only
RW = Read/Write
R/C = Read and Clear
RW/C1=Read/Write and Cleared by write 1
WO = Write only

Reserved bits are shaded and should be written with 0.
Reserved bits are undefined on read access.

10.1 Network Control Register (00H)

Bit	Name	Default	Description
7	EXT_PHY	0,RW	Select External PHY When Set When clear select Internal PHY. This bit will not be affected after a software reset
6	WAKEEN	0,RW	Wakeup Event Enable When set, it enables the wakeup function. Clearing this bit will also clear all wakeup event status. This bit will not be affected after a software reset.
5	RESERVED	0,RO	Reserved
4	FCOL	0,RW	Force Collision Mode, used for testing.
3	FDX	0,RW	Full-Duplex Mode. Read only on Internal PHY mode. R/W on External PHY mode
2:1	LBK	00,RW	Loopback Mode Bit 2 1 0 0 normal 0 1 MAC internal loopback 1 0 internal PHY digital loopback 1 1 internal PHY analog loopback
0	RST	0,RW	Software reset and auto clear after 10us

10.2 Network Status Register (01H)

Bit	Name	Default	Description
7	SPEED	X,RO	Media speed 0:100Mbps 1:10Mbps, when internal PHY is used. This bit is no meaning when LINKST=0
6	LINKST	X,RO	Link status 0:link failed 1:link OK, when internal PHY is used
5	WAKEST	0,RW/C1	Wakeup Event Status Clears by read or write 1. This bit will not be affected after a software reset
4	TXFULL	0,RO	TX FIFO Full When there are two packets in TX SRAM, TX FIFO FULL will be set
3	TX2END	0,RW/C1	TX Packet 2 Complete Status Clears by read or write 1.Transmit completion of packet index 2
2	TX1END	0,RW/C1	TX Packet 1 Complete Status Clears by read or write 1. Transmit completion of packet index 1
1	RXOV	0,RO	RX FIFO Overflow
0	RXRDY	0,RO	RX Packet Ready, there are one or more packets in RX FIFO

10.3 TX Control Register (02H)

Bit	Name	Default	Description
7	RESERVED	0,RO	Reserved
6	TJDIS	0,RW	Transmit Jabber Disable When set, the transmit Jabber Timer(2048 bytes) is disabled. Otherwise it is enabled
5	EXCECM	0,RW	Excessive Collision Mode Control 0 = abort this packet when excessive collision count more than 15 1 = still try to transmit this packet
4	PAD_DIS2	0,RW	PAD appends disable for packet index 2.
3	CRC_DIS2	0,RW	CRC appends disable for packet index 2
2	PAD_DIS1	0,RW	PAD appends disable for packet index 1
1	CRC_DIS1	0,RW	CRC appends disable for packet index 1
0	RESERVED	0,RO	Reserved

10.4 TX Status Register I (03H) for packet index I

Bit	Name	Default	Description
7	TJTO	0,RO	Transmit Jabber Time Out It is set to indicate the transmitted frame is truncated due to more than 2048 bytes are transmitted
6	LC	0,RO	Loss of Carrier It is set to indicate the loss of carrier during the frame transmission. It is not valid in internal loopback mode
5	NC	0,RO	No Carrier It is set to indicate that there is no carrier signal during the frame transmission. It is not valid in internal loopback mode
4	LC	0,RO	Late Collision It is set to indicate that a collision occurs after the collision window of 64 bytes.
3	COL	0,RO	Collision packet, collision occurs during transmission.
2	EC	0,RO	Excessive collision It is set to indicate that the transmission is aborted due to 16 excessive collisions.
1:0	RESERVED	0,RO	Reserved

10.5 TX Status Register II (04H) for packet index I I

Bit	Name	Default	Description
7	TJTO	0,RO	Transmit Jabber Time Out It is set to indicate the transmitted frame is truncated due to more than 2048 bytes are transmitted
6	LC	0,RO	Loss of Carrier It is set to indicate the loss of carrier during the frame transmission. It is not valid in internal loopback mode
5	NC	0,RO	No Carrier It is set to indicate that no carrier signal during the frame transmission. It is not valid in internal loopback mode
4	LC	0,RO	Late Collision It is set to indicate a collision occurs after the collision window of 64 bytes
3	COL	0,RO	Collision Packet Collision occurs during transmission
2	EC	0,RO	Excessive collision It is set to indicate the transmission is aborted due to 16 excessive collisions
1:0	RESERVED	0,RO	Reserved

10.6 RX Control Register (05H)

Bit	Name	Default	Description
7	RESERVED	0,RO	Reserved
6	WTDIS	0,RW	Watchdog Timer Disable When set, the Watchdog Timer (2048 bytes) is disabled. Otherwise it is enabled
5	DIS_LONG	0,RW	Discard Long Packet, packet length over 1522byte
4	DIS_CRC	0,RW	Discard CRC Error Packet
3	ALL	0,RW	Pass All Multicast
2	RUNT	0,RW	Pass Runt Packet
1	PRMSC	0,RW	Promiscuous Mode
0	RXEN	0,RW	RX Enable

10.7 RX Status Register (06H)

Bit	Name	Default	Description
7	RF	0,RO	Runt Frame It is set to indicate the received frame has the size smaller than 64 bytes.
6	MF	0,RO	Multicast Frame It is set to indicate the received frame has a multicast address.
5	LCS	0,RO	Late Collision Seen It is set to indicate that a late collision found during the frame reception.
4	RWTO	0,RO	Receive Watchdog Time-Out It is set to indicate that receive more than 2048 bytes.
3	PLE	0,RO	Physical Layer Error It is set to indicate that a physical layer error found during the frame reception.
2	AE	0,RO	Alignment Error It is set to indicate that the received frame ends with a non-byte boundary.

1	CE	0,RO	CRC Error It is set to indicate that the received frame ends with a CRC error.
0	FOE	0,RO	FIFO Overflow Error It is set to indicate that a FIFO Overflow error happens during the frame reception.

10.8 Receive Overflow Counter Register (07H)

Bit	Name	Default	Description
7	RXFU	0,R/C	Receive Overflow Counter Overflow This bit is set when the ROC has an overflow condition.
6:0	ROC	0,R/C	Receive Overflow Counter This is a statistic counter, which indicates that the received packet count upon FIFO overflow

10.9 Back Pressure Threshold Register (08H)

Bit	Name	Default	Description
7:4	BPHW	3h, RW	Back Pressure High Water Overflow Threshold MAC will generate the jam pattern when RX SRAM free space is lower than this threshold value Default is 3K-byte free space. Please don't exceed SRAM size (1 unit=1K bytes)
3:0	JPT	7h, RW	Jam Pattern Time Default is 200us bit3 bit2 bit1 bit0 time 0 0 0 0 5us 0 0 0 1 10us 0 0 1 0 15us 0 0 1 1 25us 0 1 0 0 50us 0 1 0 1 100us 0 1 1 0 150us 0 1 1 1 200us 1 0 0 0 250us 1 0 0 1 300us 1 0 1 0 350us 1 0 1 1 400us 1 1 0 0 450us 1 1 0 1 500us 1 1 1 0 550us 1 1 1 1 600us

10.10 Flow Control Threshold Register (09H)

Bit	Name	Default	Description
7:4	HWOT	3h, RW	RX FIFO High Water Overflow Threshold Send a pause packet with pause_time=FFFFH when the RX RAM free space is less than this value., If this value is zero, its meaning is no free RX SARM space. Default is 3K-byte free space. Please don't exceed SRAM size. (1 unit=1K bytes)
3:0	LWOT	8h, RW	RX FIFO Low Water Overflow Threshold Send a pause packet with pause_time=0000 when RX SARM free space is larger than this value. This pause packet is enabled after high water pause packet is transmitted. Default SRAM free space is 8K-byte. Please don't exceed SRAM size. (1 unit=1K bytes)

10.11 RX/TX Flow Control Register (0AH)

Bit	Name	Default	Description
7	TXP0	0,RW	TX pause packet, Auto clears after pause packet transmission completion. Set to TX pause packet with time = 0000H
6	TXPF	0,RW	TX pause packet, Auto clears after pause packet transmission completion. Set to TX pause packet with time = FFFFH.
5	TXPEN	0,RW	Force TX Pause Packet Enable Enable the pause packet for high/low water threshold control.
4	BKPA	0,RW	Back pressure mode. This mode is for half duplex mode only. Generates a jam pattern when any packet coming and RX SRAM over BPHW.
3	BKPM	0,RW	Back pressure mode. This mode is for half duplex mode only. Generates a jam pattern when a packet's DA match and RX SRAM over BPHW.
2	RXPS	0,R/C	RX pause packet status, latch and read clear
1	RXPCS	0,RO	RX pause packet current status
0	FLCE	0,RW	Flow Control Enable Set to enable the flow control mode(i.e. to disable TX function).

10.12 EEPROM & PHY Control Register (0BH)

Bit	Name	Default	Description
7:6	RESERVED	0,RO	Reserved
5	REEP	0,RW	Reload EEPROM. Driver needs to clear it after operation complete.
4	WEP	0,RW	Write EEPROM enable
3	EPOS	0,RW	EEPROM or PHY Operation Select When reset, select EEPROM; when set, select PHY.
2	ERPRR	0,RW	EEPROM Read or PHY Register Read Command. Driver needs to clear it after operation complete.
1	ERPRW	0,RW	EEPROM Write or PHY Register Write Command. Driver needs to clear it after operation complete.
0	ERRE	0,RO	EEPROM Access Status or PHY Access Status When set, it indicates that the EEPROM or PHY access is in progress.

10.13 EEPROM & PHY Address Register (0CH)

Bit	Name	Default	Description
7:6	PHY_ADR	1,RW	PHY Address bit 1 and 0, the PHY address bit [4:2] is force to 0. Force to 01 if internal PHY is selected
5:0	EROA	0,RW	EEPROM Word Address or PHY Register Address

10.14 EEPROM & PHY Data Register (EE_PHY_L : 0DH EE_PHY_H : 0EH)

Bit	Name	Default	Description
7:0	EE_PHY_L	X,RW	EEPROM or PHY Low Byte Data
7:0	EE_PHY_H	X,RW	EEPROM or PHY High Byte Data

10.15 Wake Up Control Register (0FH)

Bit	Name	Type	Description
7:6	RESERVED	0,RO	Reserved
5	LINKEN	0,RW	When set, enable Link Status Change Wake-up Event. This bit will not be affected after a software reset.
4	SAMPLEEN	0,RW	When set, enable Sample Frame Wake-up Event. This bit will not be affected after a software reset.
3	MAGICEN	0,RW	When set, enable Magic Packet Wake-up Event. This bit will not be affected after a software reset.
2	LINKST	0,RO	When set, indicates link change and Link Status Change Event occurred. This bit will not be affected after a software reset.
1	SAMPLEST	0,RO	When set, indicates the sample frame is received and Sample Frame Event occurred. This bit will not be affected after a software reset.
0	MAGICST	0,RO	When set, indicates the Magic Packet is received and Magic packet Event occurred. This bit will not be affected after a software reset.

10.16 Physical Address Register (10H~15H)

Bit	Name	Default	Description
7:0	PAB5	X,RW	Physical Address Byte 5 (15H)
7:0	PAB4	X,RW	Physical Address Byte 4 (14H)
7:0	PAB3	X,RW	Physical Address Byte 3 (13H)
7:0	PAB2	X,RW	Physical Address Byte 2 (12H)
7:0	PAB1	X,RW	Physical Address Byte 1 (11H)
7:0	PAB0	X,RW	Physical Address Byte 0 (10H)

10.17 Multicast Address Register (16H~1DH)

Bit	Name	Default	Description
7:0	MAB7	X,RW	Multicast Address Byte 7 (1DH)
7:0	MAB6	X,RW	Multicast Address Byte 6 (1CH)
7:0	MAB5	X,RW	Multicast Address Byte 5 (1BH)
7:0	MAB4	X,RW	Multicast Address Byte 4 (1AH)
7:0	MAB3	X,RW	Multicast Address Byte 3 (19H)
7:0	MAB2	X,RW	Multicast Address Byte 2 (18H)
7:0	MAB1	X,RW	Multicast Address Byte 1 (17H)
7:0	MAB0	X,RW	Multicast Address Byte 0 (16H)

10.18 General purpose control Register (1EH)

Bit	Name	Default	Description
7	RESERVED	0,RO	Reserved
6:0	GEP_CNTL	1,RW	General purpose control: Define the input/output direction of General Purpose Register When a bit is set 1, the direction of correspondent bit of General Purpose Register is output. GPIO0 default is output for POWER_DOWN function. Others default are input

10.19 General purpose Register (1FH)

Bit	Name	Default	Description
7	RESERVED	0,RO	Reserved
6:1	GEPIO6-1	0,RW	General Purpose When the correspondent bit of General Purpose Control Register is 1, the value of the bit is output to pin GEPIO6-1 When the correspondent bit of General Purpose Control Register is 0, the value of the bit be read is reflected from correspondent pins of GEPIIO6-1 The GEPIOs are mapped to pins GEPIO6 to GEPIO1 respectively
0	GEPIO0	1,RW	General Purpose When the correspondent bit of General Purpose Control Register is 1, the value of the bit is output to pin GEPIO0 When the correspondent bit of General Purpose Control Register is 0, the value of the bit be read is reflected from pin GEPIO0 GEPIO0 default output 1 to POWER_DOWN internal PHY. Driver need to clear this POWER_DOWN signal by write "0" when it wants PHY active. If other device need, it also can refer this signal. This default value can be programmed by EEPROM. Please refer EEPROM description

10.20 TX SRAM Write Pointer Address Register (20H~21H)

Bit	Name	Default	Description
7:0	TWPAH	00H,RO	TX SRAM write pointer address high byte (21H)
7:0	TWPAL	00H.RO	TX SRAM write pointer address low byte (20H)

10.21 TX SRAM Read Pointer Address Register (22H~23H)

Bit	Name	Default	Description
7:0	TRPAH	00H,RO	TX SRAM read pointer address high byte (23H)
7:0	TRPAL	00H.RO	TX SRAM read pointer address low byte (22H)

10.22 RX SRAM Write Pointer Address Register (24H~25H)

Bit	Name	Default	Description
7:0	RWPAH	0CH,RO	RX SRAM write pointer address high byte (25H)
7:0	RWPAL	04H.RO	RX SRAM write pointer address low byte (24H)

10.23 RX SRAM Read Pointer Address Register (26H~27H)

Bit	Name	Default	Description
7:0	RRPAH	0CH,RO	RX SRAM read pointer address high byte (27H)
7:0	RRPAL	00H.RO	RX SRAM read pointer address low byte (26H)

10.24 Vendor ID Register (28H~29H)

Bit	Name	Default	Description
7:0	VIDH	0AH,RO	Vendor ID high byte (29H)
7:0	VIDL	46H.RO	Vendor ID low byte (28H)

10.25 Product ID Register (2AH~2BH)

Bit	Name	Default	Description
7:0	PIDH	96H,R	Product ID high byte (2BH)
7:0	PIDL	01H.R	Product ID low byte (2AH)

10.26 Chip Revision Register (2CH)

Bit	Name	Default	Description
7:0	CHIPR	00H,RO	CHIP revision

10.27 USB Device Address Register (F0H)

Bit	Name	Default	Description
7	RESERVED	0,RO	Reserved
6:0	USBFA	0,RO	USB device address

10.28 Receive Packet Counter Register (F1H)

Bit	Name	Default	Description
7:0	RXC	0,RO	RXC is the packet counter received in SRAM , when greater than 255 packets, the value will keep at 255

10.29 Transmit Packet Counter/USB Status Register (F2H)

Bit	Name	Default	Description
7	RXFAULT	0,RC	Indicate RX has unexpected condition
6	SUSFLAG	0,RC	Indicate device has suspend condition
5	EP1RDY	0,RO	Indicate there are data ready for read from EP1 pipe
4:3	SRAMS	10,RO	SRAM size. 10:16KB, 00:32KB, 01:48KB, 11:64KB
2	TXC2	0,RO	Represent there are two packets in transmit buffer
1	TXC1	0,RO	Represent there is only one packet in transmit buffer
0	TXC0	0,RO	Represent there is no any packet in transmit buffer.

10.30 USB Control Register (F4H)

Bit	Name	Default	Description
7	Reserved	0,RW	Reserved
6	Reserved	0,RW	Reserved
5	EP3ACK	0,RW	When set and EP3_NAK=0, EP3 will always return 8-byte data to host per interrupt-interval
4	EP3NAK	0,RW	When set, EP3 will always return NAK.
3	Reserved	0,RW	Reserved
2	Reserved	0,RW	Reserved
1	Reserved	0,RW	Reserved
0	MEMTST	0,RW	Before any memory-command, this bit must be set to 1. When in MEM_TST, TX/RX FIFO controller will be flushed.

10.31 EEPROM Format:

name	Word	offset	description
MAC address	0	0~5	6 byte ethernet address
Auto Load Control	3	6-7	Bit 1:0=01: Update vendor ID and product ID Bit 5:2 reserved Bit 7:6=01: Accept setting of WORD7[3:0] Bit 9:8=01: Accept setting of WORD7[6:4] Bit 11:10=01: Accept setting of WORD7[7] Bit 13:12=01: Accept setting of WORD7[8] Bit 15:14=01: Accept setting of WORD11
Vendor ID	4	8-9	2 byte vendor ID (Default: 0A46h)
Product ID	5	10-11	2 byte product ID (Default: 9601h)
Reserved	6	12-13	reserved
Wake-UP mode control	7	14-15	Bit0: WOL active low when set (default: active high) Bit1: WOL is pulse mode (default: level mode) Bit2: magic wakeup event enabled when set. (default: no) Bit3: link_change wakeup event enabled when set (default: no) Bit4: magic wakeup event enabled if USB in suspend state (default: yes) Bit5: link_change wakeup event enabled if USB in suspend state (default: yes) Bit6: sample frame wakeup event enabled if USB in suspend state (default: yes) Bit7: LED mode 1 (default: 0) Bit8: internal PHY is enabled after power-on (default: no) Bit15:9: reserved
String1 address	8	16	Vendor describe string start address
String2 length	8	17	Vendor describe string length
String2 address	9	18	Product describe string start address
String2 length	9	19	Product describe string length
String3 address	10	20	Product describe string start address
String3 length	10	21	Product describe string length
USB control	11	22-23	Bit7: 0: USB maximum power. Unit is 2ma. Bit15:8: USB class code
CRC		126~127	2 byte CRC of 0~125

11. MII Register Description

ADD	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	CONTROL	Reset	Loop back	Speed select	Auto-N Enable	Power Down	Isolate	Restart Auto-N	Full Duplex	Coll. Test	Reserved						
01	STATUS	T4 Cap.	TX FDX Cap.	TX HDX Cap.	10 FDX Cap.	10 HDX Cap.	Reserved				Pream. Supr.	Auto-N Compl.	Remote Fault	Auto-N Cap.	Link Status	Jabber Detect	Extd Cap.
02	PHYID1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0
03	PHYID2	1	0	1	1	1	0	Model No.					Version No.				
04	Auto-Neg. Advertise	Next Page	FLP Rcv Ack	Remote Fault	Reserved		FC Adv	T4 Adv	TX FDX Adv	TX HDX Adv	10 FDX Adv	10 HDX Adv	Advertised Protocol Selector Field				
05	Link Part. Ability	LP Next Page	LP Ack	LP RF	Reserved		LP FC	LP T4	LP TX FDX	LP TX HDX	LP 10 FDX	LP 10 HDX	Link Partner Protocol Selector Field				
06	Auto-Neg. Expansion	Reserved											Pardet Fault	LP Next Pg Able	Next Pg Able	New Pg Rcv	LP AutoN Cap.
16	Specified Config.	BP 4B5B	BP SCR	BP ALIGN	BP_ADP OK	Rsvd	TX	Rsvd	Rsvd	Force 100LNK	Re-served		RPDCTR-EN	Reset St. Mch	Pream. Supr.	Sleep mode	Remote LoopOut
17	Specified Conf/Stat	100 FDX	100 HDX	10 FDX	10 HDX	Reserved			PHY ADDR [4:0]				Auto-N. Monitor Bit [3:0]				
18	10T Conf/Stat	Rsvd	LP Enable	HBE Enable	SQUE Enable	JAB Enable	10T Serial	Reserved									Polarity Reverse

Key to Default

In the register description that follows, the default column takes the form:
<Reset Value>, <Access Type> / <Attribute(s)>

Where：
<Reset Value>:
1 Bit set to logic one
0 Bit set to logic zero
X No default value
(PIN#) Value latched in from pin # at reset
<Access Type>:
RO = Read Only
RW = Read/Write

<Attribute (s)>:
SC = Self Clearing
P = Value Permanently Set
LL = Latching Low
LH = Latching High

11.1 Basic Mode Control Register (BMCR) - 00

Bit	Bit Name	Default	Description
0.15	Reset	0, RW/SC	Reset 1=Software reset 0=Normal operation This bit sets the status and controls the PHY registers to their default states. This bit, which is self-clearing, will keep returning a value of one until the reset process is completed
0.14	Loopback	0, RW	Loopback Loopback control register 1 = Loop-back enabled 0 = Normal operation When in 100Mbps operation mode, setting this bit may cause the descrambler to lose synchronization and produce a 720ms "dead time" before any valid data appear at the MII receive outputs
0.13	Speed selection	1, RW	Speed select 1 = 100Mbps 0 = 10Mbps Link speed may be selected either by this bit or by auto-negotiation. When auto-negotiation is enabled and bit 12 is set, this bit will return auto-negotiation selected media type
0.12	Auto-negotiation enable	1, RW	Auto-negotiation Enable 1 = Auto-negotiation is enabled, bit 8 and 13 will be in auto-negotiation status
0.11	Power down	0, RW	Power Down While in the power-down state, the PHY should respond to management transactions. During the transition to power-down state and while in the power-down state, the PHY should not generate spurious signals on the MII. 1=Power down 0=Normal operation
0.10	Isolate	0,RW	Isolate 1 = Isolates the PHY from the MII with the exception of the serial management. (When this bit is asserted, the PHY does not respond to the TXD[0:3], TX_EN, and TX_ER inputs, and it shall present a high impedance on its TX_CLK, RX_CLK, RX_DV, RX_ER, RX[0:3], COL and CRS outputs. When PHY is isolated from the MII it shall respond to the management transactions) 0 = Normal operation
0.9	Restart auto-negotiation	0,RW/SC	Restart Auto-negotiation 1 = Restart auto-negotiation. Re-initiates the auto-negotiation process. When auto-negotiation is disabled (bit 12 of this register cleared), this bit has no function and it should be cleared. This bit is self-clearing and it will keep returning a value of 1 until auto-negotiation is initiated by the PHY. The operation of the auto-negotiation process will not be affected by the management entity that clears this bit 0 = Normal operation

0.8	Duplex mode	1,RW	Duplex Mode 1 = Full duplex operation. Duplex selection is allowed when Auto-negotiation is disabled (bit 12 of this register is cleared). With auto-negotiation enabled, this bit reflects the duplex capability selected by auto-negotiation 0 = Normal operation
0.7	Collision test	0,RW	Collision Test 1 = Collision test enabled. When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN 0 = Normal operation
0.6-0.0	RESERVED	0,RO	Reserved Write as 0, ignore on read

11.2 Basic Mode Status Register (BMSR) - 01

Bit	Bit Name	Default	Description
1.15	100BASE-T4	0,RO/P	100BASE-T4 Capable 1 = Able to perform in 100BASE-T4 mode 0 = Not able to perform in 100BASE-T4 mode
1.14	100BASE-TX full duplex	1,RO/P	100BASE-TX Full Duplex Capable 1 = Able to perform 100BASE-TX in full duplex mode 0 = Not able to perform 100BASE-TX in full duplex mode
1.13	100BASE-TX half duplex	1,RO/P	100BASE-TX Half Duplex Capable 1 = Able to perform 100BASE-TX in half duplex mode 0 = Not able to perform 100BASE-TX in half duplex mode
1.12	10BASE-T full duplex	1,RO/P	10BASE-T Full Duplex Capable 1 = Able to perform 10BASE-T in full duplex mode 0 = Not able to perform 10BASE-TX in full duplex mode
1.11	10BASE-T half duplex	1,RO/P	10BASE-T Half Duplex Capable 1 = Able to perform 10BASE-T in half duplex mode 0 = Not able to perform 10BASE-T in half duplex mode
1.10-1.7	RESERVED	0,RO	Reserved Write as 0, ignore on read
1.6	MF preamble suppression	0,RO	MII Frame Preamble Suppression 1 = PHY will accept management frames with preamble suppressed 0 = PHY will not accept management frames with preamble suppressed
1.5	Auto-negotiation Complete	0,RO	Auto-negotiation Complete 1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed
1.4	Remote fault	0,RO/LH	Remote Fault 1 = Remote fault condition detected (cleared on read or by a chip reset). Fault criteria and detection method is PHY implementation specific. This bit will set after the RF bit in the ANLPAR (bit 13, register address 05) is set 0 = No remote fault condition detected
1.3	Auto-negotiation ability	1,RO/P	Auto Configuration Ability 1 = Able to perform auto-negotiation 0 = Not able to perform auto-negotiation
1.2	Link status	0,RO/LL	Link Status 1 = Valid link is established (for either 10Mbps or 100Mbps operation)

			0 = Link is not established The link status bit is implemented with a latching function, so that the occurrence of a link failure condition causes the link status bit to be cleared and remain cleared until it is read via the management interface
1.1	Jabber detect	0,RO/LH	Jabber Detect 1 = Jabber condition detected 0 = No jabber This bit is implemented with a latching function. Jabber conditions will set this bit unless it is cleared by a read to this register through a management interface or a PHY reset. This bit works only in 10Mbps mode
1.0	Extended capability	1,RO/P	Extended Capability 1 = Extended register capable 0 = Basic register capable only

11.3 PHY ID Identifier Register #1 (PHYID1) - 02

The PHY Identifier Registers #1 and #2 work together in a single identifier of the DM9601. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), a vendor's model number, and a model revision number. DAVICOM Semiconductor's IEEE assigned OUI is 00606E.

Bit	Bit Name	Default	Description
2.15-2.0	OUI_MSB	<0181h>	OUI Most Significant Bits This register stores that bit 3 to 18 of the OUI (00606E) are mapped to bit 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bit 1 and 2)

11.4 PHY Identifier Register #2 (PHYID2) - 03

Bit	Bit Name	Default	Description
3.15-3.10	OUI_LSB	<101110>, RO/P	OUI Least Significant Bits Bit 19 to 24 of the OUI (00606E) are mapped to bit 15 to 10 of this register respectively
3.9-3.4	VNDR_MDL	<001000>, RO/P	Vendor Model Number Six bits of vendor model number mapped to bit 9 to 4 (most significant bit to bit 9)
3.3-3.0	MDL_REV	<0000>, RO/P	Model Revision Number Four bits of vendor model revision number mapped to bit 3 to 0 (most significant bit to bit 3)

11.5 Auto-negotiation Advertisement Register(ANAR) – 04

This register contains the advertised abilities of this DM9601 device as they will be transmitted to its link partner during Auto-negotiation.

Bit	Bit Name	Default	Description
4.15	NP	0,RO/P	Next Page Indication 0 = No next page available 1 = Next page available The PHY has no next page, so this bit is permanently set to 0
4.14	ACK	0,RO	Acknowledge 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The PHY's auto-negotiation state machine will automatically control this bit in the outgoing FLP bursts and set it at the appropriate time during the auto-negotiation process. Software should not attempt to write to this bit
4.13	RF	0, RW	Remote Fault 1 = Local device senses a fault condition 0 = No fault detected
4.12-4.11	RESERVED	X, RW	Reserved Write as 0, ignore on read
4.10	FCS	0, RW	Flow Control Support 1 = Controller chip supports flow control ability 0 = Controller chip doesn't support flow control ability
4.9	T4	0, RO/P	100BASE-T4 Support 1 = 100BASE-T4 is supported by the local device 0 = 100BASE-T4 is not supported The PHY does not support 100BASE-T4 so this bit is permanently set to 0
4.8	TX_FDX	1, RW	100BASE-TX Full Duplex Support 1 = 100BASE-TX full duplex is supported by the local device 0 = 100BASE-TX full duplex is not supported
4.7	TX_HDX	1, RW	100BASE-TX Support 1 = 100BASE-TX is supported by the local device 0 = 100BASE-TX is not supported
4.6	10_FDX	1, RW	10BASE-T Full Duplex Support 1 = 10BASE-T full duplex is supported by the local device 0 = 10BASE-T full duplex is not supported
4.5	10_HDX	1, RW	10BASE-T Support 1 = 10BASE-T is supported by the local device 0 = 10BASE-T is not supported
4.4-4.0	Selector	<00001>, RW	Protocol Selection Bits These bits contain the binary encoded protocol selector supported by this node <00001> indicates that this device supports IEEE 802.3 CSMA/CD

11.6 Auto-negotiation Link Partner Ability Register (ANLPAR) – 05

This register contains the advertised abilities of the link partner when received during Auto-negotiation.

Bit	Bit Name	Default	Description
5.15	NP	0, RO	Next Page Indication 0 = Link partner, no next page available 1 = Link partner, next page available
5.14	ACK	0, RO	Acknowledge 1 = Link partner ability data reception acknowledged 0 = Not acknowledged The PHY's auto-negotiation state machine will automatically control this bit from the incoming FLP bursts. Software should not attempt to write to this bit
5.13	RF	0, RO	Remote Fault 1 = Remote fault indicated by link partner 0 = No remote fault indicated by link partner
5.12-5.11	RESERVED	X, RO	Reserved Write as 0, ignore on read
5.10	FCS	0, RW	Flow Control Support 1 = Controller chip supports flow control ability by link partner 0 = Controller chip doesn't support flow control ability by link partner
5.9	T4	0, RO	100BASE-T4 Support 1 = 100BASE-T4 is supported by the link partner 0 = 100BASE-T4 is not supported by the link partner
5.8	TX_FDX	0, RO	100BASE-TX Full Duplex Support 1 = 100BASE-TX full duplex is supported by the link partner 0 = 100BASE-TX full duplex is not supported by the link partner
5.7	TX_HDX	0, RO	100BASE-TX Support 1 = 100BASE-TX half duplex is supported by the link partner 0 = 100BASE-TX half duplex is not supported by the link partner
5.6	10_FDX	0, RO	10BASE-T Full Duplex Support 1 = 10BASE-T full duplex is supported by the link partner 0 = 10BASE-T full duplex is not supported by the link partner
5.5	10_HDX	0, RO	10BASE-T Support 1 = 10BASE-T half duplex is supported by the link partner 0 = 10BASE-T half duplex is not supported by the link partner
5.4-5.0	Selector	<00000>, RO	Protocol Selection Bits Link partner's binary encoded protocol selector

11.7 Auto-negotiation Expansion Register (ANER)- 06

Bit	Bit Name	Default	Description
6.15-6.5	RESERVED	X, RO	Reserved Write as 0, ignore on read
6.4	PDF	0, RO/LH	Local Device Parallel Detection Fault PDF = 1 : A fault detected via parallel detection function PDF = 0 : No fault detected via parallel detection function
6.3	LP_NP_ABLE	0, RO	Link Partner Next Page Able LP_NP_ABLE = 1 : Link partner, next page available LP_NP_ABLE = 0 : Link partner, no next page
6.2	NP_ABLE	0,RO/P	Local Device Next Page Able NP_ABLE = 1 : next page available NP_ABLE = 0 : no next page
6.1	PAGE_RX	0, RO/LH	New Page Received A new link code word page received. This bit will be automatically cleared when the register (register 6) is read by management.
6.0	LP_AN_ABLE	0, RO	Link Partner Auto-negotiation Able A “1” in this bit indicates that the link partner supports Auto-negotiation

11.8 DAVICOM Specified Configuration Register (DSCR) - 16

Bit	Bit Name	Default	Description
16.15	BP_4B5B	0, RW	Bypass 4B5B Encoding and 5B4B Decoding 1 = 4B5B encoder and 5B4B decoder function bypassed 0 = Normal 4B5B and 5B4B operation
16.14	BP_SCR	0, RW	Bypass Scrambler/Descrambler Function 1 = Scrambler and descrambler function bypassed 0 = Normal scrambler and descrambler operation
16.13	BP_ALIGN	0, RW	Bypass Symbol Alignment Function 1 = Receive functions (descrambler, symbol alignment and symbol decoding functions) bypassed. Transmit functions (symbol encoder and scrambler) bypassed 0 = Normal operation
16.12	BP_ADPOK	0, RW	BYPASS ADPOK Force signal detector (SD) active. This register is for debug only, not release to customer 1=Force SD is OK 0=Normal operation
16.11	RESERVED	0, RO	Reserved Write as 0, ignore on read
16.10	TX	1, RW	100BASE-TX or FX Mode Control 1 = 100BASE-TX operation 0 = 100BASE-FX operation
16.9	RESERVED	0, RO	Reserved
16.8	RESERVED	0, RO	Reserved Write as 0, ignore on read.
16.7	F_LINK_100	0, RW	Force Good Link in 100Mbps

			0 = Normal 100Mbps operation 1 = Force 100Mbps good link status This bit is useful for diagnostic purposes
16.6	RESERVED	0, RO	Reserved Write as 0, ignore on read
16.5	RESERVED	0, RO	Reserved Write as 0, ignore on read
16.4	RPDCTR-EN	1, RW	Reduced Power Down Control Enable This bit is used to enable automatic reduced power down 0 : Disable automatic reduced power down 1 : Enable automatic reduced power down
16.3	SMRST	0, RW	Reset State Machine When writes 1 to this bit, all state machines of PHY will be reset. This bit is self-clear after reset is completed
16.2	MFPSC	0, RW	MF Preamble Suppression Control MII frame preamble suppression control bit 1 = MF preamble suppression bit on 0 = MF preamble suppression bit off
16.1	SLEEP	0, RW	Sleep Mode Writing a 1 to this bit will cause PHY entering the Sleep mode and power down all circuit except oscillator and clock generator circuit. When waking up from Sleep mode (write this bit to 0), the configuration will go back to the state before sleep; but the state machine will be reset
16.0	RLOUT	0, RW	Remote Loopout Control When this bit is set to 1, the received data will loop out to the transmit channel. This is useful for bit error rate testing

11.9 DAVICOM Specified Configuration and Status Register (DSCSR) - 17

Bit	Bit Name	Default	Description
17.15	100FDX	1, RO	100M Full Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M full duplex mode. The software can read bit[15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode
17.14	100HDX	1, RO	100M Half Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 100M half duplex mode. The software can read bit[15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode
17.13	10FDX	1, RO	10M Full Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit. If this bit is 1, it means the operation 1 mode is a 10M Full Duplex mode. The software can read bit[15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode.
17.12	10HDX	1, RO	10M Half Duplex Operation Mode After auto-negotiation is completed, results will be written to this bit.

<table>
<tr><td></td><td></td><td></td><td>If this bit is 1, it means the operation 1 mode is a 10M half duplex mode. The software can read bit[15:12] to see which mode is selected after auto-negotiation. This bit is invalid when it is not in the auto-negotiation mode</td></tr>
<tr><td>17.11-17.9</td><td>RESERVED</td><td>0, RO</td><td>Reserved
Write as 0, ignore on read</td></tr>
<tr><td>17.8-17.4</td><td>PHYADR[4:0]</td><td>(PHYADR), RW</td><td>PHY Address Bit 4:0
The first PHY address bit transmitted or received is the MSB of the address (bit 4). A station management entity connected to multiple PHY entities must know the appropriate address of each PHY</td></tr>
<tr><td>17.3-17.0</td><td>ANMB[3:0]</td><td>0, RO</td><td>Auto-negotiation Monitor Bits
These bits are for debug only. The auto-negotiation status will be written to these bits
<table>
<tr><th>B3</th><th>b2</th><th>b1</th><th>B0</th><th></th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>In IDLE state</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Ability match</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Acknowledge match</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Acknowledge match fail</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Consistency match</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Consistency match fail</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Parallel detects signal_link_ready</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Parallel detects signal_link_ready fail</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Auto-negotiation completed successfully</td></tr>
</table></td></tr>
</table>

11.10 10BASE-T Configuration/Status (10BTCSR) - 18

Bit	Bit Name	Default	Description
18.15	RESERVED	0, RO	Reserved Write as 0, ignore on read
18.14	LP_EN	1, RW	Link Pulse Enable 1 = Transmission of link pulses enabled 0 = Link pulses disabled, good link condition forced This bit is valid only in 10Mbps operation
18.13	HBE	1,RW	Heartbeat Enable 1 = Heartbeat function enabled 0 = Heartbeat function disabled When the PHY is configured for full duplex operation, this bit will be ignored (the collision/heartbeat function is invalid in full duplex mode).
18.12	SQUELCH	1, RW	Squelch Enable 1 = normal squelch 0 = low squelch
18.11	JABEN	1, RW	Jabber Enable Enables or disables the Jabber function when the PHY is in 10BASE-T full duplex or 10BASE-T transceiver loopback mode 1 = Jabber function enabled 0 = Jabber function disabled
12. 18.10- 18.1	RESERVED	0, RO	Reserved Write as 0, ignore on read
18.0	POLR	0, RO	Polarity Reversed When this bit is set to 1, it indicates that the 10Mbps cable polarity is reversed. This bit is set and cleared by 10BASE-T module automatically

12. Functional Description

12.1 100Base-TX Operation

The block diagram in figure 3 provides an overview of the functional blocks contained in the transmit section. The transmitter section contains the following functional blocks:

- 4B5B Encoder
- Scrambler
- Parallel to Serial Converter
- NRZ to NRZI Converter
- NRZI to MLT-3
- MLT-3 Driver

12.1.1 4B5B Encoder

The 4B5B encoder converts 4-bit (4B) nibble data generated by the MAC Reconciliation Layer into a 5-bit (5B) code group for transmission, reference to Table 1. This conversion is required for control and packet data to be combined in code groups. The 4B5B encoder substitutes the first 8 bits of the MAC preamble with a J/K code-group pair (11000 10001) upon transmit. The 4B5B encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of the Transmit Enable signal from the MAC Reconciliation layer, the 4B5B encoder injects the T/R code-group pair (01101 00111) indicating end of frame. After the T/R code-group pair, the 4B5B encoder continuously injects IDLEs into the transmit data stream until Transmit Enable is asserted and the next transmit packet is detected.

The DM9601 includes a Bypass 4B5B conversion option within the 100Base-TX Transmitter for support of applications like 100 Mbps repeaters which do not require 4B5B conversion.

12.1.2 Scrambler

The scrambler is required to control the radiated emissions (EMI) by spreading the transmit energy across the frequency spectrum at the media connector and on the twisted pair cable in 100Base-TX operation.

By scrambling the data, the total energy presented to the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels on the cable could peak beyond FCC limitations at frequencies related to repeated 5B sequences like continuous transmission of IDLE symbols. The scrambler output is combined with the NRZ 5B data from the code-group encoder via an XOR logic function. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at critical frequencies.

12.1.3 Parallel to Serial Converter

The Parallel to Serial Converter receives parallel 5B scrambled data from the scrambler and serializes it (converts it from a parallel to a serial data stream). The serialized data stream is then presented to the NRZ to NRZI Encoder block

12.1.4 NRZ to NRZI Encoder

After the transmit data stream has been scrambled and serialized, the data must be NRZI encoded for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable.

12.1.5 MLT-3 Converter

The MLT-3 conversion is accomplished by converting the data stream output from the NRZI encoder into two binary data streams with alternately phased logic one events.

12.1.6 MLT-3 Driver

The two binary data streams created at the MLT-3 converter are fed to the twisted pair output driver which converts these streams to current sources and alternately drives either side of the transmit transformer's primary winding, resulting in a minimal current MLT-3 signal. Refer to figure 4 for the block diagram of the MLT-3 converter.

12.1.7 4B5B Code Group

Symbol	Meaning	4B code 3210	5B Code 43210
0	Data 0	0000	11110
1	Data 1	0001	01001
2	Data 2	0010	10100
3	Data 3	0011	10101
4	Data 4	0100	01010
5	Data 5	0101	01011
6	Data 6	0110	01110
7	Data 7	0111	01111
8	Data 8	1000	10010
9	Data 9	1001	10011
A	Data A	1010	10110
B	Data B	1011	10111
C	Data C	1100	11010
D	Data D	1101	11011
E	Data E	1110	11100
F	Data F	1111	11101
I	Idle	undefined	11111
J	SFD (1)	0101	11000
K	SFD (2)	0101	10001
T	ESD (1)	undefined	01101
R	ESD (2)	undefined	00111
H	Error	undefined	00100
V	Invalid	undefined	00000
V	Invalid	undefined	00001
V	Invalid	undefined	00010
V	Invalid	undefined	00011
V	Invalid	Undefined	00101
V	Invalid	undefined	00110
V	Invalid	undefined	01000
V	Invalid	undefined	01100
V	Invalid	undefined	10000
V	Invalid	undefined	11001

Table 1

12.2 100Base-TX Receiver

The 100Base-TX receiver contains several function blocks that convert the scrambled 125Mb/s serial data to synchronous 4-bit nibble data that is then provided to the MII.
The receive section contains the following functional blocks:

- Signal Detect
- Digital Adaptive Equalization
- MLT-3 to Binary Decoder
- Clock Recovery Module
- NRZI to NRZ Decoder
- Serial to Parallel
- Descrambler
- Code Group Alignment
- 4B5B Decoder

12.2.1 Signal Detect

The signal detect function meets the specifications mandated by the ANSI XT12 TP-PMD 100Base-TX Standards for both voltage thresholds and timing parameters.

12.2.2 Adaptive Equalization

When transmitting data at high speed over copper twisted pair cable, attenuation based on frequency becomes a concern. In high speed twisted pair signaling, the frequency content of the transmitted signal can vary greatly during normal operation based on the randomness of the scrambled data stream. This variation in signal attenuation caused by frequency variations must be compensated for to ensure the integrity of the received data. In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt various cable lengths and cable types, depend on the installed environment. The selection of long cable lengths for a given implementation, requires significant compensation which will be over-killed in a situation that includes shorter, less attenuating cable lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

12.2.3 MLT-3 to NRZI Decoder

The DM9601 decodes the MLT-3 information from the Digital Adaptive Equalizer into NRZI data. The relationship between NRZI and MLT-3 data is shown in figure 4.

12.2.4 Clock Recovery Module

The Clock Recovery Module accepts NRZI data from the MLT-3 to NRZI decoder. The Clock Recovery Module locks onto the data stream and extracts the 125Mhz reference clock. The extracted and synchronized clock and data are presented to the NRZI to NRZ Decoder.

12.2.5 NRZI to NRZ

The transmit data stream is required to be NRZI encoded in for compatibility with the TP-PMD standard for 100Base-TX transmission over Category-5 unshielded twisted pair cable. This conversion process must be reversed on the receive end. The NRZI to NRZ decoder, receives the NRZI data stream from the Clock Recovery Module and converts it to a NRZ data stream to be presented to the Serial to Parallel conversion block.

12.2.6 Serial to Parallel

The Serial to Parallel Converter receives a serial data stream from the NRZI to NRZ converter, and converts the data stream to parallel data to be presented to the descrambler.

12.2.7 Descrambler

Because of the scrambling process required to control the radiated emissions of transmit data streams, the receiver must descramble the receive data streams. The descrambler receives scrambled parallel data streams from the Serial to Parallel converter, descrambles the data streams, and presents the data streams to the Code Group alignment block.

12.2.8 Code Group Alignment

The Code Group Alignment block receives un-aligned 5B data from the descrambler and converts it into 5B code group data. Code Group Alignment occurs after the J/K is detected, and subsequent data is aligned on a fixed boundary.

12.2.9 4B5B Decoder

The 4B5B Decoder functions as a look-up table that translates incoming 5B code groups into 4B (Nibble) data. When receiving a frame, the first two 5-bit code groups received are the start-of-frame delimiter (J/K symbols). The J/K symbol pair is stripped and two nibbles of preamble pattern are substituted. The last two code groups are the end-of-frame delimiter (T/R symbols).
The T/R symbol pair is also stripped from the nibble presented to the Reconciliation layer.

12.3 10Base-T Operation

The 10Base-T transceiver is IEEE 802.3u compliant. When the DM9601 is operating in 10Base-T mode, the coding scheme is Manchester. Data processed for transmit is presented to the MII interface in nibble format, converted to a serial bit stream, then Manchester encoded. When receiving, the Manchester encoded bit stream is decoded and converted into nibble format for presentation to the MII interface.

12.4 Collision Detection

For half-duplex operation, a collision is detected when the transmit and receive channels are active simultaneously. When a collision has been detected, it will be reported by the COL signal on the MII interface. Collision detection is disabled in Full Duplex operation.

12.5 Carrier Sense

Carrier Sense (CRS) is asserted in half-duplex operation during transmission or reception of data. During full-duplex mode, CRS is asserted only during receive operations.

12.6 Auto-Negotiation

The objective of Auto-negotiation is to provide a means to exchange information between segment linked devices and to automatically configure both devices to take maximum advantage of their abilities. It is important to note that Auto-negotiation does not test the link segment characteristics. The Auto-Negotiation function provides a means for a device to advertise supported modes of operation to a remote link partner, acknowledge the receipt and understanding of common modes of operation, and to reject un-shared modes of operation. This allows devices on both ends of a segment to establish a link at the best common mode of operation. If more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function.

Auto-negotiation also provides a parallel detection function for devices that do not support the Auto-negotiation feature. During Parallel detection there is no exchange of configuration information, instead, the receive signal is examined. If it is discovered that the signal matches a technology that the receiving device supports, a connection will be automatically established using that technology. This allows devices, which do not support Auto-negotiation but support a common mode of operation, to establish a link.

12.7 Power Reduced Mode

The Signal detect circuit is always turned on to monitor the signal if there is no signal on the media (cable disconnected). The DM9601 automatically turns off the power and enters the Power Reduced mode, whether its operation mode is N-way or force mode. When enters the Power Reduced mode, the transmit circuit still sends out fast link pules with minimum power consumption. If a valid signal is detected from the media, which might be N-ways fast link pules, 10Base-T normal link pules, or 100Base-TX MLT3 signals, the device wakes up and resumes normal operation mode.

That can be writing Zero to Reg.16.4 to disable Power Reduced mode.

12.8 Power Down Mode

That can be setting Reg.0.11 high to enter the Power Down mode, which disables all transmit, receive functions and MII interface functions except the MDC/MDIO management interface.

12.9 Reduced Transmit Power Mode

Additional Transmit power reduction can be gained by designing with 1.25:1 turns ration magnetic on its TX side and using a 8.5KΩ resistor on BGRES and BGGND pins, and the TX+/TX- pull-high resistors should be changed from 50Ω to 78Ω.. This configuration could be reduced about 20% transmit power.

13. DC and AC Electrical Characteristics

13.1 Absolute Maximum Ratings (25°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVdd, AVdd	Supply Voltage	-0.3	3.6	V	
VIN	DC Input Voltage (VIN)	-0.5	5.5	V	
VOUT	DC Output Voltage(VOUT)	-0.3	3.6	V	
Tstg	Storage Temperature Rang (Tstg)	-65	+150	°C	EIAJ-4701
Tc	Case Temperature	0	85	°C	Air Flow = 0m/min
LT	Lead Temp. (TL, Soldering, 10 sec.)	---	235	°C	J-STD-020A
ESD	ESD rating (Rzap=1.5k Czap=100PF		3000	V	

13.2 Operating Conditions

Symbol	Parameter	Min.	Max.	Unit	Conditions
DVDD,AVDD	Supply Voltage	3.135	3.465	V	
PD (Power Dissipation)	100BASE-TX	---	100	mA	3.3V
	10BASE-T TX	---	80	mA	3.3V
	10BASE-T idle	---	44	mA	3.3V
	Auto-negotiation	---	60	mA	3.3V
	Power Reduced Mode(without cable)	---	20	mA	3.3V
	Power Down Mode	---	10	mA	3.3V

Comments

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

13.3 DC Electrical Characteristics (VCC = 3.3V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
TTL Inputs (TXD0~TXD3, TXCLK, MDC, MDIO, TXEN, TXER, RXEN, TESTMODE, RMII, PHYAD0~4, OPMODE0-2, RPTR, BP4B5B, RESET#)						
VIL	Input Low Voltage	---	---	0.8	V	
VIH	Input High Voltage	2.0	---	---	V	
IIL	Input Low Leakage Current	-1	---	---	uA	VIN = 0.0V
IIH	Input High Leakage Current	---	---	1	uA	VIN = 3.3V
MII TTL Outputs (RXD0-RXD3, RXDV, RXER, CRS, COL, MDIO)						
VOL	Output Low Voltage	---	---	0.4	V	IOL = 4mA
VOH	Output High Voltage	2.4	---	---	V	IOH = -4mA
Non-MII TTL Outputs (LINKLED#, SPEEDLED#, FDXLED#, MDINTR#)						
VOL	Output Low Voltage	---	---	0.4	V	IOL = 1mA
VOH	Output High Voltage	2.4	---	---	V	IOH = -0.1mA
Receiver						
VICM	RX+/RX- Common mode Input Voltage	---	1.2	---	V	100 Ω Termination Across
Transmitter						
VTD100	100TX+/- Differential Output Voltage	1.9	2.0	2.1	V	Peak to Peak
VTD10	10TX+/- Differential Output Voltage	4.4	5	5.6	V	Peak to Peak
ITD100	100TX+/- Differential Output Current	|19|	|20|	|21|	mA	
ITD10	10TX+/- Differential Output Current	|44|	|50|	|56|	mA	

13.4 USB Transceiver Interface DC Specification

Symbol	Parameter	Condition	Min	Max	Unit
VDI	Differential input Sensitivity		0.2		V
VCM	Differential common mode range		0.8	2.5	V
VIL	LOW-level input voltage			0.8	V
VIH	HIGH-level input voltage		2.0		V
VOL	LOW-level output voltage			0.3	V
VOH	HIGH-level output voltage		2.8	3.6	V

13.5 AC Electrical Characteristics & Timing Waveforms

13.5.1 TP Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tTR/F	100TX+/- Differential Rise/Fall Time	3.0	---	5.0	ns	
TTM	100TX+/- Differential Rise/Fall Time Mismatch	0	---	0.5	ns	
TTDC	100TX+/- Differential Output Duty Cycle Distortion	0	---	0.5	ns	
tT/T	100TX+/- Differential Output Peak-to-Peak Jitter	0	---	1.4	ns	
XOST	100TX+/- Differential Voltage Overshoot	0	---	5	%	

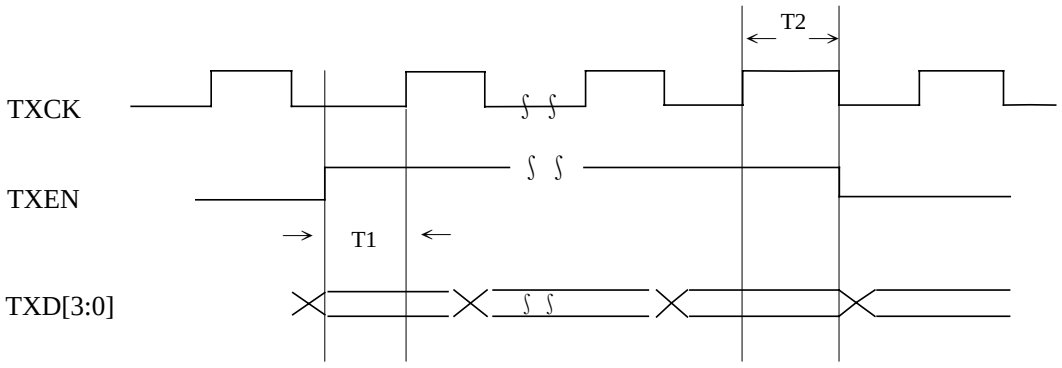
13.5.2 Oscillator/Crystal Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
TCKC	OSC Cycle Time	39.998	40	40.002	ns	50ppm
TPWH	OSC Pulse Width High	16	20	24	ns	
TPWL	OSC Pulse Width Low	16	20	24	ns	

13.5.3 USB Transceiver Interface AC Specification

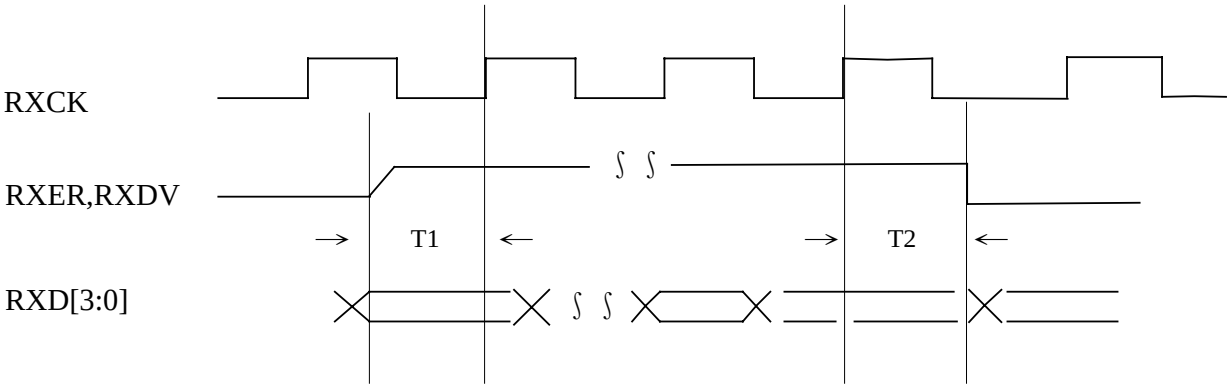
Symbol	Parameter	Condition	Min	Max	Unit
TFR	Rise time	CL=50pf	4	20	ns
TFF	Fall time	CL=50pf	4	20	ns
Tfrfm	Rise time / Fall time matching		90	111.1	%
VCRS	Output voltage cross point		1.3	2.0	V

13.5.4 External MII Interface Transmit Timing

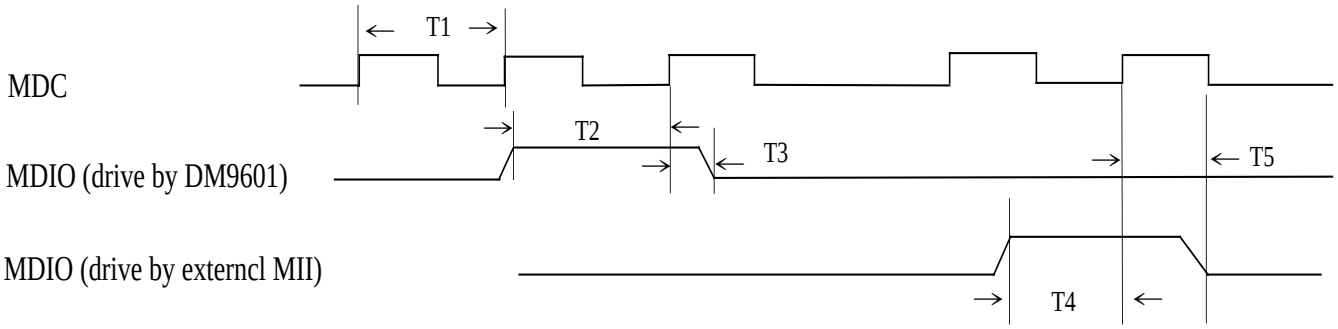


Symbol	parameter	Min.	Typ.	Max.	Unit
T1	TXEN,TXD[3：0] setup time		32		ns
T2	TXEN,TXD[3：0] hold time		32		ns

13.5.5 External MII Interface Receive Timing



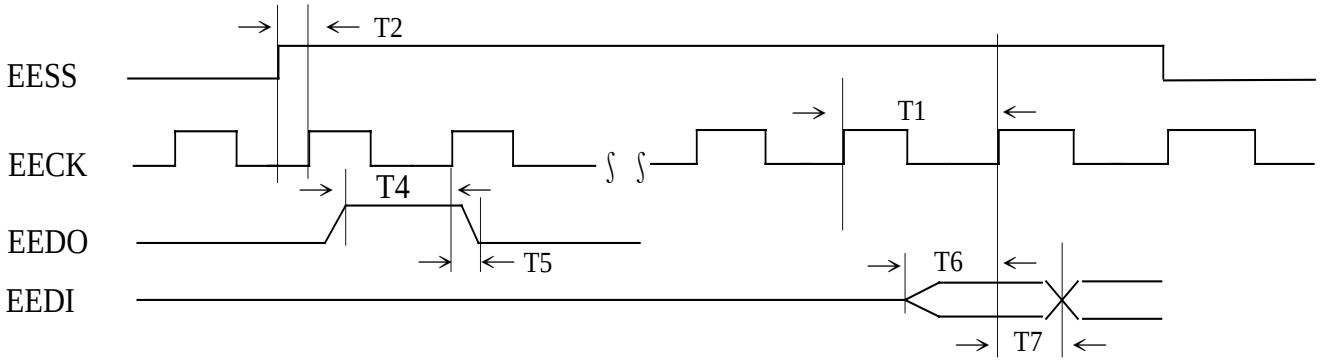
Symbol	parameter	Min.	Typ.	Max.	Unit
T1	RXER, RXDV,RXD[3：0] setup time	5			ns
T2	RXER, RXDV,RXD[3：0] hold time	5			ns



13.5.6 MII Management Interface Timing

Symbol	parameter	Min.	Typ.	Max.	Unit
T1	MDC frequency		2		MHz
T2	MDIO by DM9601 setup time		187		ns
T3	MDIO by DM9601 hold time		313		ns
T4	MDIO by external MII setup time	40			ns
T5	MDIO by external MII hold time	40			ns

13.5.7 EEPROM Interface Timing



Symbol	parameter	Min.	Typ.	Max.	Unit
T1	EECK frequency		0.375		MHz
T2	EECS setup time		500		ns
T3	EECS hold time		2166		ns
T4	EEDO setup time		480		ns
T5	EEDO hold time		2200		ns
T6	EEDI setup time	80			ns
T7	EEDI hold time	80			ns

14. Application Notes

14.1 Network Interface Signal Routing

Place the transformer as close as possible to the RJ-45 connector. Place all the 50Ω resistors as close as possible to the DM9601 RX± and TX± pins. Traces routed from RX± and TX± to the transformer should run in close pairs directly to the transformer. The designer should be careful not to place the transmit pair across the receive pair. As always, vias should be avoided as much as possible. The network interface should be void of any signal other than the TX± and RX± pairs between the RJ-45 to the transformer and the transformer to the DM9601. There should be no power or ground planes in the area under the network side of the transformer to include the area under the RJ-45 connector. (Refer to Figure 4 and 5.) Keep chassis ground away from all active signals. The RJ-45 connector and any unused pin should be tied to chassis ground through a resistor divider network and a 2KV bypass capacitor.

The Band Gap resistor should be placed as physically close to pins 25 and 26 as possible. (Refer to Figure 1 and 2.) The designer should not run any high-speed signal near the Band Gap resistor placement.

14.2 10Base-T/100Base-TX Application

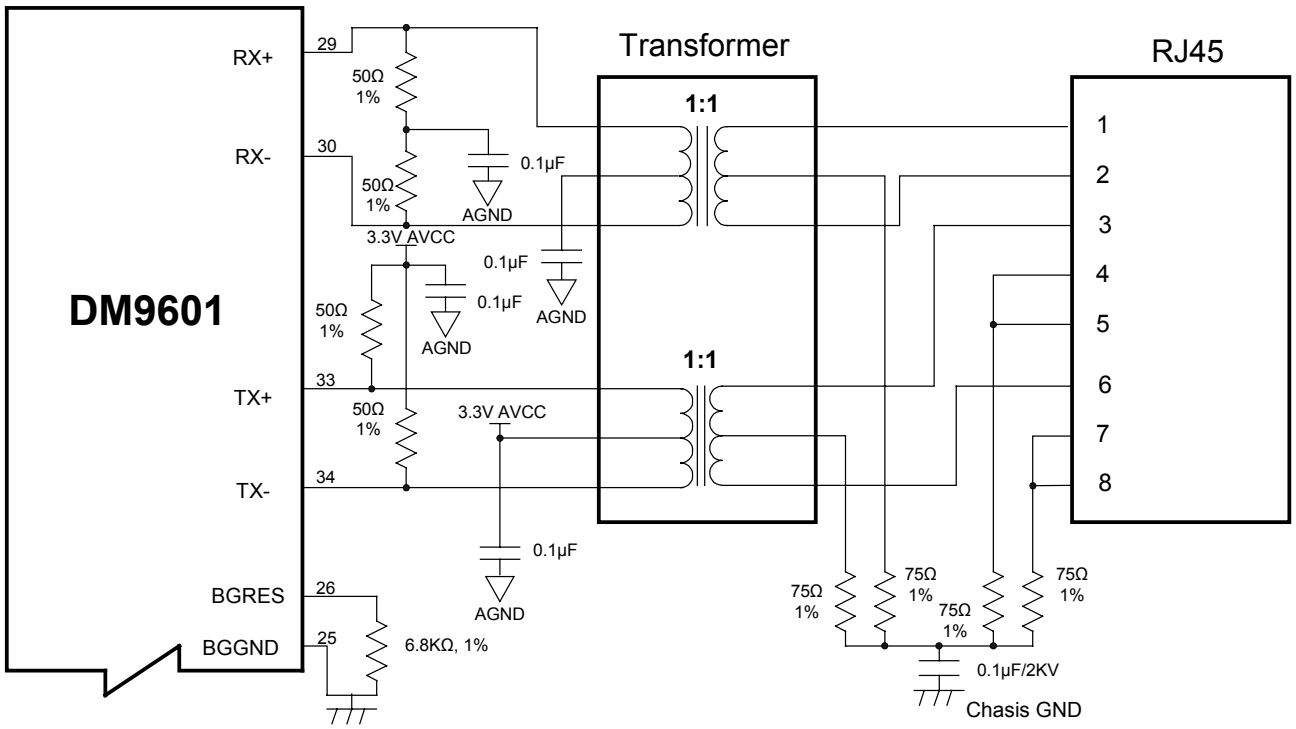


Figure 14-1

14.3 10Base-T/100Base-TX (Power Reduction Application)

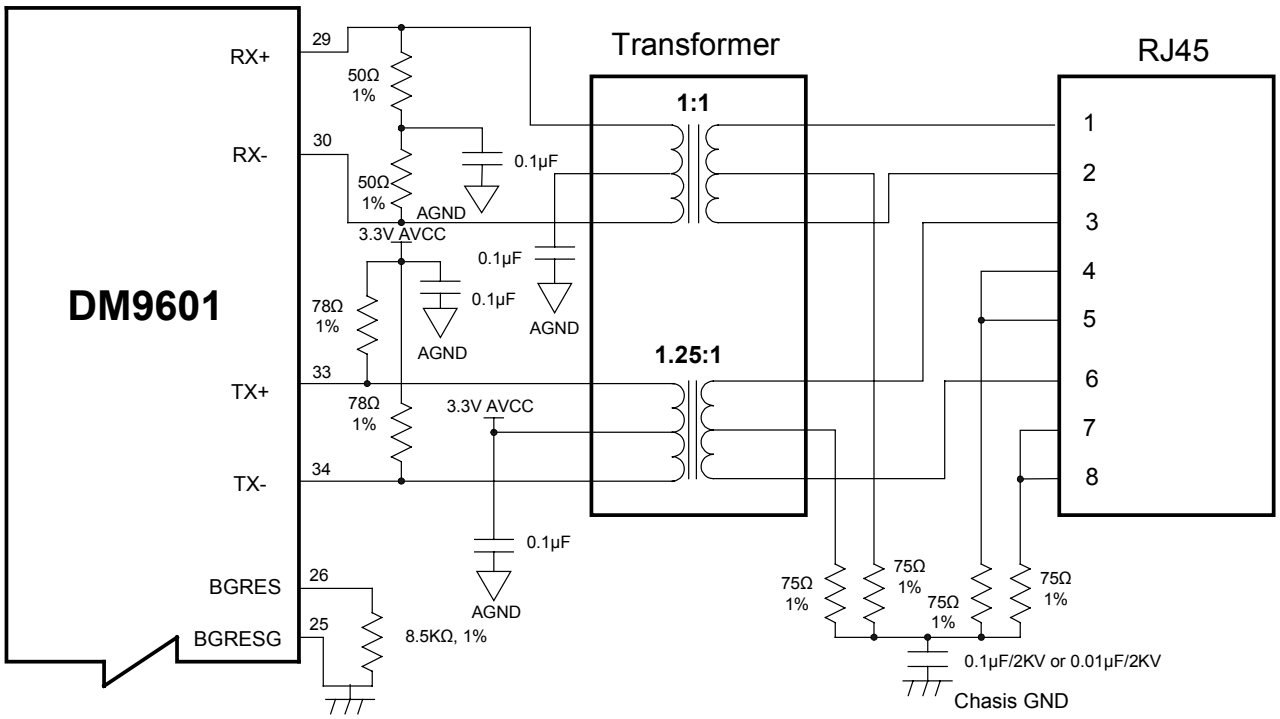


Figure 14-2

14.4 USB 1.1 Application:

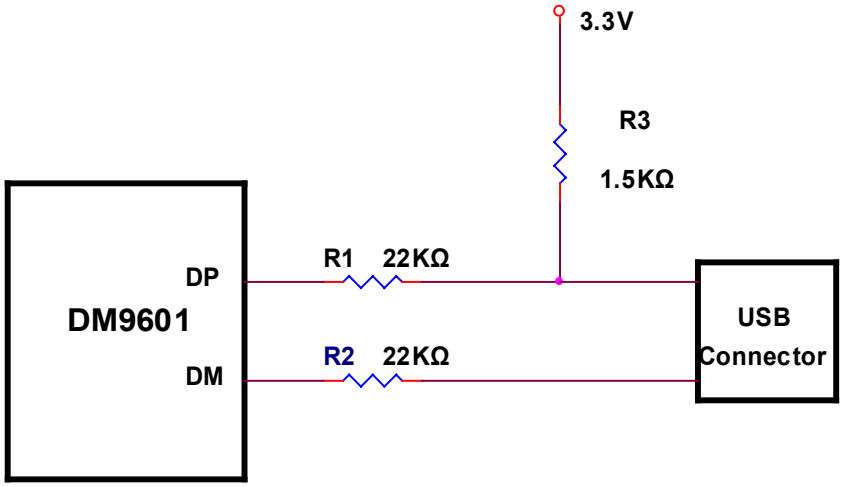


Figure 14-3

USB 1.1 Application Layout Guide:

for the USB differential signal DP/DM connecting to the USB connector:

- The traces inhibit crossover on the DP/DM Signal.
- The termination resistances should be as close as possible to the DP/DM Pins.
- The DP/DM trace should have the same length and be as short as possible.
- The DP/DM trace should be on the same plane and the width should be at least 2mm.

14.5 Power Decoupling Capacitors

Davicom Semiconductor recommends to place all the decoupling capacitors for all power supply pins as close as possible to the power pads of the DM9601 (The best placed distance is < 3mm from the above mentioned pins). The recommended decoupling capacitor is 0.1 μF or 0.01 μF, as required by the design layout.

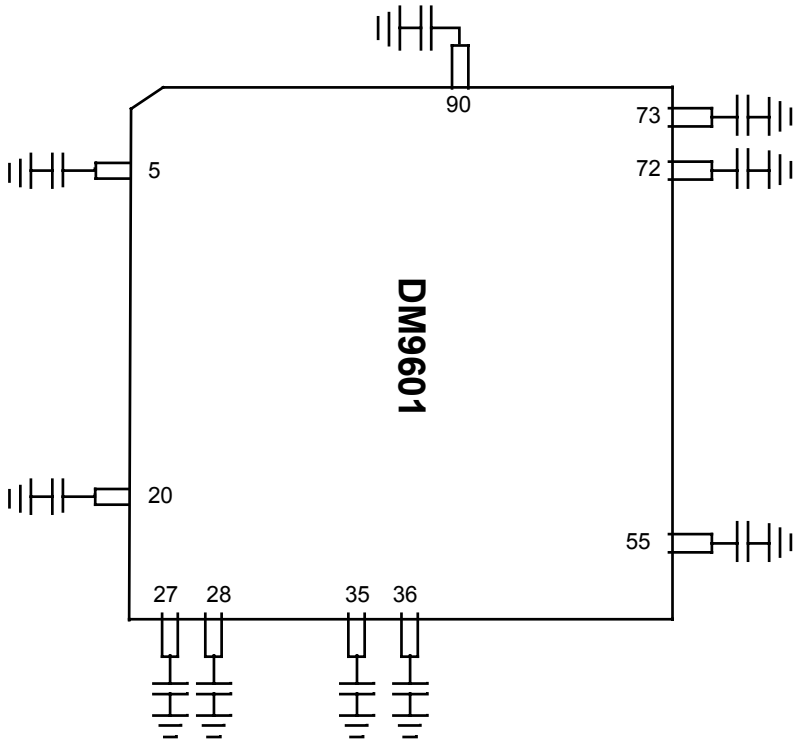


Figure 14-4

14.6 Ground Plane Layout

Davicom Semiconductor recommends a single ground plane approach to minimize EMI. Ground plane partitioning can cause increased EMI emissions that could make the network interface card not comply with specific FCC regulations (part 15). Figure 5 shows a recommended ground layout scheme.

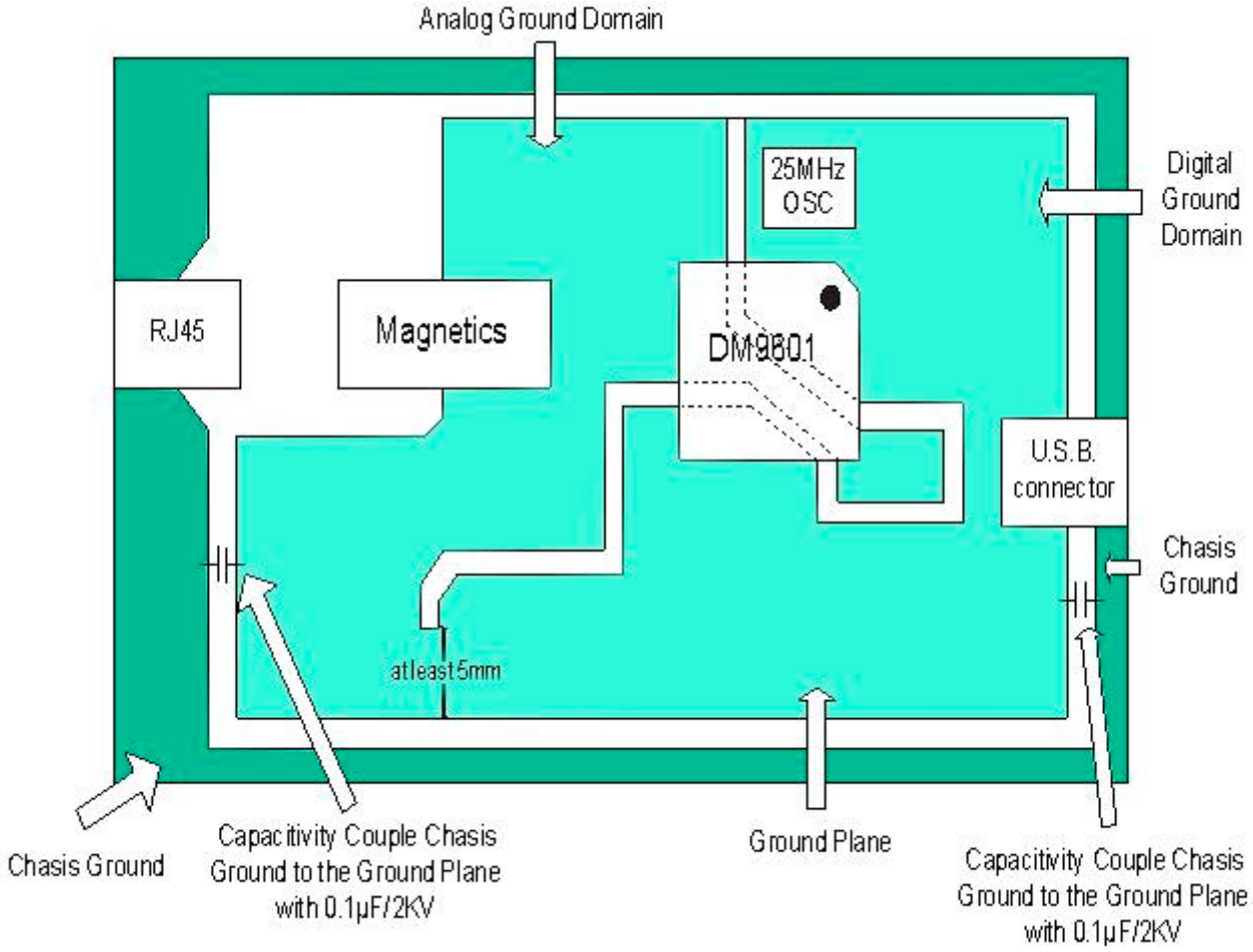


Figure 14-5

11.7 Power Plane Partitioning

The power planes should be approximately illustrated in Figure 6. The ferrite bead used should have an impedance at least 75Ω at 100MHz. A suitable bead is the Panasonic surface mound bead, part number EXCCL4532U or an equivalent. A 10μF electrolytic bypass capacitors should be connected between VCC and Ground at the device side of each of the ferrite bead.

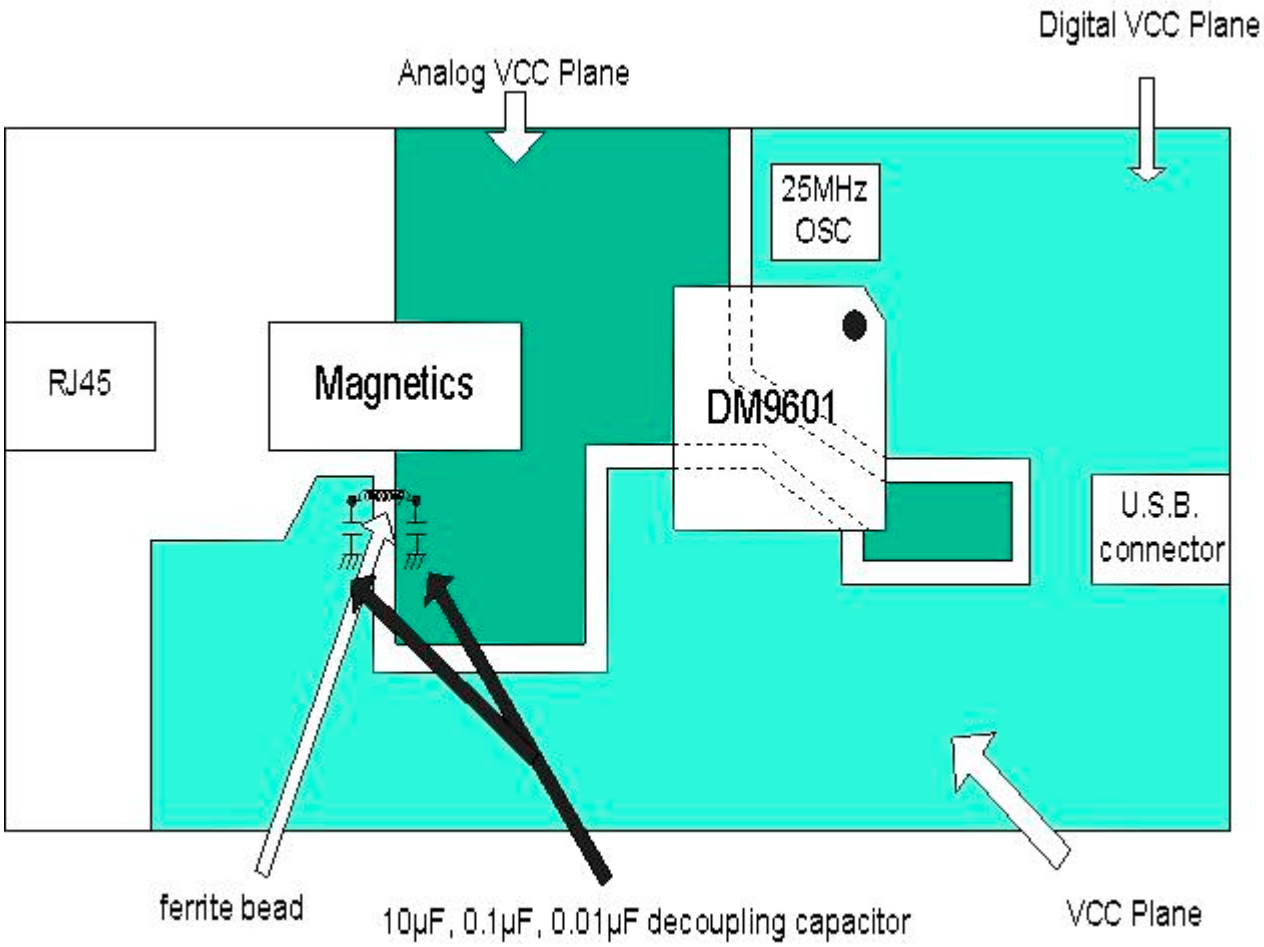


Figure 14-6

11.8 Magnetics Selection Guide

Refer to Table 2 for transformer requirements. Transformers meeting these requirements are available from a variety of magnetic manufacturers. Designers should test and qualify all magnetics before using them in an application. The transformers listed in Table 2 are electrical equivalent, but may not be pin-to-pin equivalent.

Manufacturer	Part Number
Pulse Engineering	PE-68515, H1078, H1012 H1102
Delta	LF8200, LF8221x
YCL	20PMT04, 20PMT05
Halo	TG22-3506ND, TD22-3506G1, TG22-S010ND TG22-S012ND
Nano Pulse Inc.	NPI 6181-37, NPI 6120-30, NPI 6120-37 NPI 6170-30
Fil-Mag	PT41715
Bel Fuse	S558-5999-01
Valor	ST6114, ST6118
Macronics	HS2123, HS2213

Table 2

11.9 Crystal Selection Guide

A crystal can be used to generate the 25Mhz reference clock instead of a oscillator. The crystal must be a fundamental type, series-resonant. Connect to X1 and X2, shunt each crystal lead to ground with a 22pf capacitor (see figure 7).

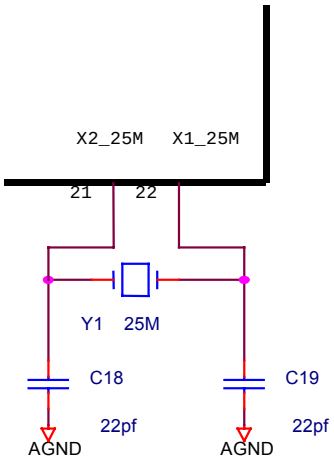
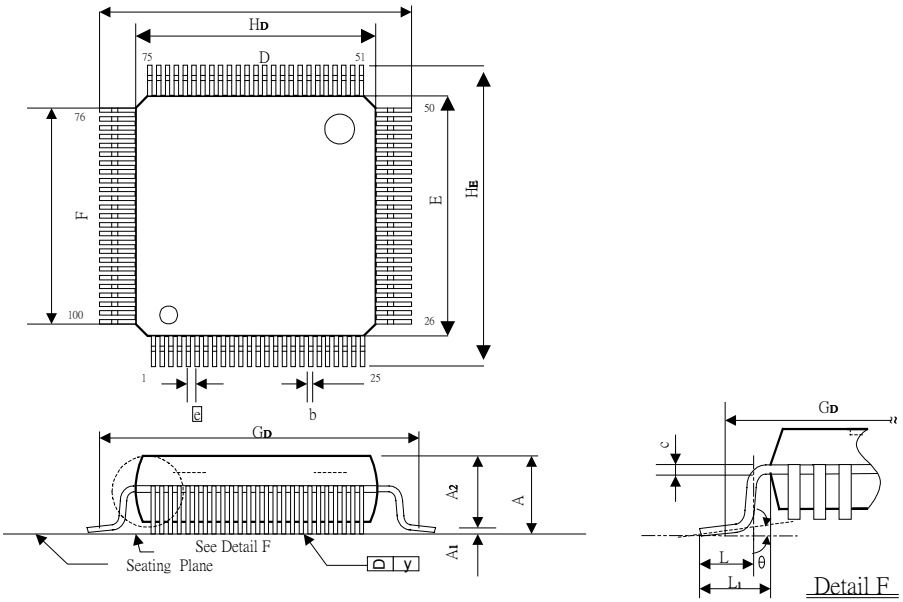


Figure 14-7
Crystal Circuit Diagram

15. Package Information

15.1 LQFP 100L Outline Dimensions

Unit: Inches/mm



Symbol	Dimensions In Inches	Dimensions In mm
A	0.063 Max.	1.60 Max.
A1	0.004 ± 0.002	0.1 ± 0.05
A2	0.055 ± 0.002	1.40 ± 0.05
b	0.009 ± 0.002	0.22 ± 0.05
c	0.006 ± 0.002	0.15 ± 0.05
D	0.551 ± 0.005	14.00 ± 0.13
E	0.551 ± 0.005	14.00 ± 0.13
e	0.020 BSC.	0.50 BSC.
F	0.481 NOM.	12.22 NOM.
GD	0.606 NOM.	15.40 NOM.
HD	0.630 ± 0.006	16.00 ± 0.15
HE	0.630 ± 0.006	16.00 ± 0.15
L	0.024 ± 0.006	0.60 ± 0.15
L_1	0.039 Ref.	1.00 Ref.
y	0.004 Max.	0.1 Max.
θ	0° ~ 12°	0° ~ 12°

Notes:

1. Dimension D & E do not include resin fins.
2. Dimension GD is for PC Board surface mount pad pitch design reference only.
3. All dimensions are based on metric system.

16. Ordering Information

Part Number	Pin Count	Package
DM9601E	100	LQFP

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WARNING
Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and/or function.

Data Sheet Changed Errata List

05/02/2001 P01 DM9601 Data Sheet start

05/31/2001 P01 Modify Page 1 Block Diagram

06/22/2001 P01 Page 20

Before Modification:

4	BKPM	0,RW	Back pressure mode. This mode is for half duplex mode only. Generate a jam pattern when a packet's DA match and RX SRAM over BPHW.
3	BKPA	0,RW	Back pressure mode. This mode is for half duplex mode only. Generate a jam pattern when any packet coming and RX SRAM over BPHW.

After modification:

4	BKPA	0,RW	Back pressure mode. This mode is for half duplex mode only. Generate a jam pattern when any packet coming and RX SRAM over BPHW.
3	BKPM	0,RW	Back pressure mode. This mode is for half duplex mode only. Generate a jam pattern when a packet's DA match and RX SRAM over BPHW.