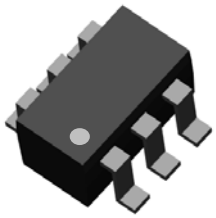
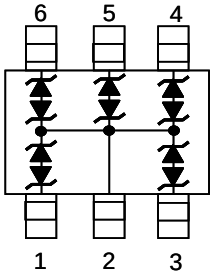
DRAFT SPEC

FIVE BI-DIRECTIONAL TVS ARRAY FOR ESD PROTECTION

This Penta TVS Array has been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry operating at 5Vdc and below. This TVS array offers an integrated solution to protect up to 5 data lines where the board space is a premium.





SOT23-6L

Marking Code

SPECIFICATION FEATURES

- **80W Power Dissipation (8/20µs Waveform)**
- **Low Leakage Current, Maximum of 1µA @ 5Vdc**
- **Very low Clamping voltage**
- **IEC61000-4-2 ESD 15kV air, 8kV Contact Compliance**
- **Industry standard SOT23-6L**
- **100% Tin Matte Finish (RoHS Compliant)**

APPLICATIONS

- **Video I/O ports protection**
- **Set Top Boxes**
- **Portable Instrumentation**

MAXIMUM RATINGS

Rating	Symbol	Value	Units
Peak Pulse Power (8/20µs Waveform)	P_{pp}	80	W
Peak Pulse Current (8/20µs Waveform)	I_{pp}	5.0	A
ESD Voltage (HBM)	V_{ESD}	>25	kV
Operating Temperature Range	T_J	-55 to +150	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

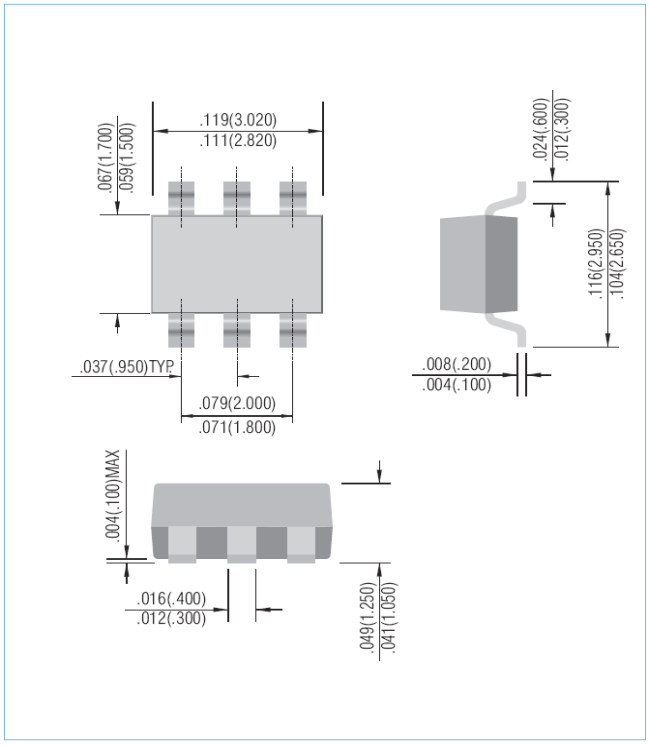
ELECTRICAL CHARACTERISTICS Tj = 25°C

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				5.0	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1mA	6.2		8.0	V
Reverse Leakage Current	I_R	V_R =5V			1	µA
Clamping Voltage (8/20µs)	V_c	I_{pp} = 1A			12	V
Clamping Voltage (8/20µs)	V_c	I_{pp} = 4A			15	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 2			15	pF
Off State Junction Capacitance	Cj	5 Vdc Bias f = 1MHz Between I/O pins and pin 2			7	pF

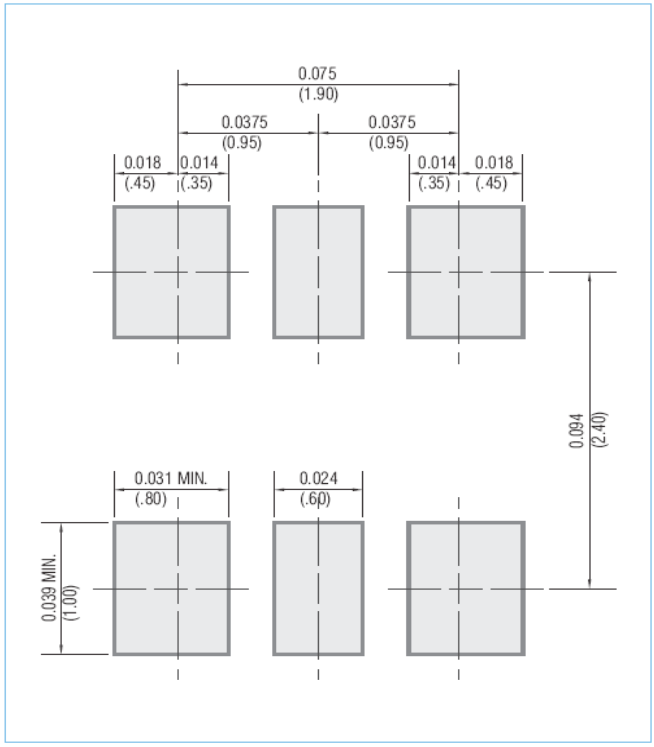
DRAFT SPEC

PACKAGE LAYOUT DIMENSIONS

SOT-23-6L Unit: inch (mm)



SOT23-6L Unit: inch (mm)



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