INTERNATIONAL RECTIFIER IOR

2N681 & 2N5204 SERIES

25 and 35 Amp RMS SCRs

Major Ratings and Characteristics

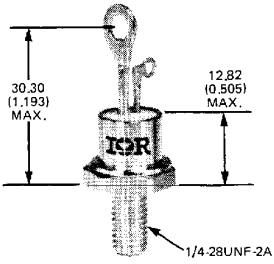
	2N681-92	2N5204-07	Units
$I_{T(RMS)}$	25	35	A
$I_{T(AV)}$	16*	22*	A
@ T_C	-65 to 65*	-40 to 40	°C
I_{TSM}			
@ 50 Hz	145	285	A
@ 60 Hz	150*	300*	
I^2t			
@ 50 Hz	103	410	A^2s
@ 60 Hz	94	375	
I_{GT}	40	40	mA
dv/dt	–	100*	V/μs
di/dt	75–100	100	A/μs
T_J	-65 to 125*	-40 to 125*	°C
V_{RRM}, V_{DRM} range	25–800	600–1200	V

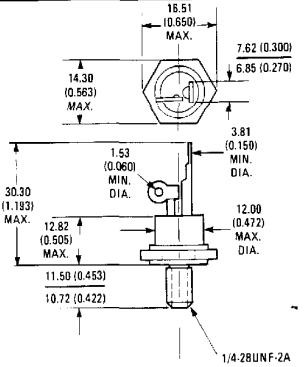
*JEDEC registered value.

Description/Features

- General purpose stud mounted
- Broad forward and reverse voltage range – through 1200 volts
- Can be supplied to meet stringent military, aerospace and other high-reliability requirements

CASE STYLE AND DIMENSIONS





Conforms to JEDEC Outline TO-208AA (TO-48)
Dimensions in Millimeters and (Inches)

VOLTAGE RATINGS (Applied gate voltage zero or negative)

Part Numbers	V_{RRM}, V_{DRM} – Max. Repetitive Peak Reverse and Off-State Voltage (V)	V_{RSM} Max. Non Repetitive Peak Reverse Voltage $t_p < 5$ ms (V)
	T_J = -65°C to 125°C	T_J = -65°C to 125°C
2N681	25*	35*
2N682	50*	75*
2N683	100*	150*
2N685	200*	300*
2N687	300*	400*
2N688	400*	500*
2N689	500*	600*
2N690	600*	720*
2N691	700*	840*
2N692	800*	960*
	T_J = -40°C to 125°C	T_J = -40°C to 125°C
2N5204	600	720
2N5205	800	960
2N5206	1000	1200
2N5207	1200	1440

ELECTRICAL SPECIFICATIONS

		2N681-92	2N5204-07	Units	Conditions
	ON-STATE				
$I_{T(RMS)}$	Max. RMS on-state current	25	35	A	
$I_{T(AV)}$	Max. average on-state current	16*	22*	A	180° half sine wave conduction
	@ T_C =	-65 to 65*	-40 to 40*	°C	
I_{TSM}	Max. peak one cycle, non-repetitive surge current	145	285	A	50 Hz half cycle sine wave or 6 ms rectangular pulse — Following any rated load condition, and with rated V_{RRM} applied following surge.
		150*	300*		60 Hz half cycle sine wave or 5 ms rectangular pulse
		170	340		50 Hz half cycle sine wave or 6 ms rectangular pulse — Same conditions as above except with V_{RRM} applied following surge = 0.
		180	355		60 Hz half cycle sine wave or 5 ms rectangular pulse
I^2t	Max. I^2t capability, for fusing	103	410	A^2s	t = 10 ms — Rated V_{RRM} applied following surge, initial T_J = 125°C
		94	375		t = 8.3 ms
I^2t	Max. I^2t capability, for individual device fusing	145	580	A^2s	t = 10 ms — V_{RRM} = 0 following surge, initial T_J = 125°C.
		135	530		t = 8.3 ms
$I^2\sqrt{t}$	Max. $I^2\sqrt{t}$ capability, for individual device fusing ①	1450	5800	$A^2\sqrt{s}$	t = 0.1 to 10ms initial $T_J \leq 125°C$ V_{RRM} following surge = 0.
V_{TM}	Max. peak on-state voltage	2*	2.3*	V	T_J = 25°C, $I_{T(AV)}$ = 16A (50A peak) 2N681, $I_{T(AV)}$ = 22A (70A peak) 2N5204
I_H	Max. holding current	20 @ 25°C†	200* @ -40°C	mA	Anode supply = 24V, initial I_T = 1.0A.
	BLOCKING				
dv/dt	Min. critical rate-of-rise of off-state voltage	100†	100*	V/μs	T_J = 125°C. Exponential to 100% rated V_{DRM} — Gate open circuited.
		250†	250		T_J = 125°C. Exponential to 67% rated V_{DRM}

*JEDEC Registered value.

① I^2t for time $t_x = I^2\sqrt{t} \cdot \sqrt{t_x}$.

† *Typical*

ELECTRICAL SPECIFICATIONS (Continued)

		2N681-92	2N5204-07	Units	Conditions
	BLOCKING (Continued)				
$I_{R(-)}$ & $I_{D(-)}$	Max. reverse and off-state current	$I_{R(AV)}$ & $I_{D(AV)}$ (Average Values)	I_{RM} & I_{DM} (Peak Values)		
	V_{RRM} & V_{DRM} = 5V				
	25 to 150V	6.5*	–		
	200 & 250V	6.0*	–		
	300V	5.0*	–		
	400V	4.0*	–	mA	T_J = 125°C, gate open circuited.
	500V	3.0*	–		
	600V	2.5*	3.3*		
	700V	2.25*	–		
	800V	2.0*	2.5*		
	1000V	–	2.0*		
	1200V	–	1.7*		
	SWITCHING				
t_d	Typical delay time	1	1	μs	T_C = 25°C, V_{DM} = rated V_{DRM}, I_{TM} = 10A dc *resistive circuit. Gate pulse: 10V, 40Ω source,* t_p = 6 μs, t_r = 0.1 μs.
di/dt	Max. non-repetitive rate of rise of turned-on current				T_C = 125°C, V_{DM} = rated V_{DRM}, I_{TM} = 2 x di/dt, Gate pulse: 20V, 15Ω, t_p = 6 μs, t_r = 0.1 μs max. Per JEDEC standard RS-397, 5.2.2.6.
	V_{DM} = 25 to 600V	100	–	A/μs	
	= 700 to 800V	75	–		
		–	100		T_C = 125°C, V_{DM} = 600V, I_{TM} = 200A @ 400 Hz, max., Gate pulse: 20V, 15Ω, t_p = 6 μs, t_r = 0.1 μs max. Per JEDEC standard RS-397, 5.2.2.6.
	TRIGGERING				
P_{GM}	Max. peak gate power	5*	60*	W	t_p ≤ 5 ms for 2N681 series; t_p ≤ 500 μs for 2N5204 series..
$P_{G(AV)}$	Max. average gate power	0.5*	0.5*	W	
$+I_{GM}$	Max. peak positive gate current	2*	2	A	
$+V_{GM}$	Max. peak positive gate voltage	10*	–	V	
$-V_{GM}$	Max. peak negative gate voltage	5*	5*	V	
I_{GT}	Max. required DC gate current to trigger	80*	80*		T_C = min. rated value. Max. required gate trigger current is the lowest value which will trigger all units with +6V anode-to-cathode.
		40	40		T_C = 25°C
		18.5	20	mA	T_C = 125°C
	Typical DC gate current to trigger	30	30		T_C = 25°C +6V anode-to-cathode
V_{GT}	Max. required DC gate voltage to trigger	3*	3*		T_C = -65°C. Max. required gate trigger voltage is *the lowest value which will trigger all units with* +6V anode-to-cathode.
		2	2	V	T_C = 25°C
	Typical DC gate voltage to trigger	1.5	1.5		T_C = 25°C +6V anode-to-cathode
V_{GD}	Max. DC gate voltage not to trigger	0.25*	0.25*	V	T_C = 125°C. Max. gate voltage not to trigger is the maximum value which will not trigger any unit with rated V_{DRM} anode-to-cathode.

THERMAL-MECHANICAL SPECIFICATIONS

		2N681-92	2N5204-07	Units	Conditions
T_J	Operating junction temperature range	-65° to 125°	-40° to 125°	°C	
T_{stg}	Storage temperature range	-65° to 125°	-40° to 125°	°C	
R_{thJC}	Max. internal thermal resistance, junction to case	1.5	1.5*	deg. C/W	DC operation
R_{thCS}	Thermal resistance, case to sink	0.35	0.35	deg. C/W	Mounting surface smooth, flat and greased.
	Mounting torque to nut ±10%	20.(27.5)		lbf · in.	Lubricated threads (non-lubricated threads).
		0.23(.32)		kgf · m	
		2.3(3.1)		N·m	
	to device	25		lbf · in.	Lubricated threads.
		0.29		kgf · m	
		2.8		N·m	
wt	Approximate weight	14(0.49)	14 (0.5)	g (oz.)	
	Case Style	TO-208AA (TO-48)			

*JEDEC Registered value.

2N681 Series

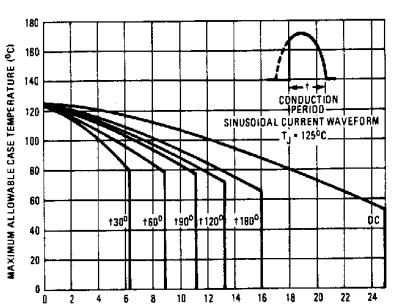


Fig. 1 – Maximum Allowable Case Temperature Vs. Average On-State Current, 2N681 Series

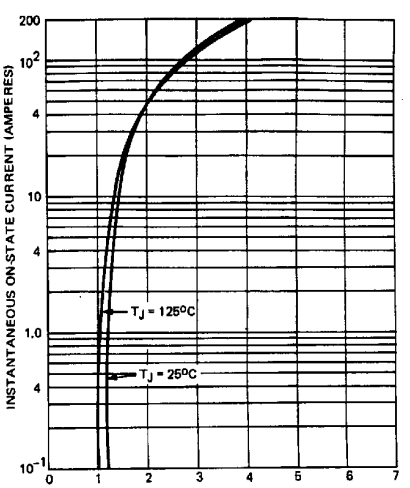


Fig. 2 – Maximum On-State Voltage Vs. Current, 2N681 Series

2N681 Series

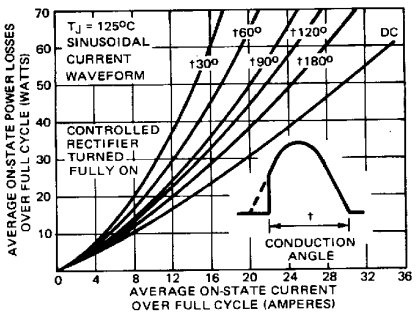


Fig. 3 – Maximum Low Level On-State Power Loss Vs. Current (Sinusoidal Current Waveform), 2N681 Series

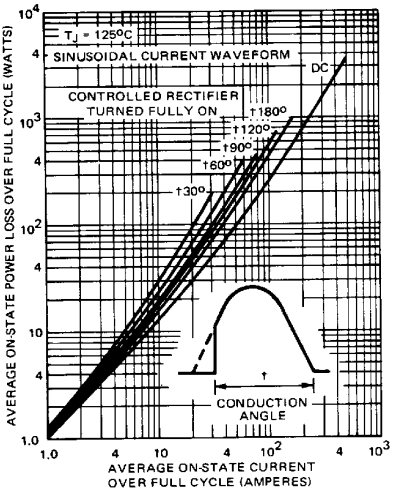


Fig. 4 – Maximum High Level On-State Power Loss Vs. Current (Sinusoidal Current Waveform), 2N681 Series

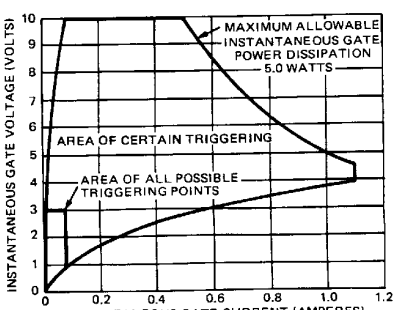


Fig. 5 – Gate Characteristics, 2N681 Series

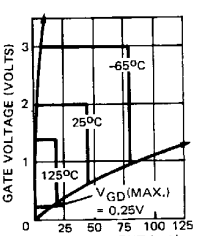


Fig. 5A – Area of All Possible Triggering Points Vs. Temperature 2N681 Series

2N681 Series

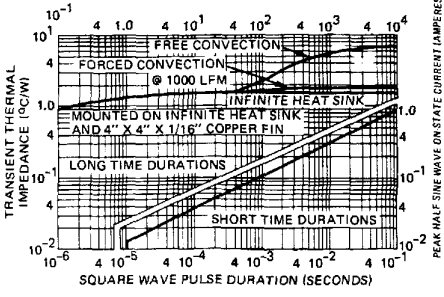


Fig. 6 – Maximum Transient Thermal Impedance, Junction to Case, Vs. Pulse Duration, 2N681 Series

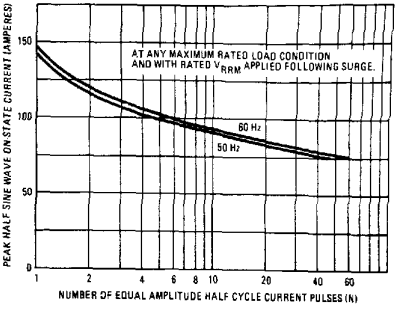


Fig. 7 – Maximum Non-Repetitive Surge Current, Vs. Number of Current Pulses, 2N681 Series

2N5204 Series

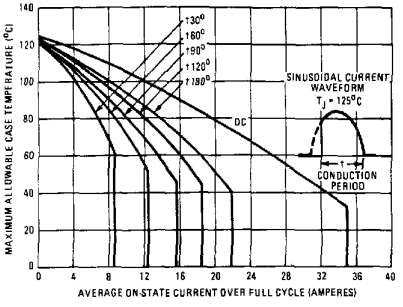


Fig. 8 – Maximum Allowable Case Temperature Vs. Average On-State Current (Sinusoidal Current Waveform), 2N5204 Series

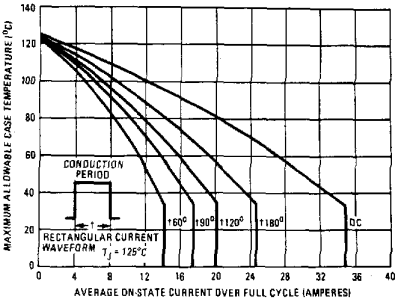


Fig. 9 – Maximum Allowable Case Temperature Vs. Average On-State Current (Rectangular Current Waveform), 2N5204 Series

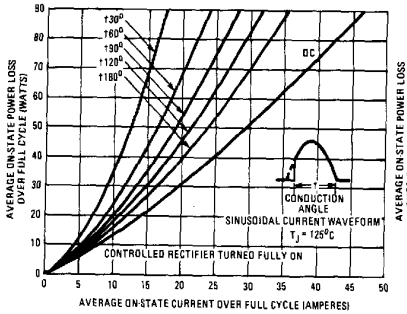


Fig. 10 – Maximum Low-Level On-State Power Loss Vs. Average On-State Current (Sinusoidal Current Waveform), 2N5204 Series

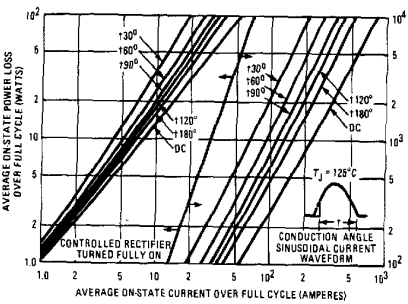


Fig. 11 – Maximum High-Level On-State Power Loss Vs. Average On-State Current (Sinusoidal Current Waveform), 2N5204 Series

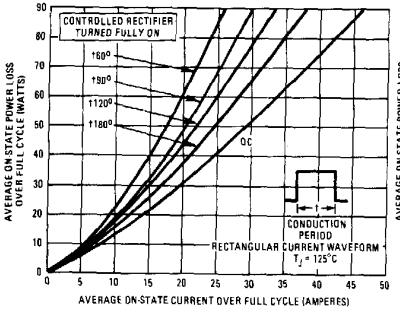


Fig. 12 – Maximum Low-Level On-State Power Loss Vs. Average On-State Current (Rectangular Current Waveform), 2N5204 Series

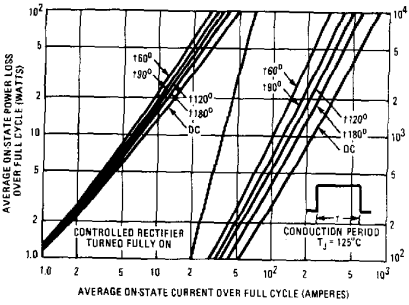


Fig. 13 – Maximum High-Level On-State Power Loss Vs. Average On-State Current (Rectangular Current Waveform), 2N5204 Series

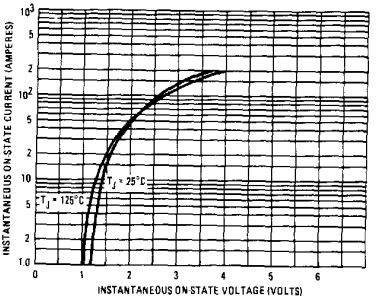


Fig. 14 – Maximum Instantaneous On-State Voltage Vs. Instantaneous On-State Current, 2N5204 Series

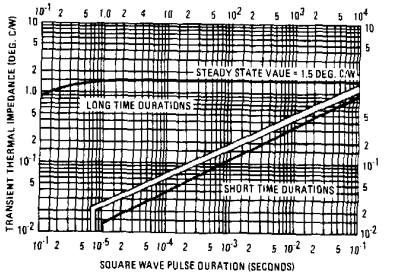


Fig. 15 – Maximum Transient Thermal Resistance, Junction to Case, Vs. Pulse Duration, 2N5204 Series