SONY

# CXD3504R

## Selective Delay Line for LCD

### Description

The CXD3504R is a selective delay line IC for performing signal processing during dot and line inverted drive of liquid crystal panels for Sony projectors.

This chip has three built-in 10-bit × 1200-word 1H delay lines, and data path with or without a 1H delay can be selected by the control pins.

### Features

- Supports dot and line inverted drive of liquid crystal panels for Sony projectors
- Three built-in 10-bit × 1200-word 1H delay lines
- Data path with or without a 1H delay can be selected by the control pins.

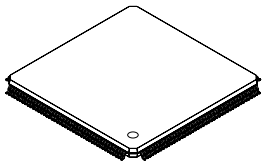
### Applications

LCD projectors, etc.

### Structure

Silicon gate CMOS IC

176 pin LQFP (Plastic)



### Absolute Maximum Ratings (Vss = 0V)

| | | | |
|---|---|---|---|
| • Supply voltage | $V_{DD}$ | –0.3 to +4.6 | V |
| • Input voltage | $V_I$ | –0.3 to $V_{DD}$ + 0.3 | V |
| • Output voltage | $V_O$ | –0.3 to $V_{DD}$ + 0.3 | V |
| • Operating temperature | Topr | –30 to +75 | °C |
| • Storage temperature | Tstg | –55 to +125 | °C |
| • Allowable power dissipation | | | |
| | $P_D$max | 850mW (Ta ≤ 75°C) | |

### Recommended Operating Conditions

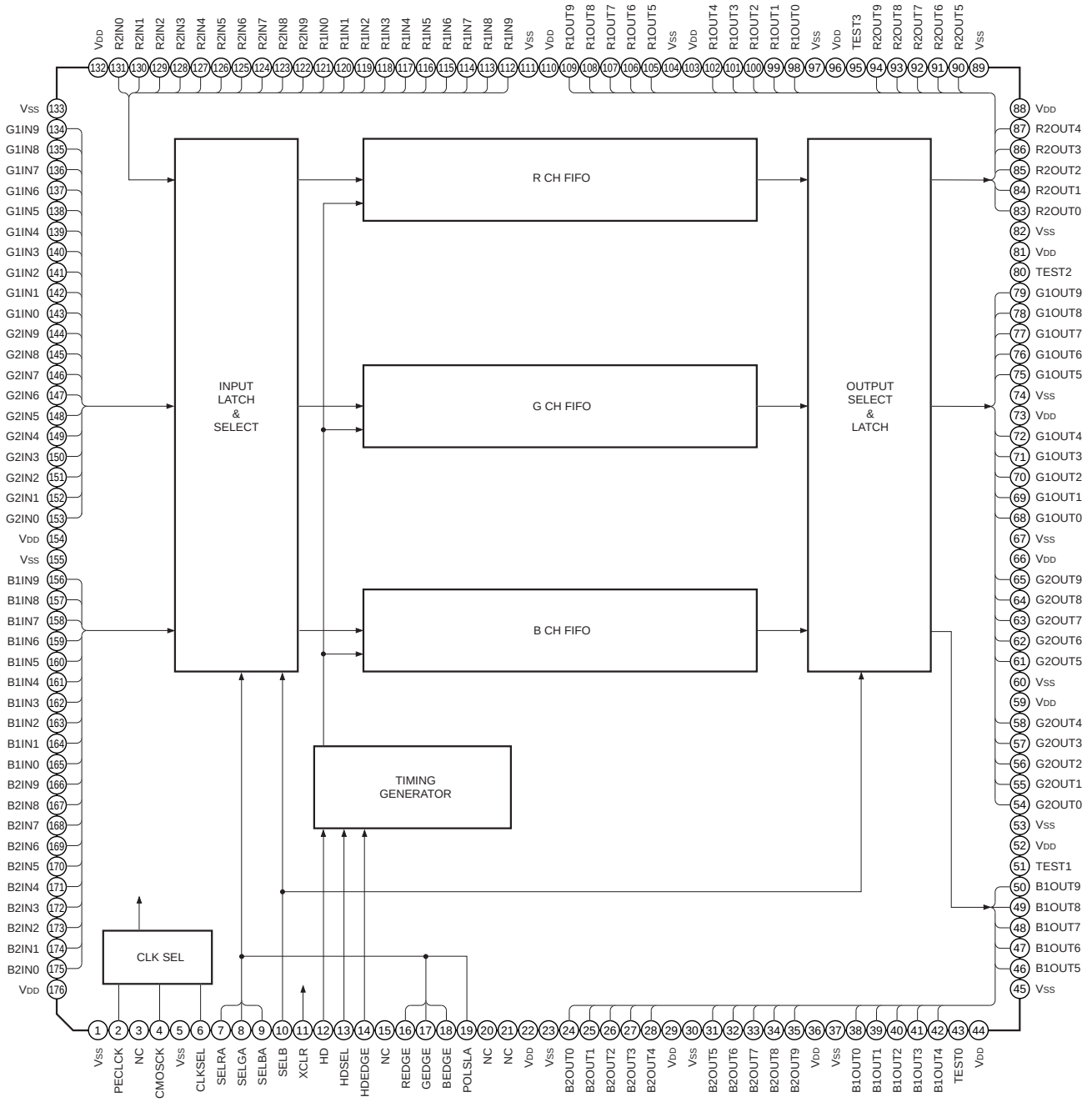
| | | | |
|---|---|---|---|
| • Supply voltage | $V_{DD}$ | 3.0 to 3.6 | V |
| • Operating temperature | Topr | –30 to +75 | °C |
| • Input voltage | $V_{IN}$ | 0 to $V_{DD}$ | V |

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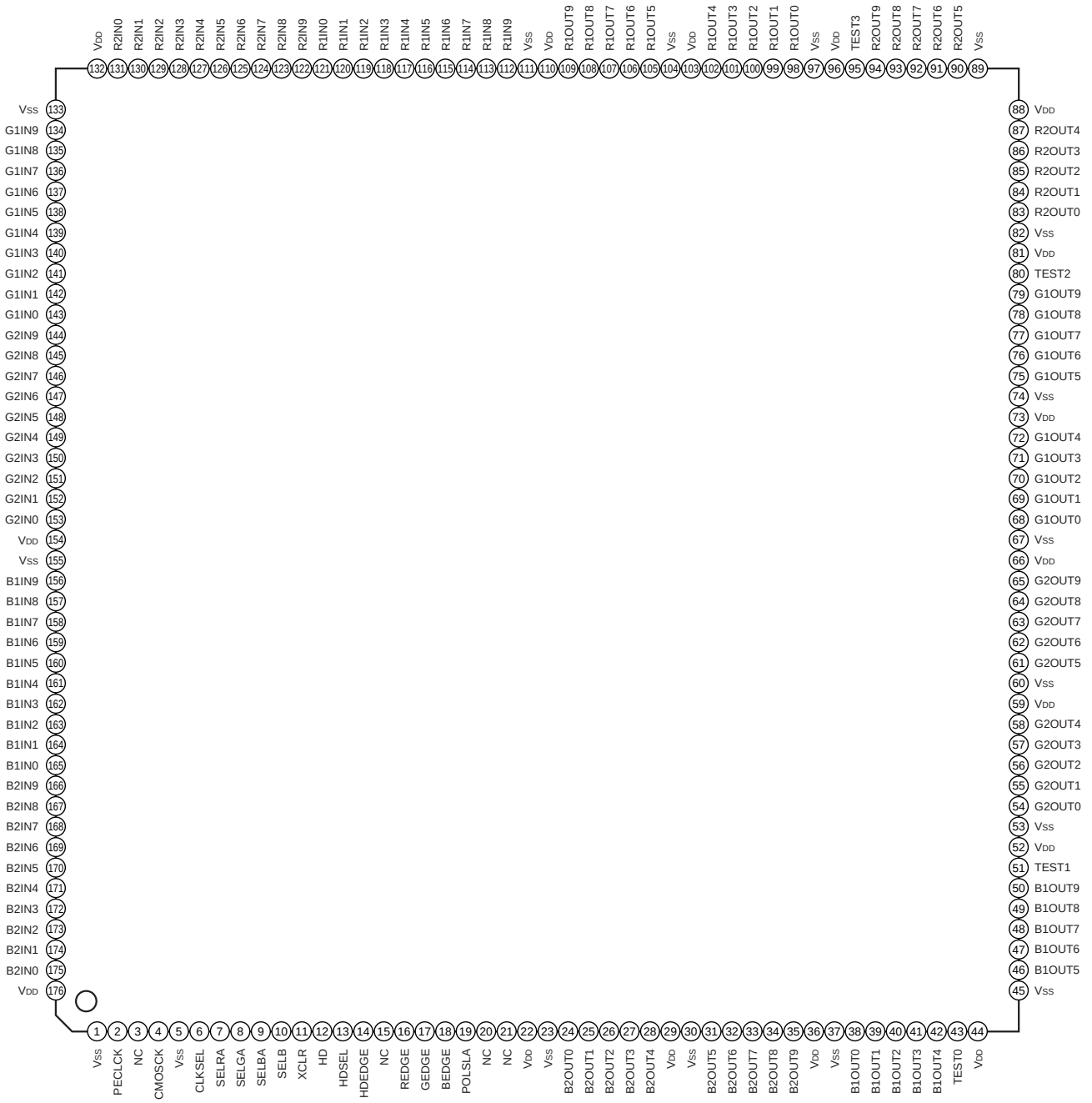


E99815-PS

## Block Diagram



## Pin Configuration



**Pin Description**

| Pin No. | Symbol | I/O | Description | Input pin for open status |
|---|---|---|---|---|
| 1 | $V_{SS}$ | P | GND | |
| 2 | PECLCK | I | Very little amp. clock input*1 | |
| 3 | NC | | | |
| 4 | CMOSCK | I | CMOS clock input*2 | |
| 5 | $V_{SS}$ | P | GND | |
| 6 | CLKSEL | I | 0: PECL, 1: CMOS | L |
| 7 | SELRA | I | SELA (Data path selection A) for R | L |
| 8 | SELGA | I | SELA (Data path selection A) for G | L |
| 9 | SELBA | I | SELA (Data path selection A) for B | L |
| 10 | SELB | I | Data path selection B | L |
| 11 | XCLR | I | 0: Direct Reset | H |
| 12 | HD | I | Horizontal sync signal input | |
| 13 | HDSEL | I | HD selection (0: ↓, 1: ↑) | L |
| 14 | HDEDGE | I | CK trigger selection of HD (0: ↓, 1: ↑) | L |
| 15 | NC | | Reserve | |
| 16 | REDGE | I | CK trigger selection of R (0: ↓, 1: ↑) | L |
| 17 | GEDGE | I | CK trigger selection of G (0: ↓, 1: ↑) | L |
| 18 | BEDGE | I | CK trigger selection of B (0: ↓, 1: ↑) | L |
| 19 | POLSLA | I | SELA polarity selection | L |
| 20 | NC | | | |
| 21 | NC | | | |
| 22 | $V_{DD}$ | P | Power supply | |
| 23 | $V_{SS}$ | P | GND | |
| 24 | B2OUT0 | O | B2 output | |
| 25 | B2OUT1 | O | B2 output | |
| 26 | B2OUT2 | O | B2 output | |
| 27 | B2OUT3 | O | B2 output | |
| 28 | B2OUT4 | O | B2 output | |
| 29 | $V_{DD}$ | P | Power Supply | |
| 30 | $V_{SS}$ | P | GND | |
| 31 | B2OUT5 | O | B2 output | |
| 32 | B2OUT6 | O | B2 output | |
| 33 | B2OUT7 | O | B2 output | |

*1 Connect to GND or $V_{DD}$ when using CMOS clock.

*2 Connect to GND or $V_{DD}$ when using small amplitude clock.

| Pin No. | Symbol | I/O | Description | Input pin for open status |
|---|---|---|---|---|
| 34 | B2OUT8 | O | B2 output | |
| 35 | B2OUT9 | O | B2 output | |
| 36 | $V_{DD}$ | P | Power supply | |
| 37 | $V_{SS}$ | P | GND | |
| 38 | B1OUT0 | O | B1 output | |
| 39 | B1OUT1 | O | B1 output | |
| 40 | B1OUT2 | O | B1 output | |
| 41 | B1OUT3 | O | B1 output | |
| 42 | B1OUT4 | O | B1 output | |
| 43 | TEST0 | I | 1: Test mode | L |
| 44 | $V_{DD}$ | P | Power supply | |
| 45 | $V_{SS}$ | P | GND | |
| 46 | B1OUT5 | O | B1 output | |
| 47 | B1OUT6 | O | B1 output | |
| 48 | B1OUT7 | O | B1 output | |
| 49 | B1OUT8 | O | B1 output | |
| 50 | B1OUT9 | O | B1 output | |
| 51 | TEST1 | I | 1: Test mode | L |
| 52 | $V_{DD}$ | P | Power supply | |
| 53 | $V_{SS}$ | P | GND | |
| 54 | G2OUT0 | O | G2 output | |
| 55 | G2OUT1 | O | G2 output | |
| 56 | G2OUT2 | O | G2 output | |
| 57 | G2OUT3 | O | G2 output | |
| 58 | G2OUT4 | O | G2 output | |
| 59 | $V_{DD}$ | P | Power supply | |
| 60 | $V_{SS}$ | P | GND | |
| 61 | G2OUT5 | O | G2 output | |
| 62 | G2OUT6 | O | G2 output | |
| 63 | G2OUT7 | O | G2 output | |
| 64 | G2OUT8 | O | G2 output | |
| 65 | G2OUT9 | O | G2 output | |
| 66 | $V_{DD}$ | P | Power supply | |
| 67 | $V_{SS}$ | P | GND | |
| 68 | G1OUT0 | O | G1 output | |

| Pin No. | Symbol | I/O | Description | Input pin for open status |
|---|---|---|---|---|
| 69 | G1OUT1 | O | G1 output | |
| 70 | G1OUT2 | O | G1 output | |
| 71 | G1OUT3 | O | G1 output | |
| 72 | G1OUT4 | O | G1 output | |
| 73 | $V_{DD}$ | P | Power supply | |
| 74 | $V_{SS}$ | P | GND | |
| 75 | G1OUT5 | O | G1 output | |
| 76 | G1OUT6 | O | G1 output | |
| 77 | G1OUT7 | O | G1 output | |
| 78 | G1OUT8 | O | G1 output | |
| 79 | G1OUT9 | O | G1 output | |
| 80 | TEST2 | I | 1: Test mode | L |
| 81 | $V_{DD}$ | P | Power supply | |
| 82 | $V_{SS}$ | P | GND | |
| 83 | R2OUT0 | O | R2 output | |
| 84 | R2OUT1 | O | R2 output | |
| 85 | R2OUT2 | O | R2 output | |
| 86 | R2OUT3 | O | R2 output | |
| 87 | R2OUT4 | O | R2 output | |
| 88 | $V_{DD}$ | P | Power supply | |
| 89 | $V_{SS}$ | P | GND | |
| 90 | R2OUT5 | O | R2 output | |
| 91 | R2OUT6 | O | R2 output | |
| 92 | R2OUT7 | O | R2 output | |
| 93 | R2OUT8 | O | R2 output | |
| 94 | R2OUT9 | O | R2 output | |
| 95 | TEST3 | I | 1: Test mode | L |
| 96 | $V_{DD}$ | P | Power supply | |
| 97 | $V_{SS}$ | P | GND | |
| 98 | R1OUT0 | O | R1 output | |
| 99 | R1OUT1 | O | R1 output | |
| 100 | R1OUT2 | O | R1 output | |
| 101 | R1OUT3 | O | R1 output | |
| 102 | R1OUT4 | O | R1 output | |
| 103 | $V_{DD}$ | P | Power supply | |
| 104 | $V_{SS}$ | P | GND | |

| Pin No. | Symbol | I/O | Description | Input pin for open status |
|---|---|---|---|---|
| 105 | R1OUT5 | O | R1 output | |
| 106 | R1OUT6 | O | R1 output | |
| 107 | R1OUT7 | O | R1 output | |
| 108 | R1OUT8 | O | R1 output | |
| 109 | R1OUT9 | O | R1 output | |
| 110 | $V_{DD}$ | P | Power supply | |
| 111 | $V_{SS}$ | P | GND | |
| 112 | R1IN9 | I | R1 input | |
| 113 | R1IN8 | I | R1 input | |
| 114 | R1IN7 | I | R1 input | |
| 115 | R1IN6 | I | R1 input | |
| 116 | R1IN5 | I | R1 input | |
| 117 | R1IN4 | I | R1 input | |
| 118 | R1IN3 | I | R1 input | |
| 119 | R1IN2 | I | R1 input | |
| 120 | R1IN1 | I | R1 input | |
| 121 | R1IN0 | I | R1 input | |
| 122 | R2IN9 | I | R2 input | |
| 123 | R2IN8 | I | R2 input | |
| 124 | R2IN7 | I | R2 input | |
| 125 | R2IN6 | I | R2 input | |
| 126 | R2IN5 | I | R2 input | |
| 127 | R2IN4 | I | R2 input | |
| 128 | R2IN3 | I | R2 input | |
| 129 | R2IN2 | I | R2 input | |
| 130 | R2IN1 | I | R2 input | |
| 131 | R2IN0 | I | R2 input | |
| 132 | $V_{DD}$ | P | Power supply | |
| 133 | $V_{SS}$ | P | GND | |
| 134 | G1IN9 | I | G1 input | |
| 135 | G1IN8 | I | G1 input | |
| 136 | G1IN7 | I | G1 input | |
| 137 | G1IN6 | I | G1 input | |
| 138 | G1IN5 | I | G1 input | |
| 139 | G1IN4 | I | G1 input | |
| 140 | G1IN3 | I | G1 input | |

| Pin No. | Symbol | I/O | Description | Input pin for open status |
|---|---|---|---|---|
| 141 | G1IN2 | I | G1 input | |
| 142 | G1IN1 | I | G1 input | |
| 143 | G1IN0 | I | G1 input | |
| 144 | G2IN9 | I | G2 input | |
| 145 | G2IN8 | I | G2 input | |
| 146 | G2IN7 | I | G2 input | |
| 147 | G2IN6 | I | G2 input | |
| 148 | G2IN5 | I | G2 input | |
| 149 | G2IN4 | I | G2 input | |
| 150 | G2IN3 | I | G2 input | |
| 151 | G2IN2 | I | G2 input | |
| 152 | G2IN1 | I | G2 input | |
| 153 | G2IN0 | I | G2 input | |
| 154 | $V_{DD}$ | P | Power supply | |
| 155 | $V_{SS}$ | P | GND | |
| 156 | B1IN9 | I | B1 input | |
| 157 | B1IN8 | I | B1 input | |
| 158 | B1IN7 | I | B1 input | |
| 159 | B1IN6 | I | B1 input | |
| 160 | B1IN5 | I | B1 input | |
| 161 | B1IN4 | I | B1 input | |
| 162 | B1IN3 | I | B1 input | |
| 163 | B1IN2 | I | B1 input | |
| 164 | B1IN1 | I | B1 input | |
| 165 | B1IN0 | I | B1 input | |
| 166 | B2IN9 | I | B2 input | |
| 167 | B2IN8 | I | B2 input | |
| 168 | B2IN7 | I | B2 input | |
| 169 | B2IN6 | I | B2 input | |
| 170 | B2IN5 | I | B2 input | |
| 171 | B2IN4 | I | B2 input | |
| 172 | B2IN3 | I | B2 input | |
| 173 | B2IN2 | I | B2 input | |
| 174 | B2IN1 | I | B2 input | |
| 175 | B2IN0 | I | B2 input | |
| 176 | $V_{DD}$ | P | Power supply | |

**Electrical Characteristics** (Input/Output level/$V_{DD}$ = 3.0 to 3.6V, Vss = 0V, Ta = –30 to +75°C)

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit | Applicable pins |
|---|---|---|---|---|---|---|---|
| High level input voltage | $V_{IH}$ | CMOS input | 0.7$V_{DD}$ | — | — | V | *1, *2, *3 |
| Low level input voltage | $V_{IL}$ | | — | — | 0.2$V_{DD}$ | V | |
| High level output voltage | $V_{OH}$ | $I_{OH}$ = –12mA | $V_{DD}$ – 0.8 | — | — | V | *4 |
| Low level output voltage | $V_{OL}$ | $I_{OL}$ = 12mA | — | — | 0.4 | V | |
| Input leak current | $I_{IL}$ | $V_I$ = $V_{SS}$, $V_{DD}$ | –10 | — | 10 | µA | *1, *2, *3 |
| Pull-up resistor | $R_{UP}$ | | 80 | 160 | 320 | kΩ | *2 |
| Pull-down resistor | $R_{DN}$ | | 90 | 180 | 360 | kΩ | *3 |

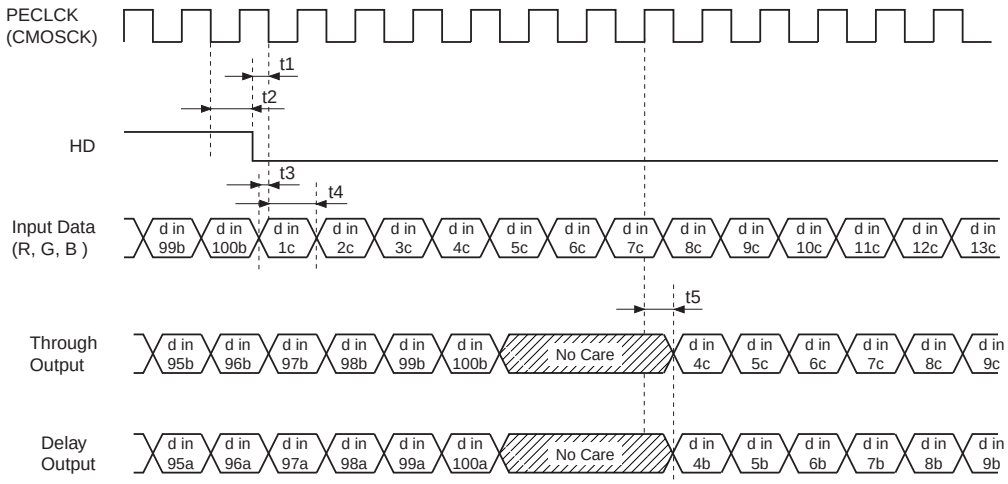
*1 Input pins except PECLCK

*2 XCLR

*3 CLKSEL, SELRA, SELGA, SELBA, SELB, HDSEL, HDEDGE, REDGE, GEDGE, BEDGE, POLSLA

*4 All output pins

**AC Characteristics**




| Item | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Input frequency | f | — | 80 | MHz |
| HD set-up time to PECLCK bar | t1 | 1.5 | — | ns |
| HD hold time from PECLCK bar | t2 | 4.5 | — | ns |
| R, G, B input data set-up time to PECLCK bar | t3 | 1 | — | ns |
| R, G, B input data hold time from PECLCK bar | t4 | 6.5 | — | ns |
| R, G, B output data delay from PECLCK | t5 | 4 | 13 | ns |
| HD set-up time to CMOSCK bar | t1 | 2 | — | ns |
| HD hold time from CMOSCK bar | t2 | 3 | — | ns |
| R, G, B input data set-up time to CMOSCK bar | t3 | 1.5 | — | ns |
| R, G, B input data hold time from CMOSCK bar | t4 | 4.5 | — | ns |
| R, G, B output data delay from CMOSCK | t5 | 3 | 12 | ns |

**Note:** The above timing values are for PECCLK (CMOSCK) = 80MHz and an output pin capacitance of 20pF.

**Description of Operation**

1) The following describes only R, but the operation for G and B is the same.

| | | | | | |
|---|---|---|---|---|---|
| SELRA:SELB = 0:0 | R2IN | → | through | → | R1OUT |
| | R1IN | → | delay | → | R2OUT |
| SELRA:SELB = 0:1 | R2IN | → | delay | → | R1OUT |
| | R1IN | → | through | → | R2OUT |
| SELRA:SELB = 1:0 | R1IN | → | through | → | R1OUT |
| | R2IN | → | delay | → | R2OUT |
| SELRA:SELB = 1:1 | R1IN | → | delay | → | R1OUT |
| | R2IN | → | through | → | R2OUT |

However, POLSLA = 0

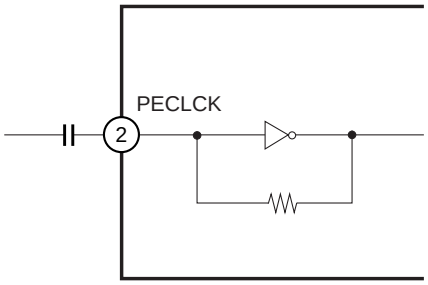
2) Be sure to set XCLR to "0" for a clock or more while HD is "1". (when HDSEL = 0) Also, input the HD signal with a "0" period length of 6 clocks or more.

**Very Little Signal Amplifier** ($V_{DD}$ = 3.0 to 3.6V, Vss = 0V, Ta = –30 to +75°C)

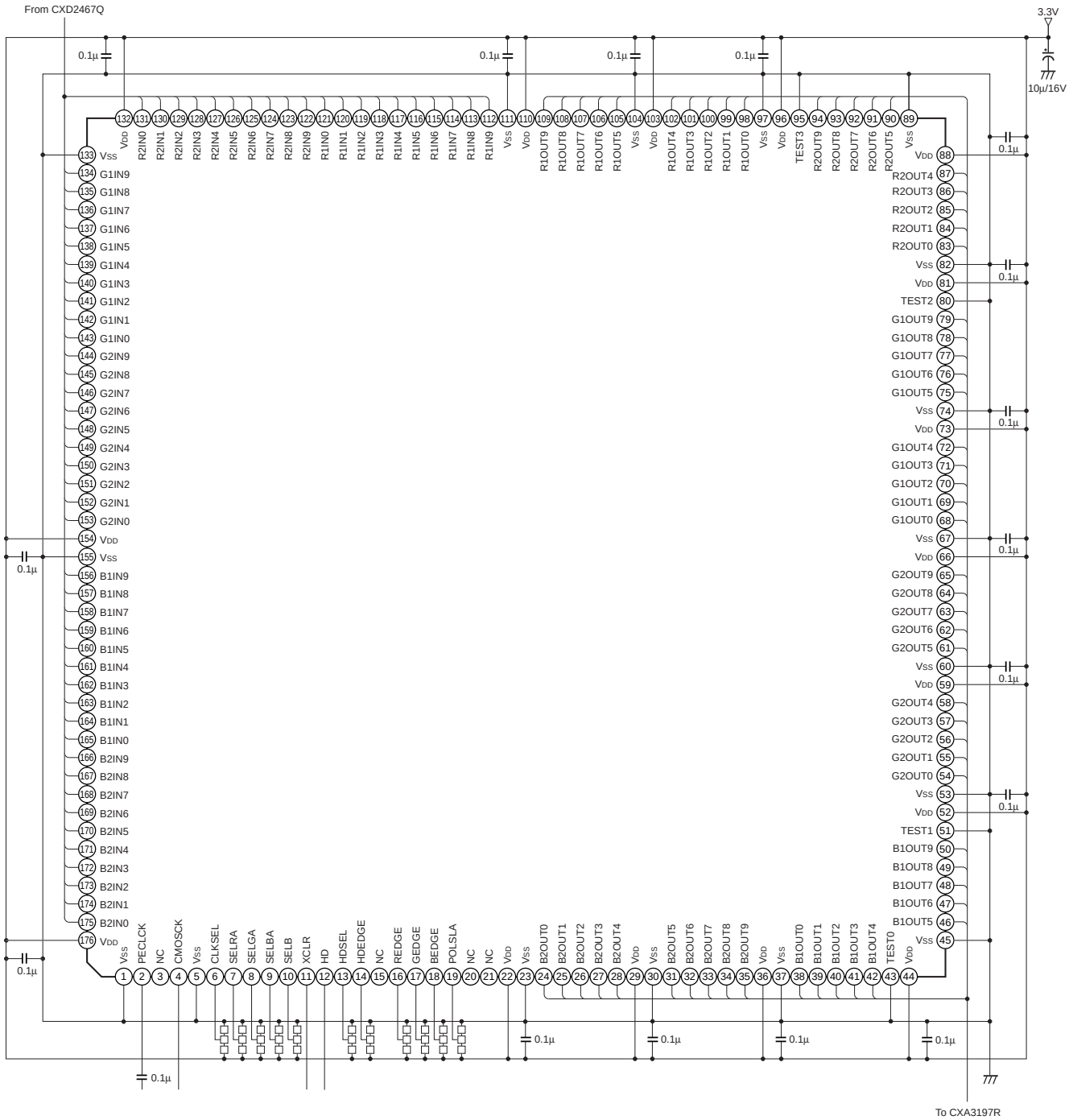
| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| High level input voltage | $V_{IH}$ | 0.4 | — | 3.6 | V |
| Low level input voltage | $V_{IL}$ | 0 | — | 3.2 | V |
| Input frequency | f | — | — | 80 | MHz |
| Input amplitude*1 | Vpp | 0.4 | — | — | V |

Applicable pins: PECLCK (Pin 2)

*1 Input the signal through a capacitor. Also, this amplitude is the value between the through capacitor and the input pin.



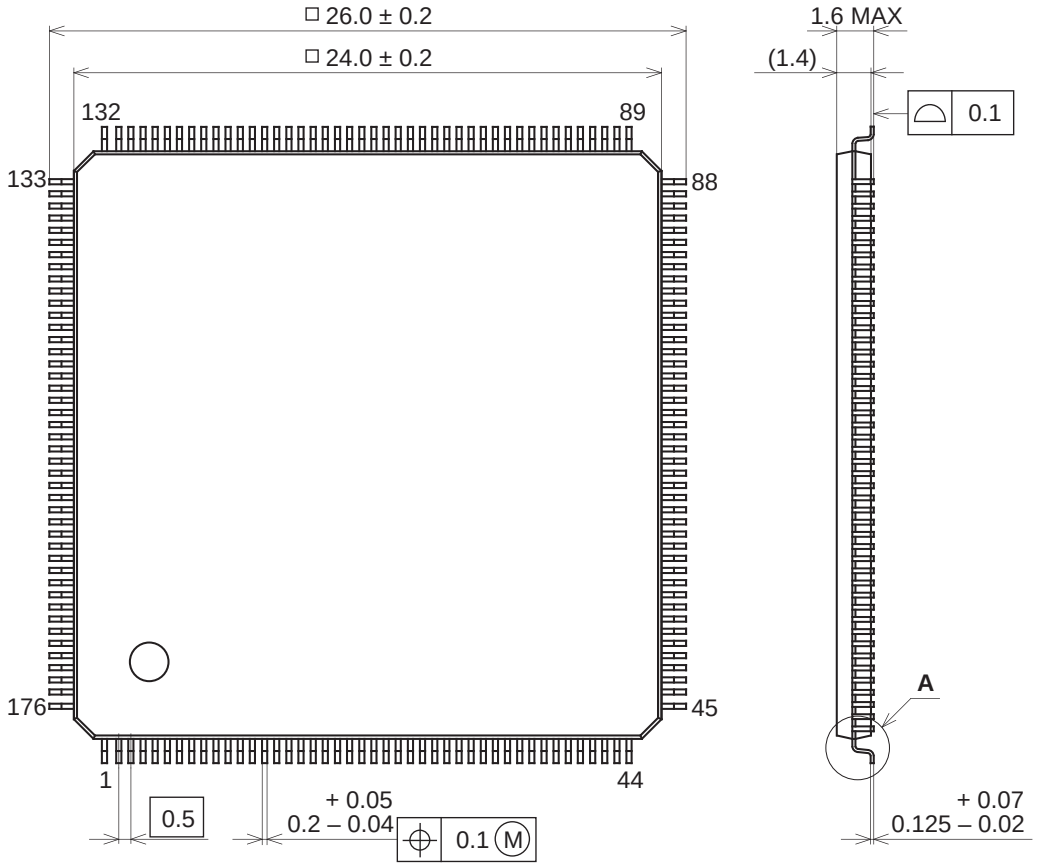
## Application Circuit

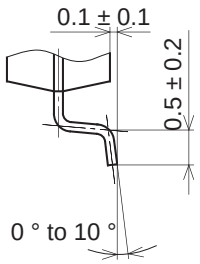



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

**Package Outline** Unit: mm

176PIN LQFP(PLASTIC)




DETAIL **A**

| | |
|---|---|
| SONY CODE | LQFP-176P-L061 |
| EIAJ CODE | P-LQFP176-24X24-0.5 |
| JEDEC CODE | ———— |

PACKAGE STRUCTURE

| | |
|---|---|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER PLATING |
| LEAD MATERIAL | 42 ALLOY |
| PACKAGE MASS | 1.8 g |