# XRT6164A

## Digital Line Interface Transceiver

October 2007

### FEATURES

- Single 5V Supply
- Compatible with CCITT G.703 64Kbps Co-Directional Interface Recommendation When Used With Either XRT6165 or XRT6166
- Low Power
- Converts Balanced CMOS Transmit and Receive Signals Propagated Over Two Twisted Pair Cables to TTL Compatible Dual-Rail Data
- Links Remote Equipment Equipped With CCITT G.703 64Kbps Co-Directional Interfaces Over Distances Up to 500 Meters Without Equalization
- Receive Data Comparator Threshold Storage Provides Ping-Pong Operation Capability
- Loss of Signal Alarm
- Dual Matched Driver Outputs

### APPLICATIONS

- Data Adaption Unit (DAU)
- General Purpose TTL Compatible Line Interface

### GENERAL DESCRIPTION

The XRT6164A is a CMOS analog chip intended for general purpose line interface applications at bit rates up to 1.544Mbps (T1). It contains both receive and transmit circuitry in a 16-pin dual-in-line plastic (PDIP) package. The receiver is designed for short line applications having a cable loss up to 10dB measured at the half bit rate. The transmitter has open collector line driver outputs that are capable of handling up to 40mA. When used in conjunction with either XRT6165 or XRT6166, the chip set provides a 64Kbps codirectional interface as specified in CCITT G.703.

### ORDERING INFORMATION

| Part No. | Package | Operating Temperature Range |
|---|---|---|
| XRT6164AIP | 16-Lead 300 Mil PDIP | -40° C to +85° C |
| XRT6164AID | 16-Lead 300 Mil JEDEC SOIC | -40° C to +85° C |



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## Block Diagram

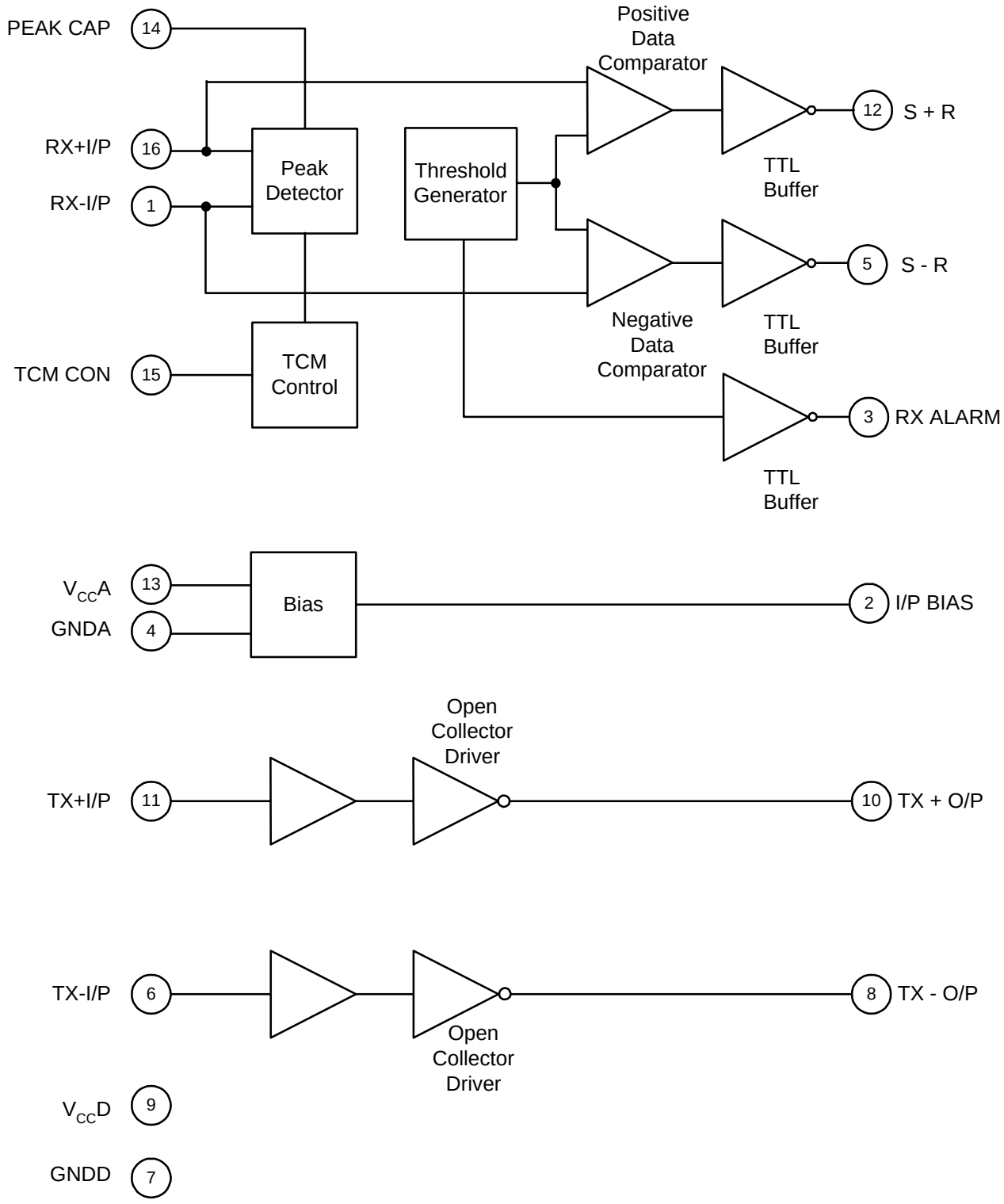
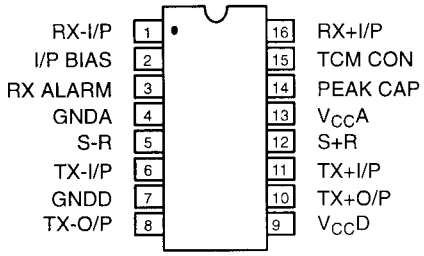
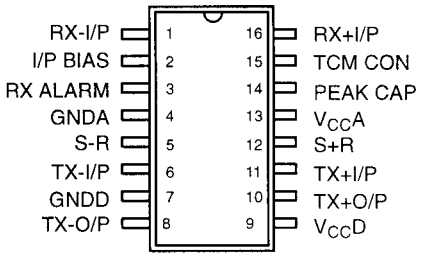



**Figure 1. XRT6164A Block Diagram**

## PIN CONFIGURATION




**16 Lead PDIP (0.300")**




**16 Lead SOIC (Jedec, 0.300")**

## PIN DESCRIPTION

| Pin# | Symbol | Type | Description |
|---|---|---|---|
| 1 | RX-I/P | I | **Receiver Negative CMOS Input.** Line analog input. |
| 2 | I/P BIAS | O | **Receive Input Bias.** Connects to center tap of input transformer secondary winding. |
| 3 | RX ALARM | O | **Loss of Signal Alarm.** Active low. |
| 4 | GNDA | | **Analog Ground.** |
| 5 | S-R | O | **Receive Negative Data Output.** Output from negative CMOS input pulses (active low). |
| 6 | TX-I/P | I | **Transmit Negative Input Data.** Input for negative output driver (active high). |
| 7 | GNDD | | **Digital Ground.** |
| 8 | TX-O/P | O | **Transmit Negative Output Driver.** Open collector, drives output transformer primary. |
| 9 | $V_{CC}$D | | **+5V +/-5% Digital Supply.** |
| 10 | TX+O/P | O | **Transmit Positive Output Driver.** Open collector, drives output transformer primary. |
| 11 | TX+I/P | I | **Transmit Positive Input Data.** Input for positive output driver (active high). |
| 12 | S+R | O | **Receive Positive Data Output.** Output from positive CMOS input pulses (active low). |
| 13 | $V_{CC}$A | | **+5V +/-5% Analog Supply.** |
| 14 | PEAK CAP | | **Peak Detector Capacitor.** Stores peak detector voltage. |
| 15 charge | TCM CON | I | **Time Compression Multiplex Control.** When active, disconnects peak detector and discharge paths (active low). |
| 16 | RX+I/P | I | **Receiver Positive CMOS Input.** Line analog input. |

## ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{CC}$ = 5V +/- 5%, $T_A$ = 25°C, Unless Otherwise Specified

| Parameters | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| **DC Electrical Characteristics** | | | | | |
| Supply Voltage | 4.75 | 5 | 5.25 | V | |
| Analog Supply Current | | **7** | **10** | mA | |
| Digital Supply Current | | **17** | **22** | mA | |
| **Receiver** | | | | | |
| Input Signal | | 1 | 2.2 | Vp | Measured from Pins 1 or 16 with Respect to Pin 2 |
| Dynamic Range | | | 10 | dB | Maximum Cable Loss Range |
| Input Impedance | | 20 | | kΩ | Measured Between Pins 1 and 16 |
| Input Slicing Threshold | | 50 | | % | Percent of Peak Input Signal Amplitude |
| Input Bias Voltage | | **1.45** | | V | Measured at Pin 2 |
| Loss of Signal Alarm Threshold | | 150 | | mVp | Measured from Pins 1 or 16 with Respect to Pin 2 |
| Loss of Signal Alarm Level Hysteresis | | 1.5 | | dB | Difference Between Alarm-on and Alarm-off Levels |
| Peak Detector Leakage | | -80 | | µA | |
| Data Output Low | | | **0.4** | V | Measured at Pins 5 or 12, $I_{OUT}$ = +1.6mA |
| Data Output High | **3.0** | | | V | Measured at Pins 5 or 12, $I_{OUT}$ = -40µA |
| Alarm Output Low | | | **0.4** | V | Measured at Pin 3; $I_{OUT}$ = +1.6mA |
| Alarm Output High | **$V_{cc}$ -** 0.5 | | | V | Measured at Pin 3; $I_{OUT}$ = -40µA |
| TCM Input Low Voltage | | | **0.8** | V +5µA | Measured at Pin 15; $I_{IN}$ Min = -500µA, $I_{IN}$ Max = |
| **Transmitter** | | | | | |
| Input Low Voltage | | | 0.8 | V | Measured at Pins 6, 11; $I_{IN}$ = -700µA |
| Input High Voltage | 2.2 | | | V | Measured at Pins 6, 11; $I_{IN}$ = +5µA |
| Output Low Voltage | | | **1.2** | V | Measured at Pins 8, 10; $I_{OUT}$ = -40mA |
| Output Low Current | | | 40 | mA | Measured at Pins 8, 10; $V_{OUT}$ = 1V |
| Output Leakage Current | **-100** | | | µA | Measured at Pins 8, 10; $V_{OUT}$ = 10V Outputs in off state |
| **AC Electrical Characteristics** | | | | | |
| **Receiver** | | | | | |
| Input Level | | 1 | 2.2 | Vp | Pin 1, 16 with Respect to Pin 2 1 |
| Output Rise Time | | | **80** | ns | Pins 5, 12; C L = 15pF, 10% to 90% |
| Output Fall Time | | | 80 | ns | Pins 5, 12; C L =15pF, 90% to 10% |

***Notes:***

*1. Higher input voltages are possible if a resistive input attenuator is used.*

***Bold face parameters** are covered by production test and guaranteed over operating temperature range.*

## ELECTRICAL CHARACTERISTIC (CONT'D)

| Parameters | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| **AC Electrical Characteristics (Cont'd)** | | | | | |
| **Transmitter** | | | | | |
| Output Rise Time | | | **80** | ns | Pins 8, 10; $R_L$ = 130, $C_L$ = 15pF, 10% to 90% |
| Output Fall Time | | | **80** | ns | Pins 8, 10; $R_L$ = 130, $C_L$ = 15pF, 90% to 10% |
| Rising Edge Delay | | | **100** | ns | Pins 8, 10; $R_L$ = 130, $C_L$ = 15pF, 50% to 50% (I/P to O/P) |
| Falling Edge Delay | | | **100** | **n**s | Pins 8, 10; $R_L$ = 130, $C_L$ = 15pF, 50% to 50% (I/P to O/P) |

*Notes:*
*Bold face parameters are covered by production test and guaranteed over operating temperature range.*
*Specifications are subject to change without notice*

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 20V
Storage Temperature ..... -65°C to +150°C

**Magnetic Supplier Information:**

Pulse
Telecom Product Group
P.O. Box 12235
San Diego, CA 92112
Tel. (619) 674-8100
Fax. (619) 674-8262

Transpower Technologies, Inc.
24 Highway 28, Suite 202
Crystal Bay, NV 89402-0187
Tel. (702) 831-0140
Fax. (702) 831-3521

## SYSTEM DESCRIPTION

The XRT6164A is a general purpose line interface chip that contains the receive and transmit circuitry necessary to convert TTL logic levels to a CMOS signal both to and from a twisted pair cable.

### Receiver

The XRT6164A receiver section converts a balanced CMOS signal that has been attenuated and distorted by up to 10dB of twisted pair cable to active-low TTL-compatible logic levels.

The cable is transformer coupled to the receiver differential inputs (RX+IP, RX-IP) which are biased through the input transformer secondary winding by a voltage generated on-chip (I/P BIAS). The CMOS receive signal is applied to a peak detector, and to a pair of data comparators. The peak detector output voltage charges an external capacitor connected to PEAK CAP. This voltage generates a data comparator bias level that is approximately 50% of the peak input pulse amplitude.

Thus, data slicing is automatically accomplished at the optimum level over the full cable loss range. TTL-compatible output stages buffer the receiver digital outputs (S+R, S-R) and provide active low signals corresponding to received positive and negative input pulses.

Loss of input signal is detected by a comparator that monitors input signal level. An active-low TTL-compatible logic level (RX ALARM) indicates signal loss. Comparator hysteresis prevents chatter on this output. Ping-pong operation is made possible by the time compression multiplex control input (TCM CON). A logic 0 applied to this pin during transmission stores the peak detector output voltage by disconnecting the peak detector storage capacitor charge and discharge paths.

Since the receive data comparator bias voltage is stored during transmit mode, it is immediately available when receive mode resumes.

### Transmitter

The XRT6164A transmitter section contains two matched open collector output drivers that are capable of driving the line transformer directly with a current up to 40mA. The transmitter output drivers include diode clamps to ensure non-saturating operation. Transmitter digital inputs, which are active-low, are TTL-compatible. External resistors are used between the transmitter outputs and the output transformer primary to set the output pulse amplitude.

## APPLICATION INFORMATION

*Figure 2* shows a general line driver application circuit using the XRT6164A. This device converts CMOS transmit and receive signals in the 64Kbps to 1.544Mbps range to active-low TTL-compatible logic levels. CMOS signals that have been attenuated and distorted by twisted pair cable are transformer-coupled to the line side of the XRT6164A as shown on the left side of *Figure 2*. Suggested transformers for both the input and output applications are the Pulse types PE-65535 or TTI-7147 for 64Kbps use and the PE-65835 for 1.544Mbps applications.

The right side of *Figure 2* shows the TTL-compatible digital inputs and outputs. Please refer to the pin description section of this data sheet for detailed information about each signal.

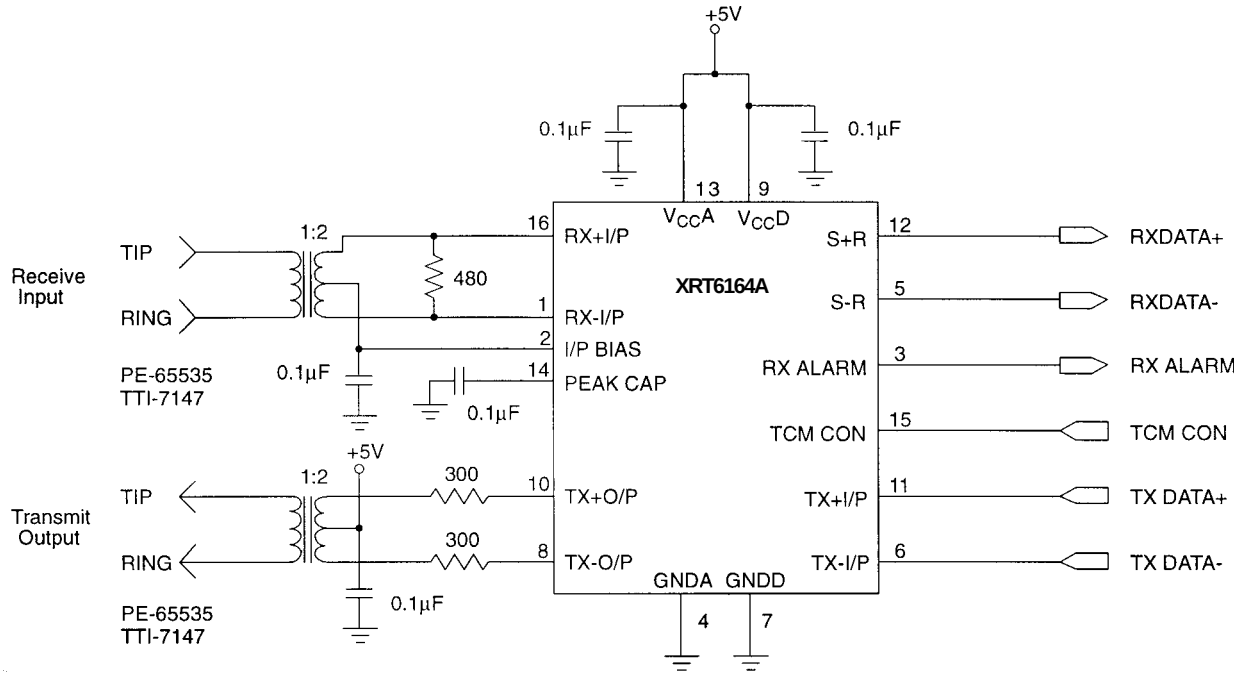
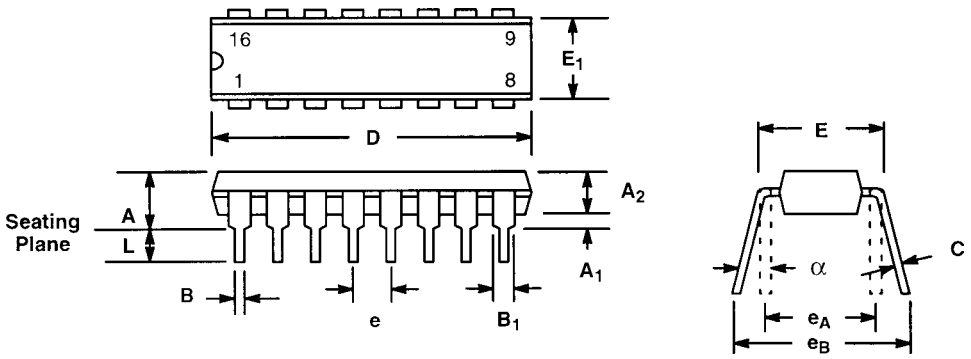



**Figure 2. XRT6164A Line Driver Application**

## 16 LEAD PLASTIC DUAL-IN-LINE
## (300 MIL PDIP)

Rev. 1.00

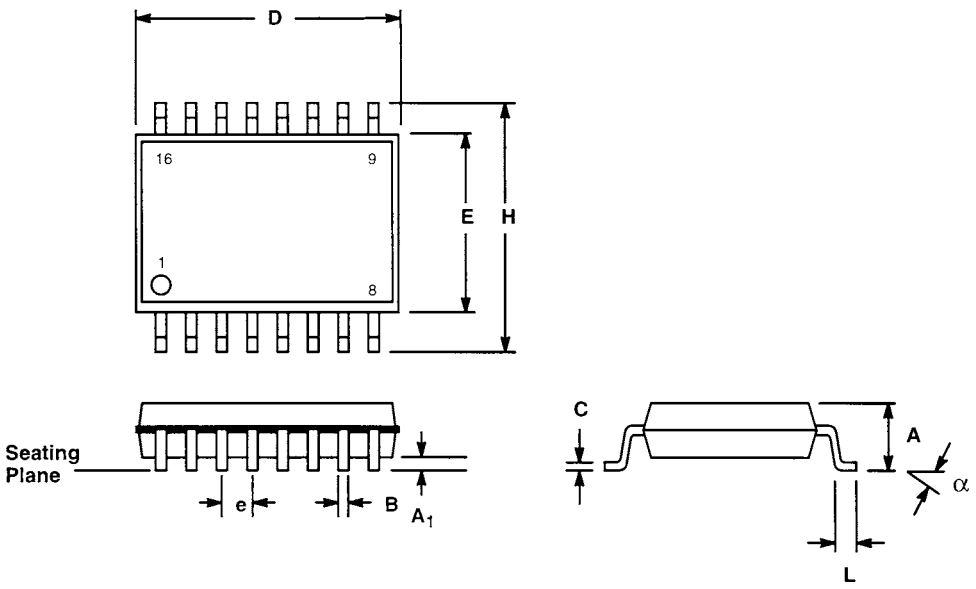



| SYMBOL | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.145 | 0.210 | 3.68 | 5.33 |
| A1 | 0.015 | 0.070 | 0.38 | 1.78 |
| A 2 | 0.115 | 0.195 | 2.92 | 4.95 |
| B | 0.014 | 0.024 | 0.36 | 0.56 |
| B 1 | 0.030 | 0.070 | 0.76 | 1.78 |
| C | 0.008 | 0.014 | 0.20 | 0.38 |
| D | 0.745 | 0.840 | 18.92 | 21.34 |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E 1 | 0.240 | 0.280 | 6.10 | 7.11 |
| e | 0.100 BSC | | 2.54 BSC | |
| e A | 0.300 BSC | | 7.62 BSC | |
| e B | 0.310 | 0.430 | 7.87 | 10.92 |
| L | 0.115 | 0.160 | 2.92 | 4.06 |
| α | 0° | 15° | 0° | 15° |

***Note:*** *The control dimension is the inch column*

## 16 LEAD SMALL OUTLINE
## (300 MIL JEDEC SOIC)

Rev. 1.00




| SYMBOL | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.093 | 0.104 | 2.35 | 2.65 |
| A 1 | 0.004 | 0.012 | 0.10 | 0.30 |
| B | 0.013 | 0.020 | 0.33 | 0.51 |
| C | 0.009 | 0.013 | 0.23 | 0.32 |
| D | 0.398 | 0.413 | 10.10 | 10.50 |
| E | 0.291 | 0.299 | 7.40 | 7.60 |
| e | 0.050 BSC | | 1.27 BSC | |
| H | 0.394 | 0.419 | 10.00 | 10.65 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |
| α | 0° | 8° | 0° | 8° |

*Note: The control dimension is the millimeter column*

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