MP7226

BiCMOS
Fixed, Quad, Voltage Output, Single or Dual Supply 8-Bit Digital-to-Analog Converter

FEATURES

- **MPS Pioneered Segmented DAC Approach**
- **Four 8-Bit DACs with Buffer Amplifiers**
- **Bipolar Amplifier Inputs for Low Noise and Drift**
- **Operates with Single or Dual Supplies**
- **µP Compatible (95ns $\overline{WR}$)**
- **No External Adjustments Required**
- **Power-on-Reset Function**
- **Specified for 5 to 15 V Operation**
- **ESD Protection: 2000 Volts Minimum**
- **Latch-Up Proof**
- **Octal Available: MP7228**

APPLICATIONS

- **Function Generators**
- **Automatic Test Equipment**
- **Process Controls**

BENEFITS

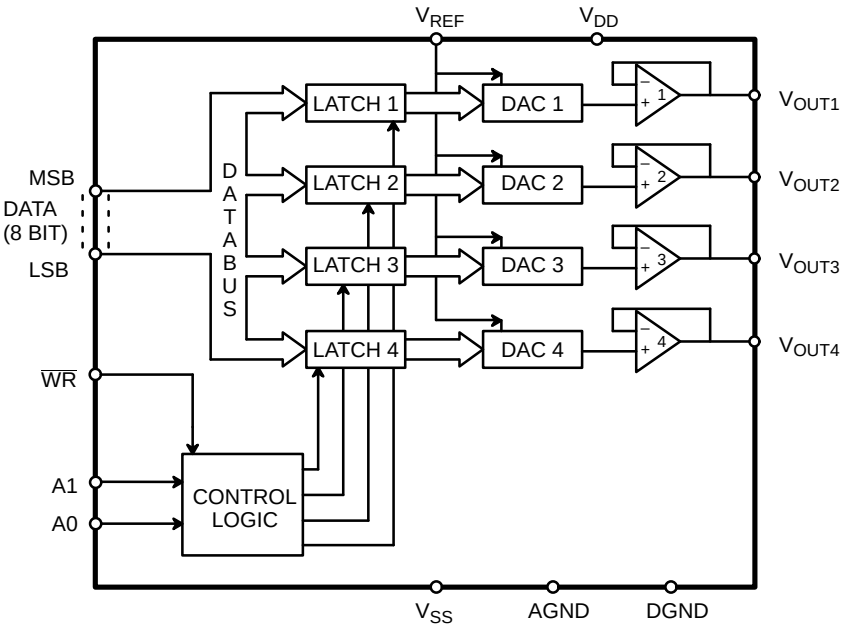
- **Reduced Board Space; Lower System Cost**
- **Reduced System Errors due to Excellent DAC-to-DAC Matching and Tracking**
- **Easy to Design with Microprocessors**
- **Stable, High Reliability through Advanced Processing**
- **Lower 1/f Noise Increases Useful Dynamic Range**

GENERAL DESCRIPTION

The MP7226 contains four 8-bit voltage-output Digital-to-Analog Converters, with BiCMOS output buffer amplifiers and interface logic on a monolithic chip. Separate on-chip latches are provided for each of the four D/A converters. The control logic is speed compatible with most 8-bit microprocessors. All digital inputs are TTL/CMOS(5V) compatible.

The MP7226 is manufactured using advanced thin film resistors on a double metal BiCMOS process. The MP7226 incorporates a unique bit decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. The MP7226 maintains 8-Bit accuracy over the full operating temperature range without laser trim or external adjustments.

SIMPLIFIED BLOCK DIAGRAM



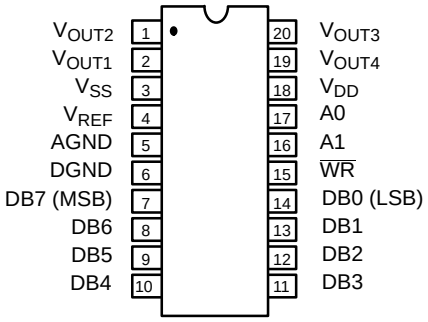
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Full Scale Error (LSB)
Plastic Dip	–40 to +85°C	MP7226KN	1	±1/2	±1
Plastic Dip	–40 to +85°C	MP7226LN*	1/2	±1/2	±1/2
PLCC	–40 to +85°C	MP7226KP	1	±1/2	±1
PLCC	–40 to +85°C	MP7226LP*	1/2	±1/2	±1/2
SOIC	–40 to +85°C	MP7226KS	1	±1/2	±1
SOIC	–40 to +85°C	MP7226LS*	1/2	±1/2	±1/2

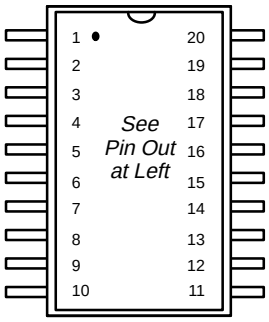
*Contact factory for availability.

PIN CONFIGURATIONS

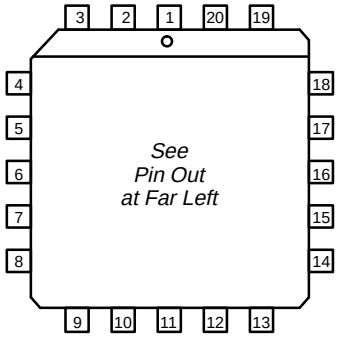
See Packaging Section for Package Dimensions



20 Pin PDIP (0.300")
N20



20 Pin SOIC (Jedec, 0.300")
S20



20 Pin PLCC
P20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	V_{OUT2}	DAC 2 Voltage Output
2	V_{OUT1}	DAC 1 Voltage Output
3	V_{SS}	Negative Power Supply (0 V to –5 V)
4	V_{REF}	Reference Input Voltage
5	AGND	Analog Ground
6	DGND	Digital Ground
7	DB7	Data Input Bit 7 (MSB)
8	DB6	Data Input Bit 6
9	DB5	Data Input Bit 5
10	DB4	Data Input Bit 4

PIN NO.	NAME	DESCRIPTION
11	DB3	Data Input Bit 3
12	DB2	Data Input Bit 2
13	DB1	Data Input Bit 1
14	DB0	Data Input Bit 0 (LSB)
15	$\overline{WR}$	Write (Active Low)
16	A1	DAC Address Bit 1
17	A0	DAC Address Bit 0
18	V_{DD}	Positive Power Supply (+5 to +15 V)
19	V_{OUT4}	DAC 4 Voltage Output
20	V_{OUT3}	DAC 3 Voltage Output

ELECTRICAL CHARACTERISTICS

Single or Dual Supply Operation (V_{DD} = +10.8 V to 16.5 V, V_{SS} = 0 V or –5 V ±10%, AGND = 0 V, DGND = 0 V, V_{REF} = +2 V to +10 V, R_L = 2kΩ, C_L = 100pF unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE								
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	
K				1		1		End Point Linearity Spec
L				1/2		1/2		
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
K				±1/2		±3/4		
L				±1/2		±3/4		
Total Unadjusted Error[2]							LSB	V_{DD} = 15 V ±10%, V_{REF} = +10 V
K				±2		±2		
L				±1		±1		
Full Scale Error[3]							LSB	V_{REF} = +10 V typ. Tempco is 5 ppm/°C
K				±1		±1		
L				±1/2		±1/2		
Zero Code Error							mV	TA = 25°C typ. Tempco is 30µV/°C
K				±20		±30		
L				±15		±20		
Output Load Resistance		2			2		kΩ	V_{OUT} = +10 V
DYNAMIC PERFORMANCE[4]								
Voltage Output Slew Rate		2	4		2		V/µs	
Voltage Output Settling Time				4		5	µs	V_{REF} = +10 V; Settling Time to ±1/2 LSB
Digital Feedthrough			25				nVs	Code transition all 0s to all 1s V_{REF} = 0 V, $\overline{WR}$ = V_{DD}
Digital Crosstalk[5]			25				nVs	Code transition all 0s to all 1s V_{REF} = +10 V, $\overline{WR}$ = 0 V
REFERENCE INPUT								
Reference Input Range[1]		1		10	1	10	V	Limitation: $V_{REF} - V_{SS}$ < 11 V
Reference Input Resistance	R_{IN}	2			2		kΩ	Min R_{IN} at Code 149_{10}
Reference Input Capacitance[4]			500				pF	Occurs when all DACs are loaded with all 1s
AC Feedthrough			–70				dB	V_{REF} = 10 kHz, 5 V p-p sinewave
DIGITAL INPUTS								
Input High Voltage	V_{INH}	2.4			2.4		V	
Input Low Voltage	V_{INL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±1	µA	V_{IN} = 0 V or V_{DD}
Input Capacitance[4]				8		8	pF	
Input Coding								Binary

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY								
V_{DD} Range		10.8		16.5	10.8	16.5	V	For specified performance
V_{SS} Range (Dual Supplies)[8]		0		–5.5	0	–5.5	V	For specified performance
I_{DD}				12		14	mA	Outputs unloaded; V_{IN}=V_{INL} or V_{INH}
I_{SS} (Dual Supplies)				10		12		Outputs unloaded; V_{IN}=V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[4, 6, 7]								
Address to $\overline{WR}$ Setup Time, t1	t_{AS}	0			0		ns	
Address to $\overline{WR}$ Hold Time, t2	t_{AH}	0			0		ns	
Data Valid to $\overline{WR}$ Setup Time, t3	t_{DS}	70			95		ns	
Data Valid to $\overline{WR}$ Hold Time, t4	t_{DH}	10			10			
$\overline{WR}$ Pulse Width, t5	t_{WR}	95			120		ns	

NOTES:

1 V_{OUT} must be less than V_{DD} by 3.5 V to ensure correct operation.

2 Total Unadjusted Error includes zero code error, relative accuracy and full-scale error.

3 Calculated after zero code error has been adjusted out.

4 Sample tested at 25°C to ensure compliance.

5 The glitch impulse transferred to the output of one converter (not adjusted) due to a change in the digital input code to another addressed converter.

6 All input rise and fall times are measured from 10% to 90% of +5 V, t_R = t_F = 5 ns.

7 Timing measurement reference level is (V_{INH} + V_{INL})/2.

Specifications are subject to change without notice

ELECTRICAL CHARACTERISTICS

Single & Dual ±5 V Supply Operation (V_{DD} = +5 V ±5%, V_{SS} = 0 V to –5 V ±10%, V_{REF} = +1.25 V, AGND = 0 V, DGND = 0 V, R_L = 2kΩ, C_L = 100pF unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE								
Resolution (All Grades)	N	8			8		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	
K				2		2		End Point Linearity Spec
L				1		1		
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
K				±1		±1		
L				±1		±1		
Total Unadjusted Error[2]				±4			LSB	V_{DD} = 5 V ±5%, V_{REF} = 1.25 V
Full Scale Error[3]							LSB	V_{REF} = +1.25 V
K				±4		±4		
L				±2		±2		
Zero Code Error				±20			mV	
Output Load Resistance		2					kΩ	V_{OUT} = +10 V
DYNAMIC PERFORMANCE[4]								
Voltage Output Slew Rate		2	4				V/µs	
Voltage Output Settling Time				4			µs	V_{REF} = +1.25 V; Settling Time to ±1/2 LSB
Digital Feedthrough			25				nVs	Code transition all 0s to all 1s V_{REF} = 0 V, $\overline{WR}$ = V_{DD}
Digital Crosstalk[5]			25				nVs	Code transition all 0s to all 1s V_{REF} = +1.25 V, $\overline{WR}$ = 0 V
REFERENCE INPUT								
Reference Input Range		1		1.6	1	1.6	V	V_{OUT} must be < V_{DD} by 3.2V
Reference Input Resistance	R_{IN}	2			2		kΩ	
Reference Input Capacitance[4]			500				pF	Occurs when all DACs are loaded with all 1s
AC Feedthrough			–70				dB	V_{REF} = 10 kHz, 1/2 V p-p sinewave
DIGITAL INPUTS								
Input High Voltage	V_{INH}	2.4			2.4		V	
Input Low Voltage	V_{INL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±1	µA	V_{IN} = 0 V or V_{DD}
Input Capacitance[4]				8		8	pF	
Input Coding								Binary

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY								
V_{DD} Range		4.75		5.25	4.75	5.25	V	For specified performance
I_{DD}				8		8	mA	Outputs unloaded; $V_{IN}=V_{INL}$ or V_{INH}
I_{SS} (Dual Supplies)				6		6		Outputs unloaded; $V_{IN}=V_{INL}$ or V_{INH}
SWITCHING CHARACTERISTICS[4, 6, 7]								
Address to $\overline{WR}$ Setup Time, t1	t_{AS}	0			0		ns	
Address to $\overline{WR}$ Hold Time, t2	t_{AH}	0			0		ns	
Data Valid to $\overline{WR}$ Setup Time, t3	t_{DS}	70			95		ns	
Data Valid to $\overline{WR}$ Hold Time, t4	t_{DH}	0						
WR Pulse Width, t5	t_{WR}	95			120		ns	

NOTES:

1 V_{OUT} must be less than V_{DD} by 3.5 V to ensure correct operation.
2 Total Unadjusted Error includes zero code error, relative accuracy and full-scale error.
3 Calculated after zero code error has been adjusted out.
4 Sample tested at 25°C to ensure compliance.
5 The glitch impulse transferred to the output of one converter (not adjusted) due to a change in the digital input code to another addressed converter.
6 All input rise and fall times are measured from 10% to 90% of +5 V, $t_R = t_F = 5$ ns.
7 Timing measurement reference level is $(V_{INH} + V_{INL})/2$.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to AGND, DGND . . . . . 0 to +17 V
Digital Input Voltage to DGND . . . . . –0.5 to V_{DD} +0.5 V
V_{REF} to AGND, DGND . . . . . –0.5 to V_{DD} +0.5 V
V_{SS} to AGND, DGND . . . . . +0.5 to –7 V
AGND to DGND . . . . . ±1 V
(Functionality Guaranteed ±0.5 V)

Storage Temperature . . . . . –65°C to +150°C

Lead Temperature (Soldering, 10 seconds) . . . . . +300°C

Package Power Dissipation Rating to 75°C
PDIP, SOIC, PLCC 900mW
Derates above 75°C . . . . . 12mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

D/A CONVERTER SECTION

The MP7226 contains four matched, 8-bit, voltage-mode Digital-to-Analog Converters (DACs) which incorporate an MPS pioneered unique bit decoding technique. This decoding scheme reduces the maximum binary weight carried by any resistor switch, reducing the accuracy required of the switches and resistor network.

In the MP7226, the first three MSBs are decoded into three equal current sources, each contributing 25% of the full scale output current.

Decoding two bits to three, a 1% change in any one of the converter's three decoded current sources affects the output by no more than 0.25% of full scale, compared with 0.5% in a conventional R-2R type CMOS DAC.

The output voltages have the same polarity as the reference voltage, allowing single supply operation. The voltage reference range is from +2V to +10V. Each DAC uses a highly-stable, thin-film, ladder network and high-speed NMOS switches. *Figure 1.* shows a simplified circuit diagram for one channel.

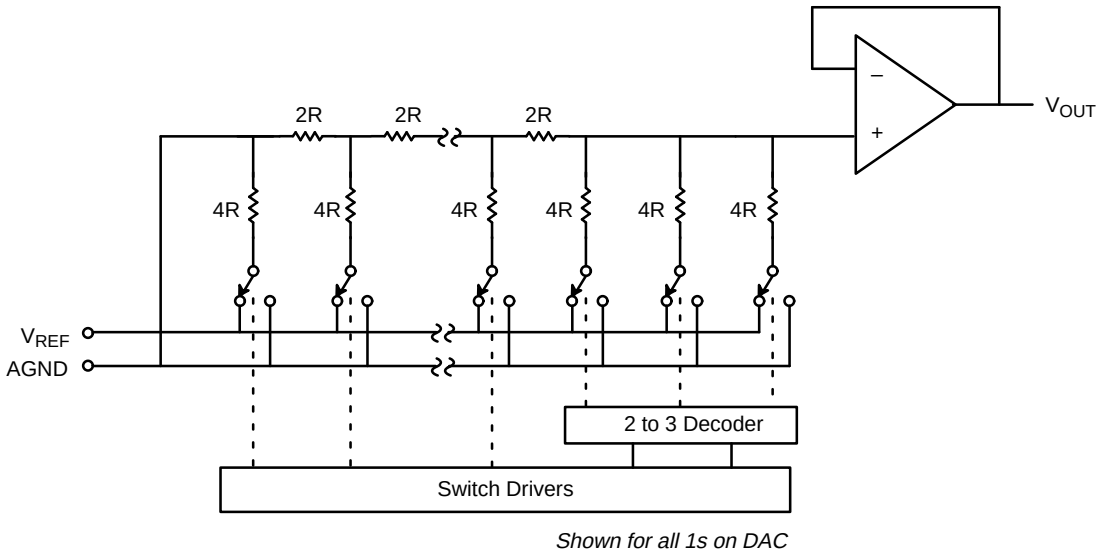


Figure 1. Simplified D/A Circuit Diagram

V_{REF} Input

The V_{REF} and AGND are common to all four DACs and set the full-scale output. The input impedance of the V_{REF} pin is the parallel combination of the four individual DAC reference impedances and is code dependent. This impedance varies from 2kΩ to 500kΩ. Therefore, it is very important that the external reference source output impedance is low enough so that its output voltage will not be affected by the varying digital code. Due to transient currents at the V_{REF} input during digital code changes, a 0.1µF or greater decoupling capacitor on that V_{REF} input is recommended. The input capacitance at the V_{REF} pin is also code dependent and typically varies from less than 120pF to 350pF.

Each V_{OUT} voltage can be represented by a digitally programmable voltage source using the following expression :

$$V_{OUT} = Dn \times V_{REF}/256$$

where Dn is the decimal equivalent to the digital input code and can vary from 0 to 255.

Output Buffer Amp

Each D/A converter output is buffered by a unity gain noninverting BiCMOS amplifier which has slew rate greater than 2 V/µs . The output buffer settles to ±1/2 LSB in less than 4µs when driving a load of 2kΩ in parallel with 100pF with a full scale transition from 0V to +10V or from +10V to 0V . The buffers can drive 2kΩ and 500pF to 10V levels without oscillation.

A simplified circuit diagram of the output buffer is shown in *Figure 2.* The Input stage is provided by BiCMOS PNP transistors with resulting lower input offset voltage, offset voltage drift over time and noise when compared to MOS process . The amplifier output stage uses a substrate NPN bipolar device to provide a low output impedance, high-output current capability.

The MP7226 is specified for single or dual power supply operation, with only the buffer amplifier outputs using V_{SS} supply current . Operating the MP7226 from dual supplies will improve the negative going output settling time near ground. In dual supply voltage operation , the output amplifier can sink 500µA when V_{OUT} = 0 V.

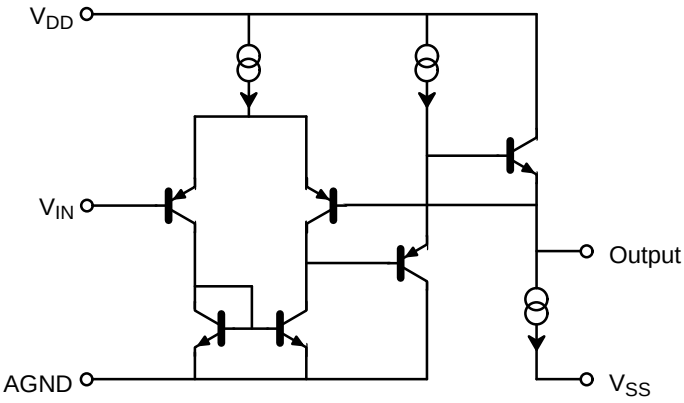


Figure 2. Simplified Output Buffer Amplifiers

The amplifiers outputs may be shorted to ground. However, the power dissipation of the package should not exceed the maximum limit.

Digital Inputs

All of the digital inputs to this DAC maintain TTL level interface compatibility and can also be driven directly with 5V CMOS logic inputs. The digital inputs are ESD protected to a rating of 2000 volts.

Digital Interface Logic

The MP7226 allows direct interface to most microprocessor buses without additional interface circuitry.

Figure 3. shows the input control logic circuit diagram and *Table 1.* shows the control logic truth table and operation for $\overline{WR}$, A1, A0. The address lines A0, and A1 determine which DAC will accept the input data. The $\overline{WR}$ input determines whether the selected DAC is transparent (output follows the input), latched, or no operation. The $\overline{WR}$ input will also inhibit power on reset of the DAC latches to 0, if its initial state = 0 after 5 µs of power.

Figure 4. shows the write cycle timing diagram. When the $\overline{WR}$ signal is low, the input latch of the selected DAC is transparent, and the DAC's output corresponds to the value present on the data bus. On some data buses, data is not always valid for the entire period that the $\overline{WR}$ signal is low and can cause unwanted data at the output. Ensuring that the write pulse ($\overline{WR}$) conforms to the data hold time, (t4) spec will prevent this problem.

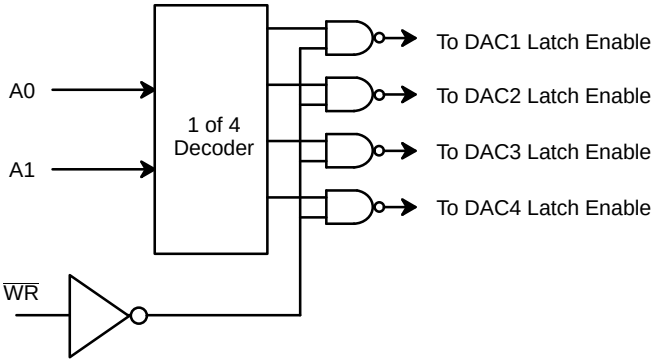
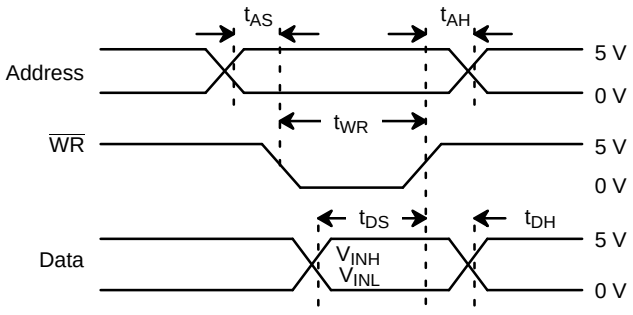


Figure 3. Input Control Logic

$\overline{WR}$	A1	A0	Operation
H	X	X	No Operation; Device Not Selected
L	L	L	DAC 1 Transparent
↑	L	L	DAC 1 Latched
L	L	H	DAC 2 Transparent
L	H	L	DAC 3 Transparent
L	H	H	DAC 4 Transparent

Table 1. Truth Table



NOTE: When the $\overline{WR}$ signal is low, the input latch of the selected DAC is transparent and any invalid data at this time will cause erroneous output.

Figure 4. Write Cycle Timing Diagram

APPLICATIONS INFORMATION

Power On Reset

At power up, all inputs are reset to 0 V if $\overline{WR}$ = 1. For $\overline{WR}$ = 0, the addressed DAC will receive input data.

Power Supply

The MP7226 can operate with either a single or dual power supply. Improved zero-code settling error can be obtained by using dual power supplies. The dual power supply specifications are a positive supply (V_{DD}) range of +10.5V to +16.5V, and a –5V supply (V_{SS}) . The single power supply specifications are a positive supply (V_{DD}) range of +10.5V to +16.5V, or range of +4.75V to 5.5V . The specified reference voltage (V_{REF}) range under these conditions is from +2V to V_{DD} –4V. For those applications requiring +10V at the output (V_{REF} = +10V), V_{DD} must be +14V minimum to meet data sheet limits . 8-bit performance is guaranteed for single supply operation (V_{SS} = 0V); however, zero code output sink capability is improved with V_{SS} = –5V. For adequate DAC and Buffer operation, V_{REF} must always be below V_{DD} by at least 3.5V.

Power Supply Decoupling

The Power Supplies used with the MP7226 should be well regulated and filtered. Local power supply decoupling consisting of a 10µF tantalum capacitor in parallel with a 0.01µF ceramic is recommended. The decoupling capacitors should be connected between the V_{DD} and AGND, and between V_{SS} and AGND if V_{SS} = –5V.

Unipolar Output Operation

In this configuration, the reference voltage is the same polarity as the output voltage. Since the reference voltage must always be positive with respect to GND, the output can only be 0 or positive.

Table 2. shows the code relationship for the part in unipolar operation

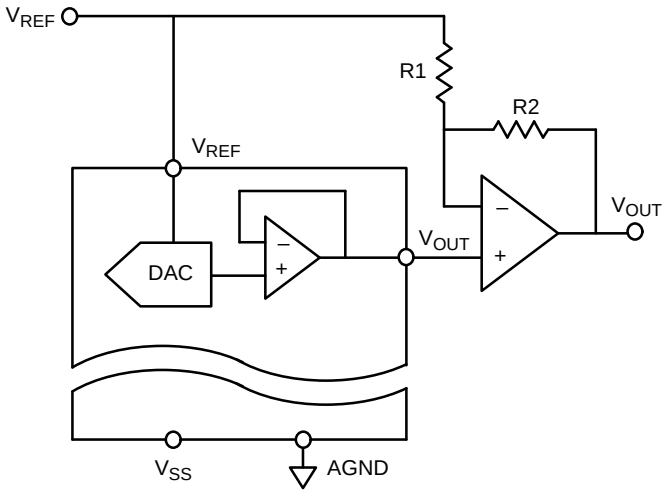
Digital Input	Analog Output, V_{OUT}
1 1 1 1 1 1 1 1	$+ V_{REF} \left(\frac{255}{256}\right)$
1 0 0 0 0 0 0 1	$+ V_{REF} \left(\frac{129}{256}\right)$
1 0 0 0 0 0 0 0	$+ V_{REF} \left(\frac{128}{256}\right) = + \frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1	$+ V_{REF} \left(\frac{127}{256}\right)$
0 0 0 0 0 0 0 1	$+ V_{REF} \left(\frac{1}{256}\right)$
0 0 0 0 0 0 0 0	$0\ V$

$Note: 1\ LSB = (2^{-8})\ (V_{REF}) = \frac{1}{256}\ (V_{REF})$

Table 2. Unipolar Code Table

Digital Input	Analog Output
1 1 1 1 1 1 1 1	$+ V_{REF} \left(\frac{127}{128}\right)$
1 0 0 0 0 0 0 1	$+ V_{REF} \left(\frac{1}{128}\right)$
1 0 0 0 0 0 0 0	0 V
0 1 1 1 1 1 1 1	$- V_{REF} \left(\frac{1}{128}\right)$
0 0 0 0 0 0 0 1	$- V_{REF} \left(\frac{127}{128}\right)$
0 0 0 0 0 0 0 0	$- V_{REF} \left(\frac{128}{128}\right) = - V_{REF}$

Table 3. Bipolar Code Table



$V_{OUT} = D_n \times V_{REF} \times (1+R2/R1) - V_{REF} \times R2/R1$
if R1 = R2
$V_{OUT} = V_{REF} \times (2D_n - 1)$
Where D_n is the digital input code and can vary from 0 to 255

Figure 5. Bipolar Output Circuit

Bipolar Binary Operation

The Bipolar Mode configuration for each DAC requires one external op-amp and two resistors per channel.

Figure 5. shows a typical Bipolar Operation circuit using the MP7226. *Table 3.* shows the code relationship for the circuit of *Figure 5.* assuming R1 = R2 .

AC Reference Signal

An AC signal can be applied to the reference of the MP7226 for multiplying capability within the upper (+10V) and lower (+2V) limits of the reference voltage input, with either single or dual supplies . This signal must be level shifted or AC coupled with proper bias level before being applied to the reference input. *Figure 6.* shows techniques for applying an AC signal to the MP7226. Since all four DACs share a common reference, they will all share this AC modulated reference. Input frequencies up to 50kHz will typically be distorted less than 0.1% .

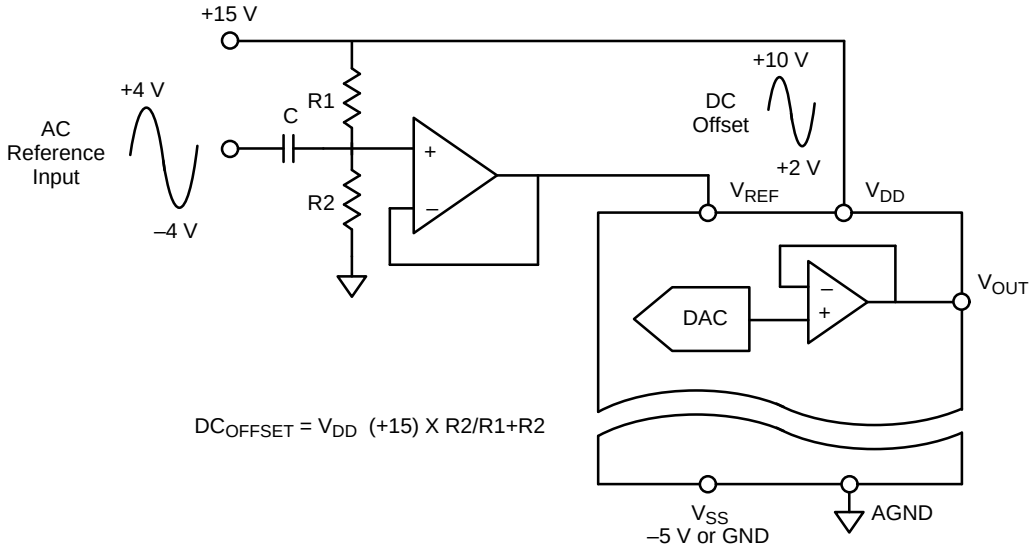


Figure 6. AC Reference Input Signal Circuit (AC Couple)

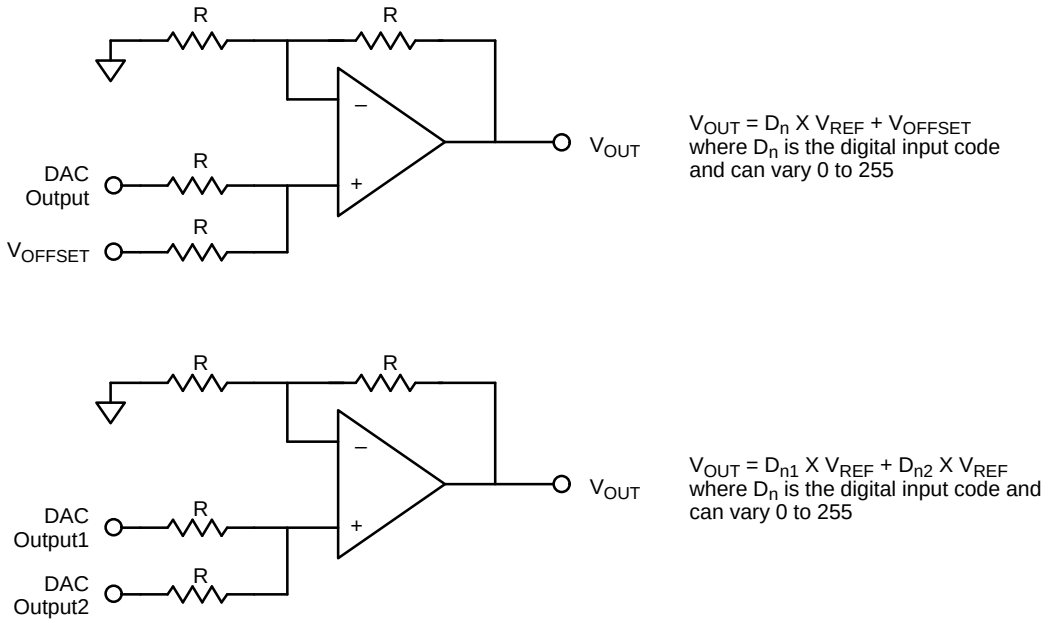


Figure 7. Digitally Programmable Offset Adjustment Circuits

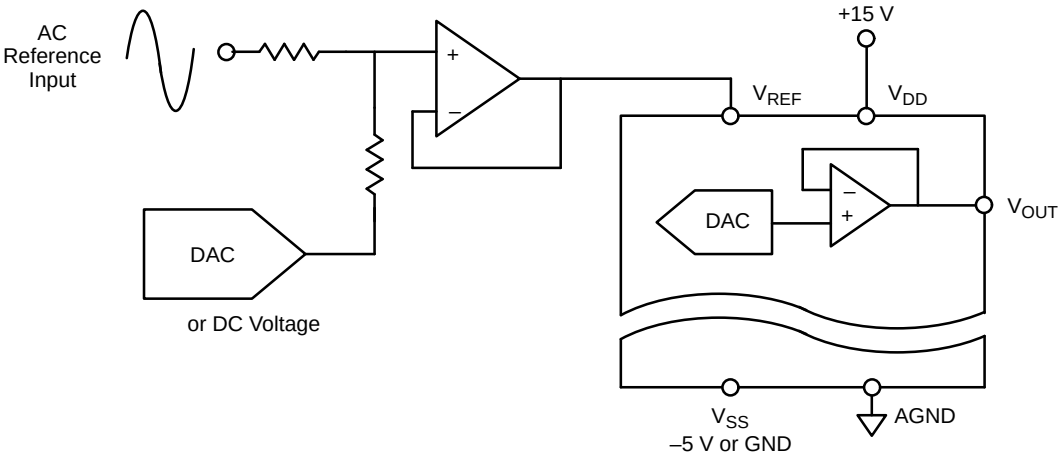


Figure 8. Digitally Programmable AC Reference Input Signal Circuit (DC Couple)

Offsetting DAC Outputs

Figure 7. shows examples of offset circuits.

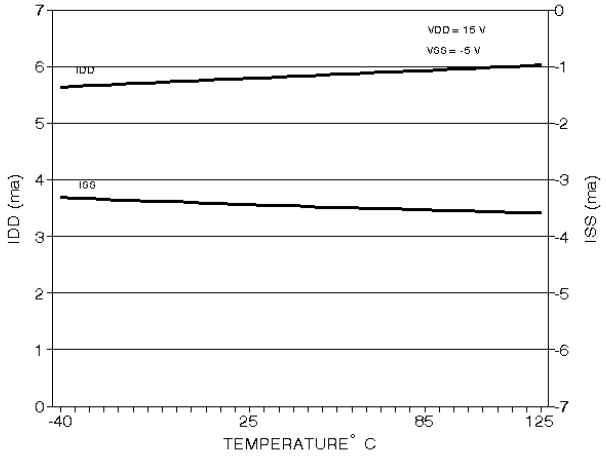
DAC offset effects

When using the device in single supply applications, and minimum reference voltage, there is a possibility that the DAC output will not change when the code is incremented from 0. Once the DAC has reached the offset voltage of the output buffer, the DAC output will begin to increment in a normal operation.

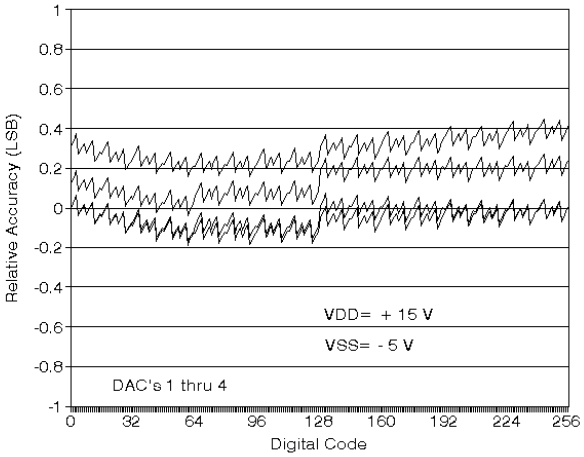
5V Operation

The MP7226 can be operated with a single power supply (V_{DD} = +5V) or dual power supplies (V_{DD} = +5V and V_{SS} = –5V) . The reference voltage range is reduced along with Some performance parameter degradation. However the DNL of each DAC remains at ±1 LSB guaranteeing monotonicity.

PERFORMANCE CHARACTERISTICS

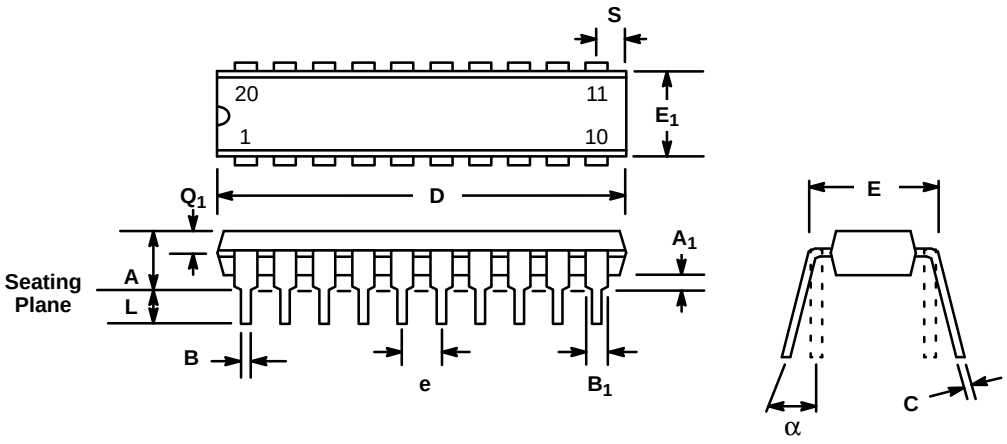


Graph 1. Power Supply Current vs. Temperature



Graph 2. Relative Accuracy vs. Digital Code

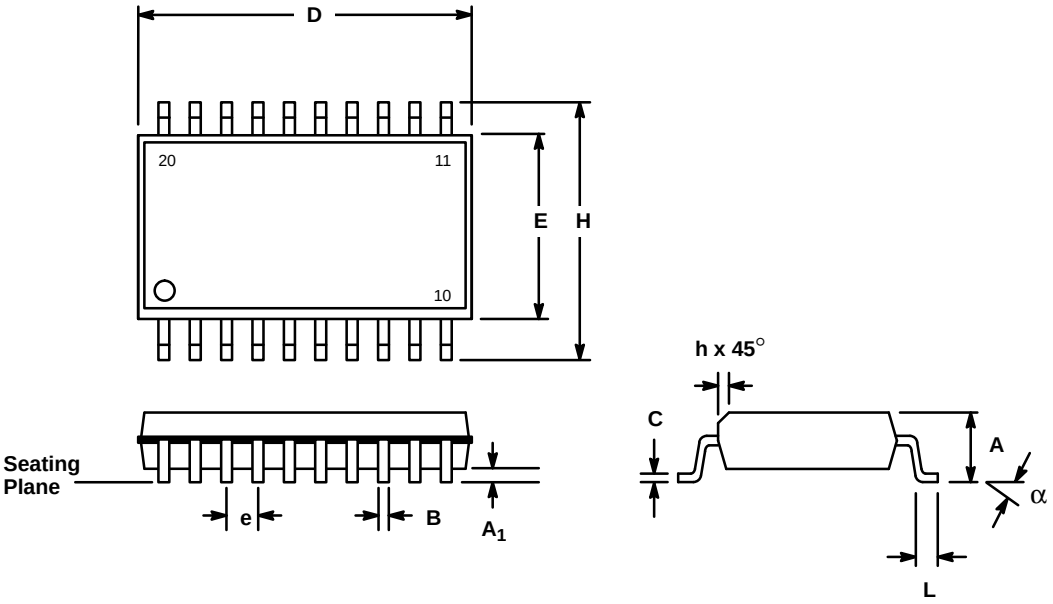
20 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.945	1.060	24.0	26.92
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.080	1.02	2.03

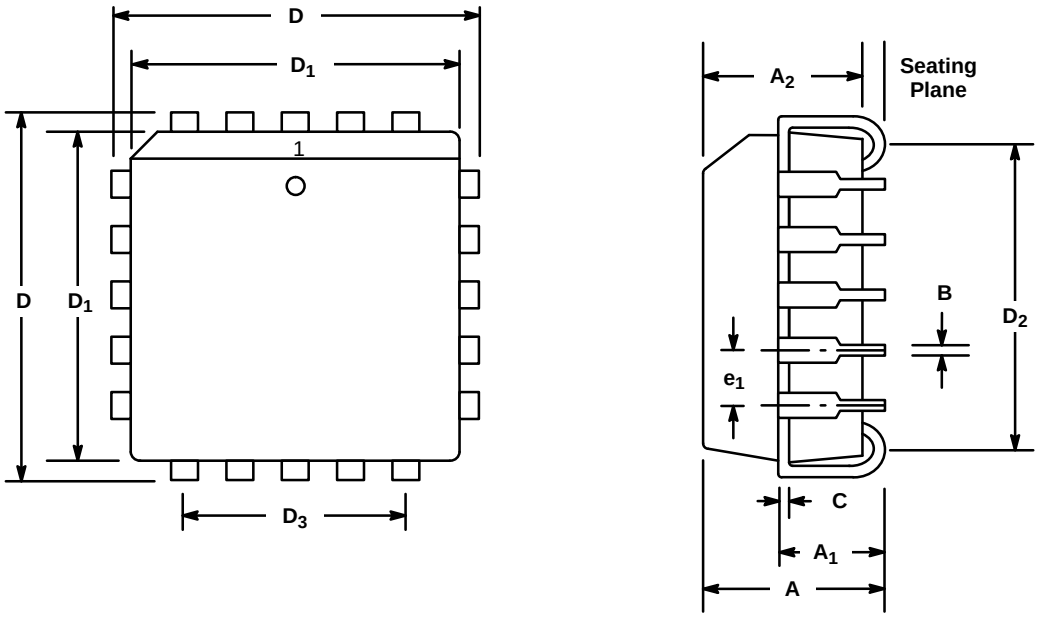
Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

20 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.642
A_1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.500	0.510	12.70	12.95
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

20 LEAD PLASTIC LEADED CHIP CARRIER (PLCC) P20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A_1	0.100	0.110	2.54	2.79
A_2	0.148	0.156	3.76	3.96
B	0.013	0.021	0.330	0.533
C	0.008	0.012	0.203	0.305
D	0.385	0.395	9.78	10.03
D_1 (1)	0.350	0.354	8.89	8.99
D_2	0.290	0.330	7.37	8.38
D_3	0.200 Ref		5.08 Ref.	
e_1	0.050 BSC		1.27 BSC	

Note: (1) Dimension D_1 does not include mold protrusion. Allowed mold protrusion is 0.254 mm/0.010 in.

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