AP1025BEN

45V Single Stepper Motor Driver IC

1. Description

The AP1025BEN provides a complete stepper motor driver solution with built-in LDMOS FET and its internal capacitors type charge pump circuit for the 45V & 1.6A constant current operation. Clock-in input mode and Parallel input mode is selectable by the setting of an external terminal. 2 phase, 1-2 phase(1/2step), W1-2 phase(1/4step) can be selected during parallel input mode, and 2 phase, 1-2 phase(1/2step), W1-2 phase(1/4step), 4W1-2 phase(1/16step) can be selected during clock-in input mode to realize calm motor operation. The IC is housed in a small 32-pin QFN package and excellent in heat dissipation. It also includes under voltage detection and thermal shut down circuits. It is suitable for various types of stepper motors.

2. Features

- Selectable input logic (Clock in input, Parallel input)
- Excitation mode is configurable
  - − Parallel input mode 2 phase, 1-2 phase(1/2step), W1-2 phase(1/4step)
  - − Clock-in input mode 2 phase, 1-2 phase(1/2step), W1-2 phase(1/4step), 4W1-2 phase(1/16step)
- Operating Temperature Range -30°C to +85°C
- Operating Voltage Range
  - − Control Power Supply Voltage (VC) 3.0V to 5.5V
  - − Motor Power Supply Voltage (VM) 9.0V to 45V
- Low H-Bridge On Resistance 0.85Ω@25°C
- Built-in UVLO (under voltage lockout circuit)
- Built-in TSD (thermal shut down circuit)
- Built-in charge pump circuit
- Built-in Sub-harmonic noise reduction function
- Built-in Phase Synchronous function
- Package 32-pin QFN (5.0mm□)

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4. Block Diagram

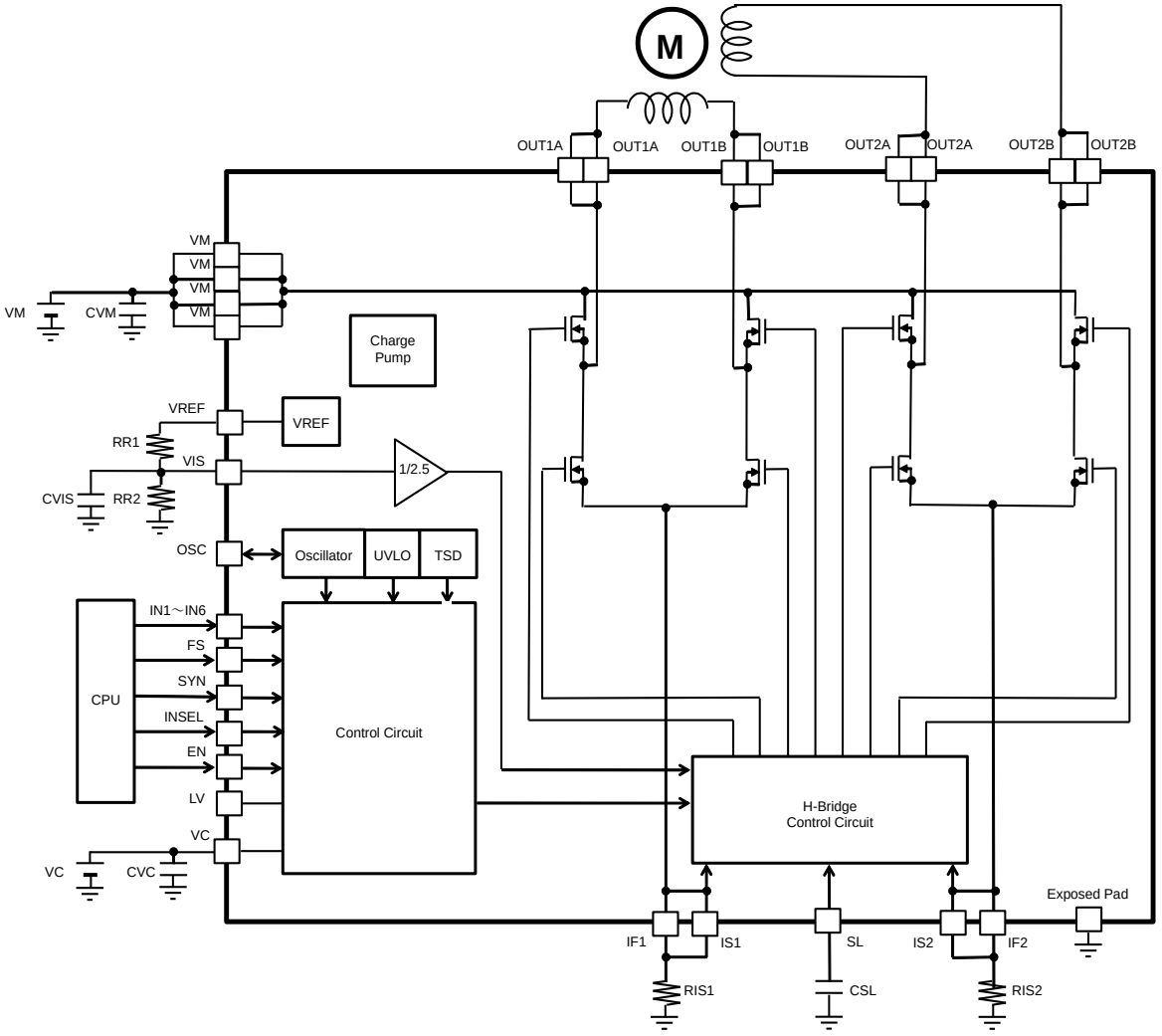


Figure 1. Block Diagram

5. Ordering Guide

AP1025BEN -30°C ～+85°C 32-pin QFN

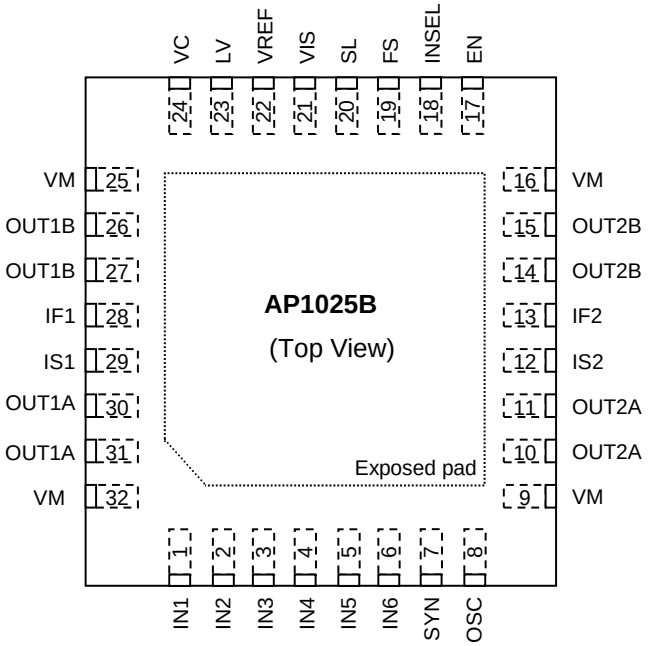
When AP1025AEN is replaced with AP1025BEN, note that the excitation mode(H,H) is changed as follows.

Table 1. Selection of the excitation mode

IN5	IN6	AP1025AEN	AP1025BEN
H	H	W1-2 phase (1/4step)	4W1-2 phase (1/16step)

6. Pin Configuration and Functions

■ Pin Configuration



■ Functions

No.	Pin Name	I/O	Function	Condition
1～6	IN1～IN6	I	Control signal input terminal	
7	SYN	I	Synchronic mode select input terminal	
8	OSC	I/O	Chopper frequency I/O terminal	
9,16,25,32	VM	P	Motor power supply terminal	
10,11	OUT2A	O	Motor driver output terminal	
12	IS2	I	Current sense terminal	
13	IF2	O	Current force terminal	
14,15	OUT2B	O	Motor driver output terminal	
17	EN	I	Enable signal input terminal	200kΩ pull-down
18	INSEL	I	Control logic select input terminal	
19	FS	I	Chopper frequency select terminal	
20	SL	I	Slope setting terminal	
21	VIS	I	Motor current setting terminal	
22	VREF	O	Reference voltage output terminal	
23	LV	O	Logic voltage output capacitor connection terminal	
24	VC	P	Control power supply terminal	
26,27	OUT1B	O	Motor driver output terminal	
28	IF1	O	Current force terminal	
29	IS1	I	Current sense terminal	
30,31	OUT1A	O	Motor driver output terminal	
-	Exposed Pad	P	Ground	

Note 1. I(Input terminal), O(Output terminal), P(Power terminal)
Note 2. Exposed Pad must be connected to GND.

7. Absolute Maximum Ratings

Parameter		Symbol	min	max	Unit	Condition
Control power supply voltage		VC	-0.5	5.5	V	
Motor power supply voltage		VM	-0.5	45	V	
VC level terminal (SL, EN, SYN, OSC, FS, INSEL, INn)		Vterm1	-0.5	VC	V	
VM level terminal (OUTnA, OUTnB)		Vterm2	-0.5	VM	V	
1.8V level terminal (LV, VREF, VIS)		Vterm3	-0.5	1.9	V	
1.2V level terminal (ISn, IFn)		Vterm4	-0.5	1.3	V	
Maximum DC output current		Iload	-	1.6	A	Ta=25°C (Note 6)
			-	1.2	A	Ta=85°C (Note 6)
Power dissipation		PD	-	3.9	W	Ta=25°C (Note 6)
			-	2.0	W	Ta=85°C (Note 6)
Junction temperature		Tj	-	150	°C	
Storage temperature		Tstg	-40	150	°C	
ESD rating	HBM	-	-	±2	kV	

Note 3. All above voltages are with respect to GND(Exposed Pad).
Note 4. Exposed Pad must be connected to GND.
Note 5. The each power supply of VC and VM is sequence-free.
Note 6. θJA=32°C/W with 4 layer board (JEDEC51).

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

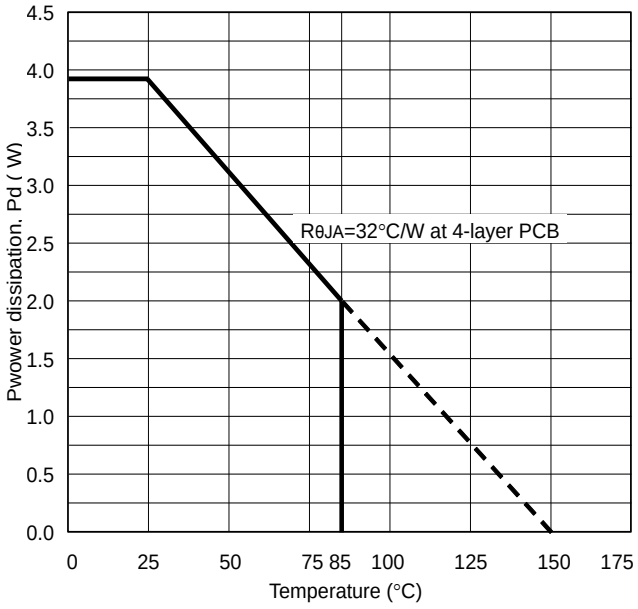


Figure 2. Maximum power dissipation

8. Recommended Operation Conditions

Parameter	Symbol	min	typ	max	Unit	Condition
Motor power supply voltage	VM	9.0	24.0	45.0	V	
Control power supply voltage	VC	3.0	5.0	5.5	V	
VIS input voltage range	VIS	0.2	-	V_{REF}	V	Iload(100%)[A]=(VIS/2.5)/RISn
Clock in input frequency	FCL	-	-	20	kHz	
Operating Temperature range	Ta	-30	-	85	°C	

Note 7. All above voltages are with respect to GND(Exposed Pad).

9. Electric Characteristics

(Ta = 25°C, VM=24V, VC = 5.0V, unless otherwise specified.)

Parameter	Symbol	Condition	min	typ	max	Unit
Quiescent current						
VC Quiescent current at OFF	I_{VCOFF}	EN="L"	-	-	10	μA
VM Quiescent current at OFF	I_{VMOFF}	EN="L"	-	-	20	μA
VC Quiescent current at operate	I_{VC}	EN="H", INSEL="H", SYN="L", FS="L", IN1=1kHz	-	1.7	2.8	mA
H-bridge circuit						
Driver on resistance (High side + Low side)	R_{ON1}	Iload 1ch/2ch=0.1A/0.1A Ta = 25°C	-	0.85	1.0	Ω
		Iload 1ch/2ch=0.1A/0.1A Ta = 25°C、VC=3.0V	-	1.0	1.5	Ω
	R_{ON2}	Iload 1ch/2ch= 1.1A / 0A or 0.8A / 0.8A Ta = 85°C (Note 9)	-	1.0	1.5	Ω
		I Iload 1ch/2ch= 1.1A / 0A or 0.8A / 0.8A Ta = 85°C (Note 9)	-	1.5	2.0	Ω
Body diode forward voltage	V_F	I_F = 100mA	-	0.8	1.2	V
Control logic						
High level input voltage	V_{IH}	VC = 3.0V-5.5V	0.7xVC	-	-	V
Low level input voltage	V_{IL}		-	-	0.3xVC	V
Input pulse rise time	t_R		-	-	1.0	μs
Input pulse fall time	t_F		-	-	1.0	μs
High level input current	I_{IH}	without EN terminal	-1.0	-	1.0	μA

Parameter	Symbol	Condition	min	typ	max	Unit
High level input current	I_{IHEN}	EN terminal	15	25	40	μA
Low level input current	I_{IL}		-1.0	-	1.0	μA
Reference voltage						
VREF terminal voltage	V_{REF}	R1+R2=12k+47k Ω	1.22	1.25	1.28	V
VREF terminal current	I_{VREF}		-	-	100	μA
Current operation						
Blanking time	t_B		2.0	2.23	2.6	μs
VIS offset voltage	V_{OSIS}		-50	0	50	mV
SL terminal output current	I_{SL}		-	50	-	μA
OSC terminal frequency 1	f_{CPL}	FS="L", SYN="L"	20	25	30	kHz
OSC terminal frequency 2	f_{CPH}	FS="H", SYN="L"	40	50	60	kHz
OSC terminal High level output voltage	V_{CPOH}	SYN="L", Iload=100μA	VC-0.1	-	-	V
OSC terminal Low level output voltage	V_{CPOL}	SYN="L", Iload=-100μA	-	-	0.1	V
OSC terminal frequency input range	f_{CPIN}	SYN="H"	20	-	60	kHz
OSC terminal input voltage range	V_{CPIN}	SYN="H"	0	-	VC	V
OSC terminal High level input voltage	V_{CPIH}	SYN="H"	0.7xVC	-	-	V
OSC terminal Low level input voltage	V_{CPIL}	SYN="H"	-	-	0.3xVC	V
Protection circuit						
VC under voltage detect voltage	V_{VCUV}		1.9	2.2	2.5	V
Thermal shut down temperature	T_{TSD}	Guaranteed by Design (Note 9)	150	175	200	°C
Temperature hysteresis	T_{TSDHYS}	Guaranteed by Design (Note 9)	-	30	-	°C

Note 8. All above voltages are with respect to GND.
Note 9. Not tested in production.

10. Functional Description

10.1 Input terminal and protection circuit

■ Common description (Parallel input mode and Clock-in input mode)

Table 2. Internal circuit operation by the ENABLE(EN) signal

EN pin	UVLO	TSD	Reference Voltage Circuit	H-Bridge
H	L	L	ON	Output
		H	ON	Hi-Z
	H	-	OFF	Hi-Z
L	-	-	OFF	Hi-Z

Note 10. UVLO, TSD and Reference Voltage Circuit show internal status. "-" is Don't Care.

Table 3. Selection of the chopper frequency by the SYN signal

SYN pin	FS pin	OSC pin	PWM chopper frequency
L	L	Output	25kHz(typ)
	H		50kHz(typ)
H	-	Input	External frequency

Note 11. Do not change input level of the SYN and FS pin during operation. "-" is Don't Care.

Table 4. Selection of the chopper frequency by the INSEL signal

INSEL	Input Mode
L	Parallel input mode. H-Bridge is controlled by input logic. Excitation mode : 2phase, 1-2phase(1/2step), W1-2phase(1/4step)
H	Clock-in input mode. H-Bridge is controlled by the count number of the clock. Excitation mode : 2phase, 1-2phase(1/2step), W1-2phase(1/4step), 4W1-2phase(1/16step)

Note 12. Do not change input level of the INSEL terminal during operation.

10.2 Parallel input mode (INSEL="L")

Table 5. Parallel input mode truth table

IN1	IN2	IN3	IN4	OUT1A	OUT1B	IS1	OUT2A	OUT2B	IS2
L	L	L	L	H	L	100%	Hi-Z	Hi-Z	0%
L	L	L	H			93%	H	L	38%
L	L	H	H			71%			71%
L	L	H	L			38%			93%
L	H	L	L	Hi-Z	Hi-Z	0%			100%
L	H	L	H	L	H	38%			93%
L	H	H	H			71%			71%
L	H	H	L			93%			38%
H	H	L	L			100%	Hi-Z	Hi-Z	0%
H	H	L	H			93%	L	H	38%
H	H	H	H			71%			71%
H	H	H	L			38%			93%
H	L	L	L	Hi-Z	Hi-Z	0%			100%
H	L	L	H	H	L	38%			93%
H	L	H	H			71%			71%
H	L	H	L			93%			38%

Note 13. The IN5 and IN6 pins are not used in Parallel input mode. They must be connected to ground.

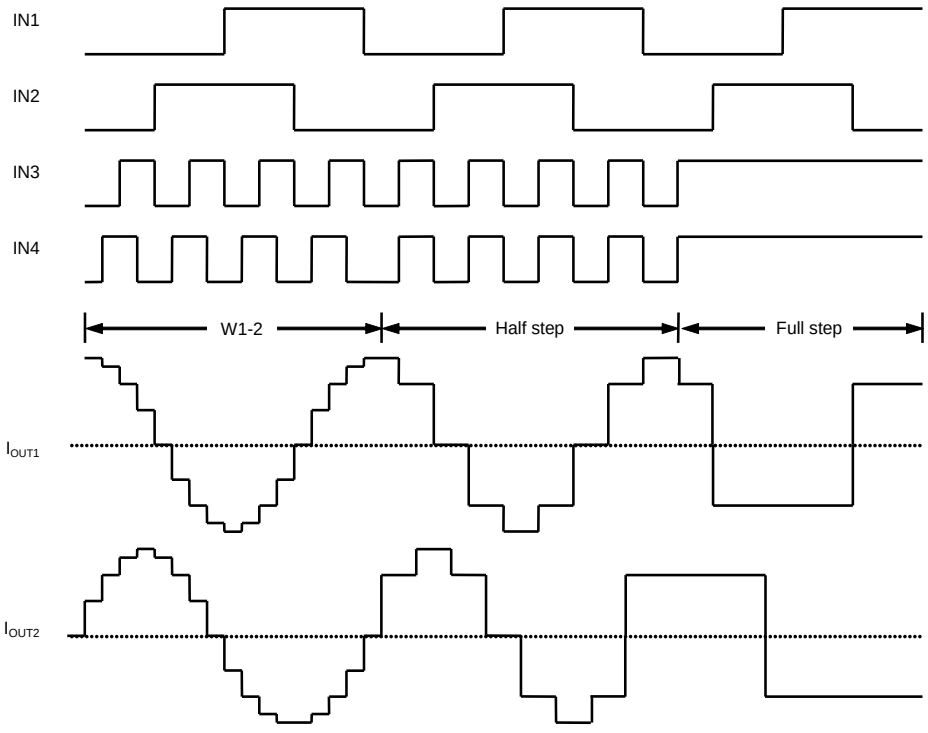


Figure 3. Input signal (Parallel input mode)

10.3 Clock-in input mode (INSEL="H")

Table 6. Clock-in input mode truth table

IN1	IN2	IN3	IN4	Condition
↑	L	L	-	Step +1(CW)
↑	H	L	-	Step -1(CCW)
↑	-	H	-	Reset
-	-	-	H	Output
-	-	-	L	Hi-Z

Note 14. "-" is Don't Care. " ↑ " shows the rising edge.

Table 7. Selection of the excitation mode

IN5	IN6	Step
L	L	W1-2 phase (1/4step)
L	H	1-2 phase (1/2step)
H	L	Full step
H	H	4W1-2 phase (1/16step)

Note 15. Do not change input level of the IN5 and IN6 terminals during operation.

■ ISn terminal current revel

Table 8. Set current ratio at each excitation mode

2 phase	1-2 phase (1/2step)	W1-2 phase (1/4step)	4W1-2 phase (1/16step)	Phase1 Current [%]	Phase2 Current [%]	Step Angle [°]
	0	0	0	100	0.00	0.0
			1	99.61	9.80	5.6
			2	98.04	19.61	11.3
			3	96.69	29.02	16.9
		1	4	92.55	38.43	22.6
			5	88.24	47.06	28.1
			6	83.14	55.69	33.8
			7	77.25	63.53	39.4
0	1	2	8	70.59	70.59	45.0
			9	63.53	77.25	50.6
			10	55.69	83.14	56.2
			11	47.06	88.24	61.9
		3	12	38.43	92.55	67.4
			13	29.02	95.69	73.1
			14	19.61	98.04	78.7
			15	9.80	99.61	84.4
	2	4	16	0.00	100	90.0
			17	-9.80	-99.61	95.6
			18	-19.61	-98.04	101.3
			19	-29.02	-95.69	106.9
		5	20	-38.43	-92.55	112.6
			21	-47.06	-88.24	118.1
			22	-55.69	-83.14	123.8
			23	-63.53	-77.25	129.4
1	3	6	24	-70.59	-70.59	135.0
			25	-77.25	-63.53	140.6
			26	-83.14	-55.69	146.2

			27	-88.24	-47.06	151.9
		7	28	-92.55	-38.43	157.4
			29	-95.69	-29.02	163.1
			30	-98.04	-19.61	168.7
			31	-99.61	-9.80	174.4
	4	8	32	-100	0.00	180.0
			33	-99.61	-9.80	185.6
			34	-98.04	-19.61	191.3
			35	-96.69	-29.02	196.9
		9	36	-92.55	-38.43	202.6
			37	-88.24	-47.06	208.1
			38	-83.14	-55.69	213.8
			39	-77.25	-63.53	219.4
2	5	10	40	-70.59	-70.59	225.0
			41	-63.53	-77.25	230.6
			42	-55.69	-83.14	236.2
			43	-47.06	-88.24	241.9
		11	44	-38.43	-92.55	247.4
			45	-29.02	-95.69	253.1
			46	-19.61	-98.04	258.7
			47	-9.80	-99.61	264.4
	6	12	48	0.00	100	270.0
			49	9.80	-99.61	275.6
			50	19.61	-98.04	281.3
			51	29.02	-95.69	286.9
		13	52	38.43	-92.55	292.6
			53	47.06	-88.24	298.1
			54	55.69	-83.14	303.8
			55	63.53	-77.25	309.4
3	7	14	56	70.59	-70.59	315.0
			57	77.25	-63.53	320.6
			58	83.14	-55.69	326.2
			59	88.24	-47.06	331.9
		15	60	92.55	-38.43	337.4
			61	95.69	-29.02	343.1
			62	98.04	-19.61	348.7
			63	99.61	-9.80	354.4
			64	100	0.00	360.0

: Home microstep position at Step Angle 45˚

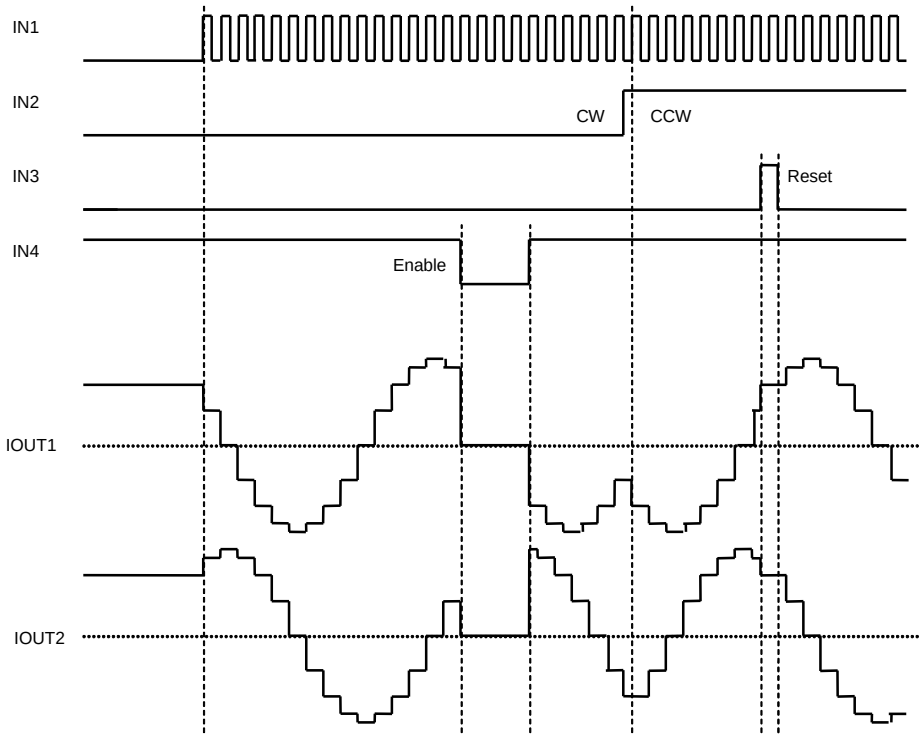


Figure 4. Input signal (Parallel input mode, IN5=”L”, IN6=”L”)

10.4 PWM Current Control

The current value of 100% PWM constant current setting ratio at each excitation mode of AP1025 (Iload (100%) [A]) is determined by H-Bridge sense resistor(RIS) and PWM constant current setting voltage(VIS) as follows.

$$Iload\ (100\%)[A] = (VIS / 2.5) / RIS \quad \text{--- (1)}$$

PWM constant current setting voltage	VIS
VIS damping ratio	1/2.5
H-Bridge sense resistor	RIS

Calculation example1 : VIS=1V, RIS=0.5ohm

$$Iload\ (100\%)[A] = (1 / 2.5) / 0.5ohm = 0.8A \quad \text{--- (2)}$$

The minimum value of the control current in the PWM constant current control in each excitation mode (Iload (min) [A]) is determined by the following equation.

$$Iload(min)[A]=VM/(Rm+R_{ON}+RIS) \times t_B \times f_{CP} \quad \text{--- (3)}$$

Motor power supply voltage	VM
OSC frequency	f_{CP} (f_{CPL}/ f_{CPH})
Blanking time	t_B
Motor on resistance	R_m
H-Bridge on resistance	R_{ON}
H-Bridge sense resistor	RIS

Calculation example2 : VM=24V, f_{CP}=25kHz, t_B=2.23us, R_m=9.4ohm, R_{ON}=1ohm, RIS=1ohm

$$Iload(min)[A]=24V/(9.4ohm+1ohm+1ohm) \times 2.23us \times 25kHz = 0.117A \quad \text{--- (4)}$$

The current value of 100% PWM constant current setting ratio should be set so that the minimum control current (Iload (min) [A]) becomes larger than the minimum value of the PWM constant current setting ratio in 4W1-2 phase excitation. In case of calculation example 2, the current value of the 100% PWM constant current setting ratio (Iload (100%) [A]) is as follows.

$$Iload(100\%)[A]=0.117/9.8\%=1.19A \quad \text{---(5)}$$

If the current value of 100% PWM constant current setting value ratio (Iload (100%) [A]) is smaller than equation (5), minimum control current value (Iload (min) [A]) may be larger than 9.8%.

10.5 Decay Mode

The AP1025 selects decay mode automatically for better current following property. Basically, it operates in slow decay mode, but it operates in fast decay mode when the current setting value is lowered, till it reaches to the setting value.

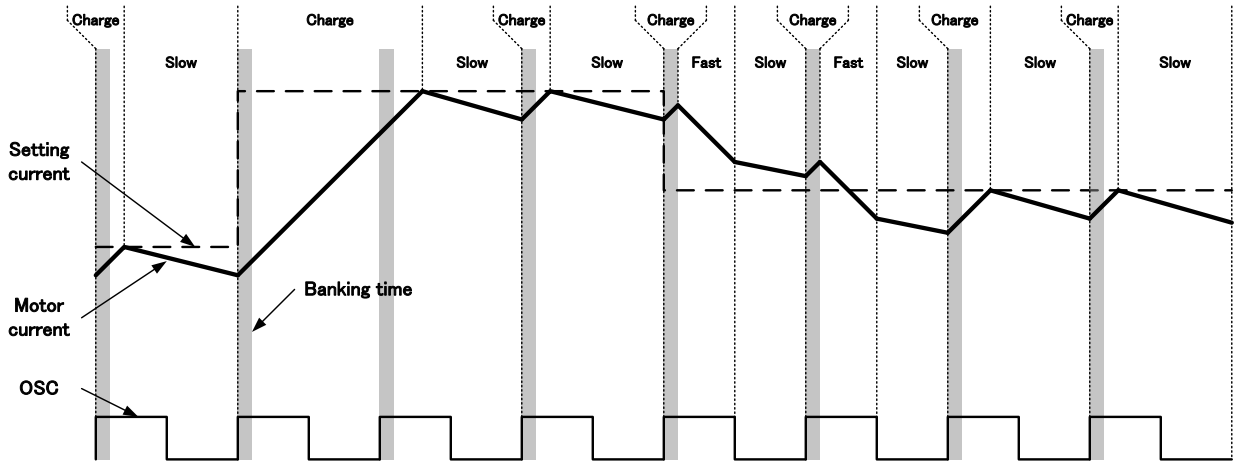


Figure 5. Current waveform image during decay mode

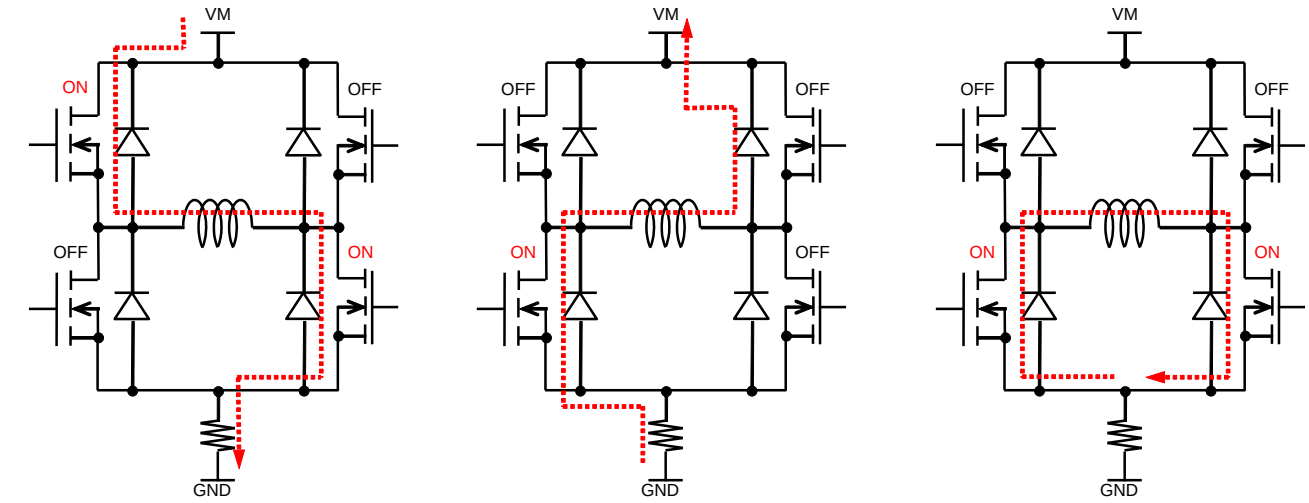


Figure 6. Decay Mode Image

10.6 Protection Circuits

・ Under Voltage Lockout Circuit (UVLO)

UVLO monitors Control power supply voltage (VC) and changes H-bridge driver output to Hi-Z if VC is lower than the specified value (V_{VCUV} =2.2V) when starting the VC source.

・ Thermal Shut Down Circuit(TSD)

As soon as abnormal high temperature (T_{TSD}=150°C) is detected, H-Bridge driver output becomes Hi-Z.

Table 9. Recovery type of abnormal heat generation detect circuit

Interface Mode	Recovery type
Parallel input	Automatic
Clock-in input	Latch

■ Parallel Input Mode

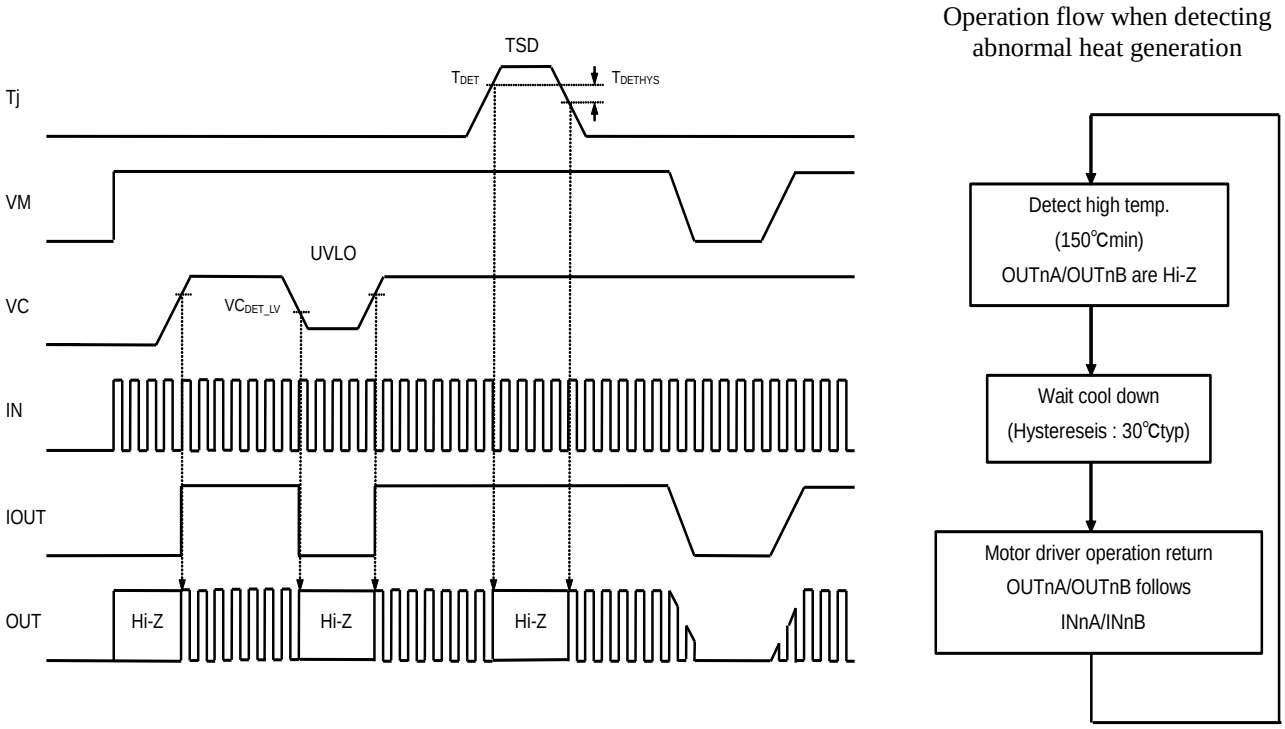
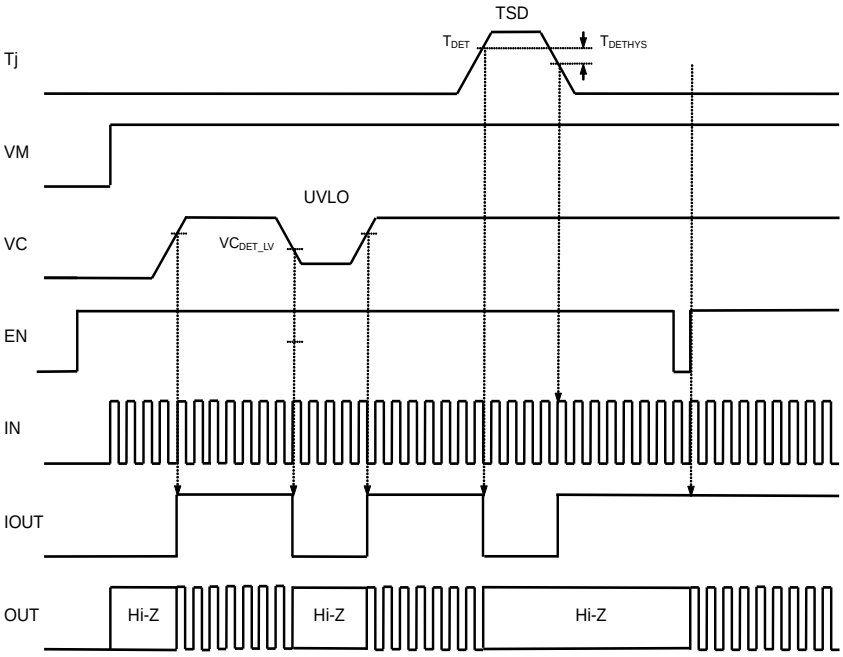


Figure 7. Timing Chart of the protection circuits (parallel input mode)

■ Clock-in input mode



Operation flow when detecting abnormal heat generation

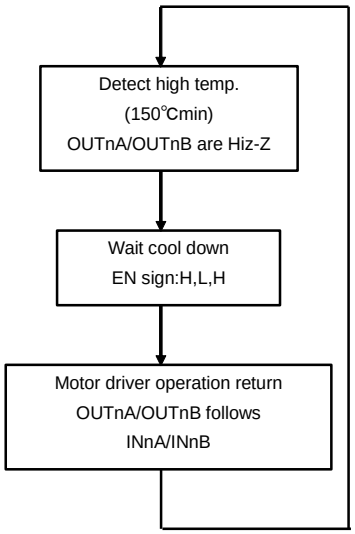


Figure 8. Timing chart of the Protection circuit (parallel input mode)

・Shorted-Load, Shorted-to-Ground and Shorted-to-Power Protection

If the motor leads are shorted together, or if one of the leads is shorted to ground or shorted to power, when current flowing is 3.3A or less, the motor driver IC will protect itself by hiccup behavior of thermal shutdown circuit (TSD). When there is a power supply capacity of 3.3A or more, the appropriate protection fuse is implemented between the motor power supply line(VM) and the power supply on the PCB.

11. Recommended External Circuit

■ **External circuit**

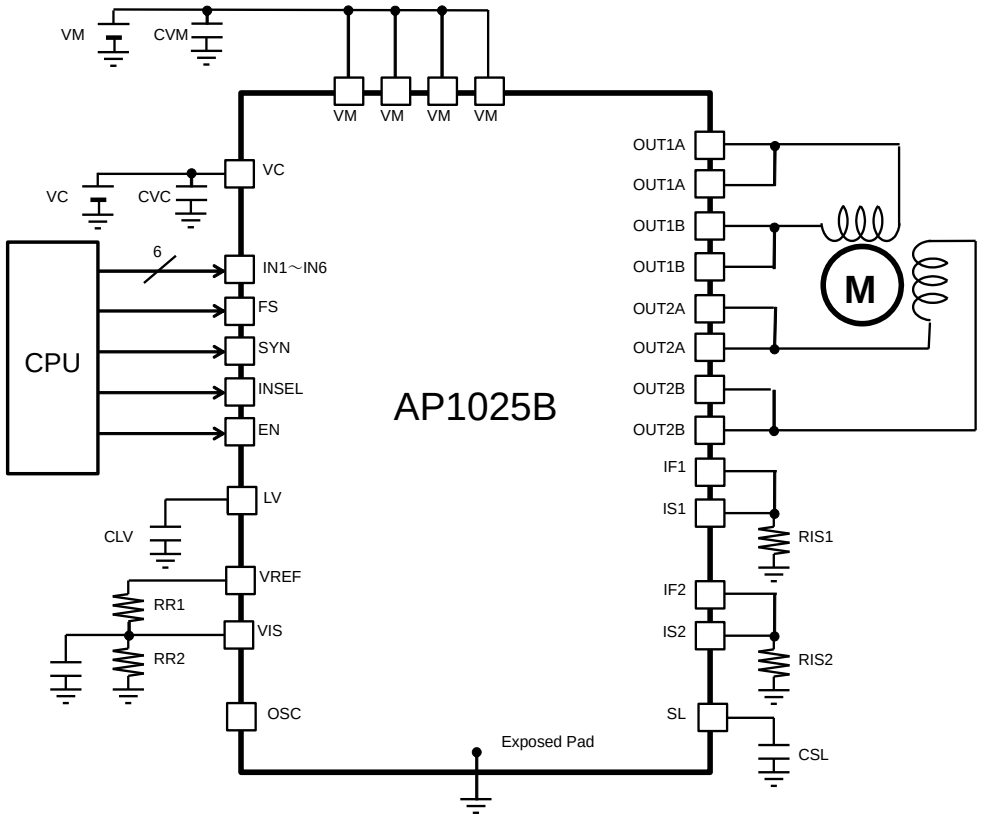


Figure 9. External Circuit Example

Table 10. Recommended external components

Items	min	typ	max	Unit	Remark
CVM	- -	47 1	- -	μF μF	Electrolytic Capacitor Ceramic Capacitor
CVC	-	1.0	-	μF	
CLV	0.68	1.0	1.5	μF	
CSL	0.001	-	0.01	μF	
CVIS	-	1.0	-	μF	
RISn	-	500	-	mΩ	Iload(100%)=0.8A
R1	-	12	-	kΩ	
R2	-	47	-	kΩ	

Note 16. Above capacitances are examples. Please choose the best external capacitors for CVM, CVC and CVIS for your system board.

Note 17. Capacitance of CVM and CVC should be adjusted considering the load current profile, the load capacitance, the line resistance and etc. of the actual system board.

Note 18. Please choose the best external capacitor for CSL as sub harmonic noise measures. If not using the CSL capacitor, please connect the SL terminal to ground.

■ Recommended Layout Example

Top View Bottom View

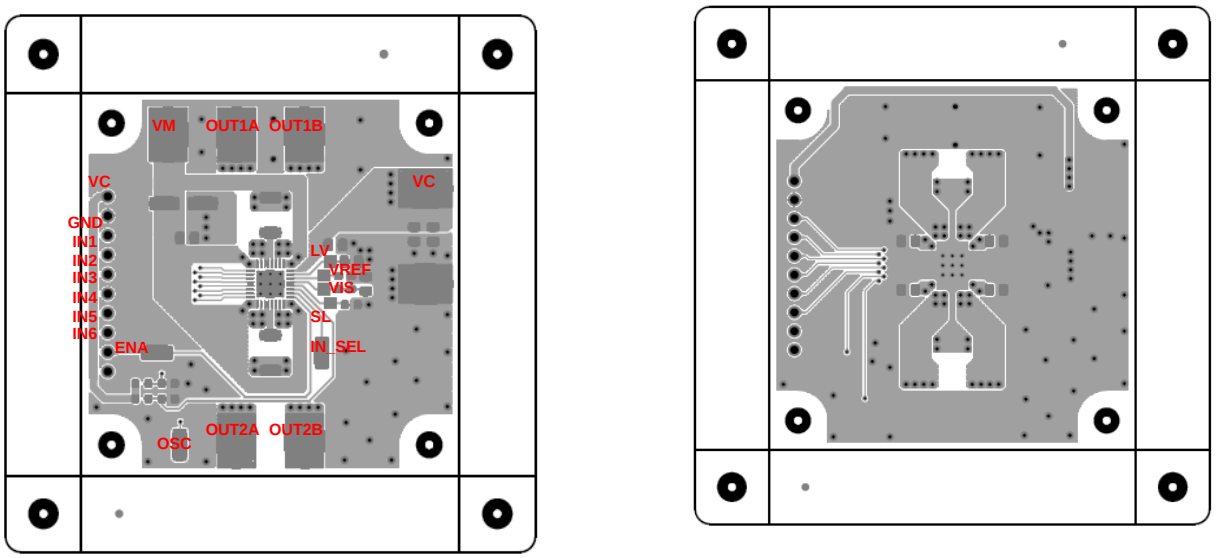


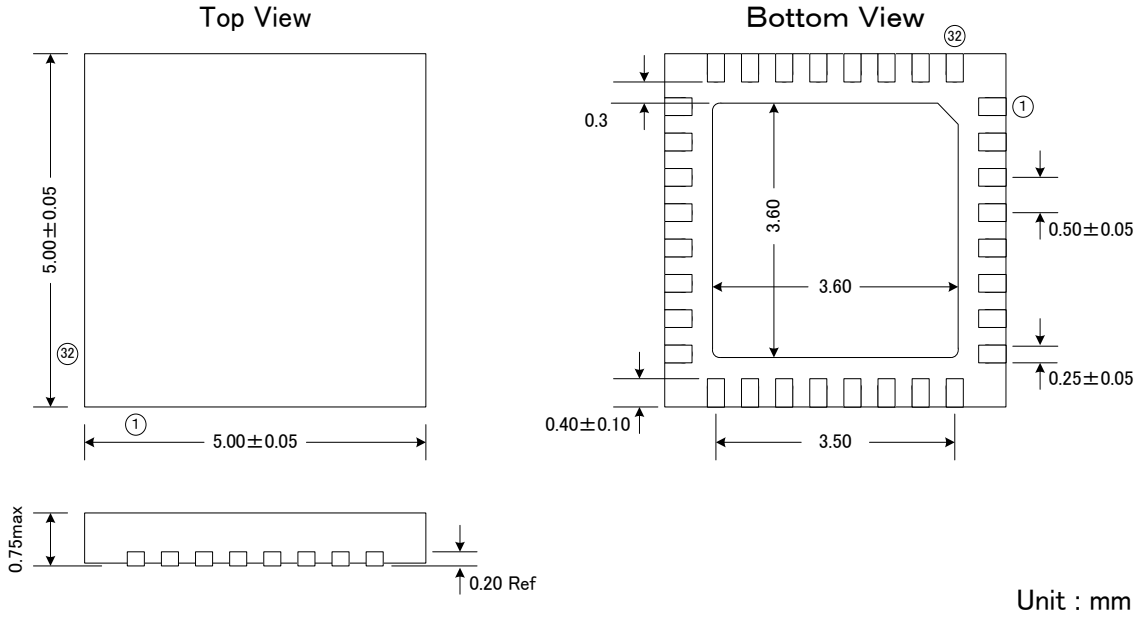
Figure 10. Layout pattern example

Note 19. Please design the ground plane of the PCB as large as possible.
Note 20. Exposed Pad (exposed backside pad) must be connected to the ground of the PCB, because the ground of IC and Exposed pad is in common.
Note 21. The ground via on the IC mounted area is effective for heat radiation to each layer of the PCB.

12. Package

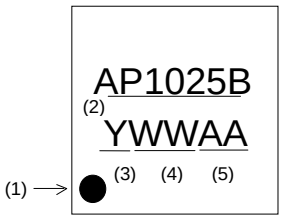
■ Outline Dimensions

・32-pin QFN package



Unit : mm

■ Marking



(1) 1pin Indication
(2) Market No.
(3) Year code (last 1 digit)
(4) Week code
(5) Management code

13. Revise History

Date (YY/MM/DD)	Revision	Page	Contents
15/01/09	00	-	First Edition

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