Data Sheet

VSC8111

ATM/SONET/SDH 155/622 Mb/s Transceiver
Mux/Demux with Integrated Clock Generation

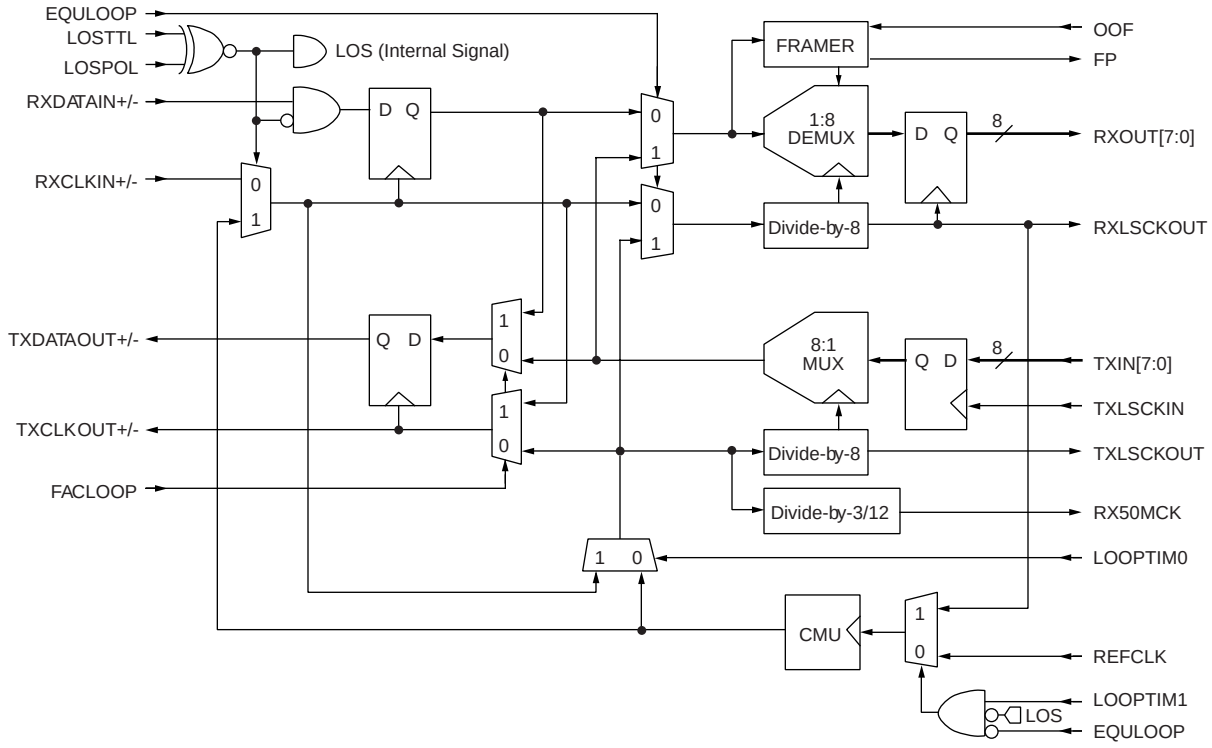
Features

- Operates at Either STS-3/STM-1 (155.52 Mb/s) or STS-12/STM-4 (622.08 Mb/s) Data Rates
- Compatible with Industry ATM UNI Devices
- On Chip Clock Generation of the 155.52 Mhz or 622.08 Mhz High Speed Clock
- Dual 8 Bit Parallel TTL Interface
- SONET/SDH Frame Detection and Recovery
- Loss of Signal (LOS) Control
- Provides Equipment, Facilities and Split Loop-back Modes as well as Loop Timing Mode
- Meets Bellcore, ITU and ANSI Specifications for Jitter Performance
- Single 3.3V Supply Voltage
- Low Power - 1.4 Watts Maximum
- 100 PQFP Package

General Description

The VSC8111 is an ATM/SONET/SDH compatible transceiver integrating an on-chip clock multiplication unit (PLL) for the high speed clock and 8 bit serial-to-parallel and parallel-to-serial data conversion. The high speed clock generated by the on-chip PLL is selectable for 155.52 or 622.08 MHz operation. The demultiplexer contains SONET/SDH frame detection and recovery. In addition, the device provides both facility and equipment loopback modes and two loop timing modes. The part is packaged in a 100 PQFP with an integrated heat spreader for optimum thermal performance and reduced cost. The VSC8111 provides an integrated solution for ATM physical layers and SONET/SDH systems applications.

VSC8111 Block Diagram



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Functional Description

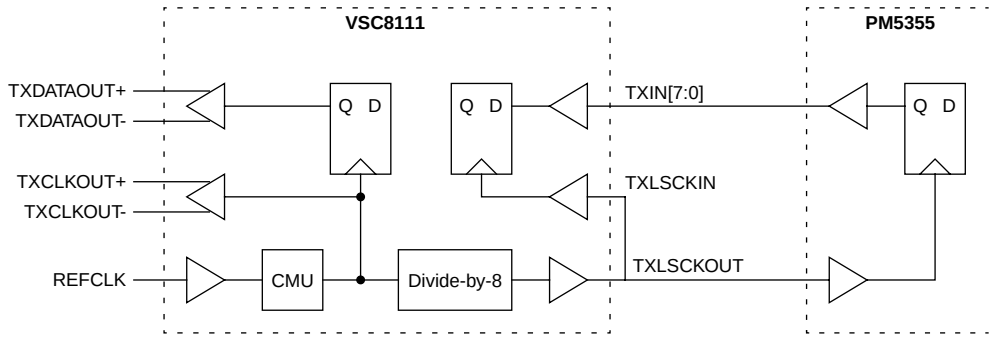
The VSC8111 is designed to provide a SONET/SDH compliant interface between the high speed optical networks and the lower speed User Network Interface (UNI) devices such as the PM5355 S/UNI-622 (or PM5312 STTX). The VSC8111 transmit section converts 8 bit parallel data at 77.76 Mb/s or 19.44 Mb/s to a serial bit stream at 622.08 Mb/s or 155.52 Mb/s, respectively. It also provides a Facility Loopback function which loops the received high speed data and clock directly to the transmit outputs. A Clock Multiplier Unit (CMU) is integrated into the transmit circuit to generate the high speed clock for the serial output data stream from input references frequency of 19.44, 38.88, 51.84 or 77.76 MHz. The CMU can be bypassed by using the receive clock in loop timing mode thus synchronizing the entire part to a single clock (RXCLKIN).

The receive section provides the serial-to-parallel conversion, converting 155 Mb/s or 622 Mb/s to an 8 bit parallel output at 19.44 Mb/s or 77.76 Mb/s, respectively. The receive section provides an Equipment Loopback function which will loop the low speed transmit data and clock back through the receive section to the 8 bit parallel data bus and clock outputs. The receive section also contains a SONET/SDH frame detector circuit which is used to provide frame recovery in the serial to parallel converter. The block diagram on page 1 shows the major functional blocks associated with the VSC8111.

Transmit Section

Byte-wide data is presented to TXIN [7:0] and is clocked into the part on the rising edge of TXLSCKIN (refer to Figure 1). The data is then serialized (MSB leading) and presented at the TXDATAOUT+/- pins. TXDATAOUT is clocked out on the falling edge of TXCLKOUT+. The serial output stream is synchronized to the CMU generated clock which is a phase locked and frequency scaled version of the input reference clock. External control inputs B0-B2 and STS12 select the multiply ratio of the CMU and either STS-3 (155 Mb/s) or STS-12 (622 Mb/s) transmission (See Table 2). A divide-by-8 version of the CMU clock (TXLSCKOUT) should be used to synchronize the transmit interface of the UNI device to the transmit input registers on the VSC8111. (See Application Notes, Pg. 22)

Figure 1: Data and Clock Transmit Block Diagram



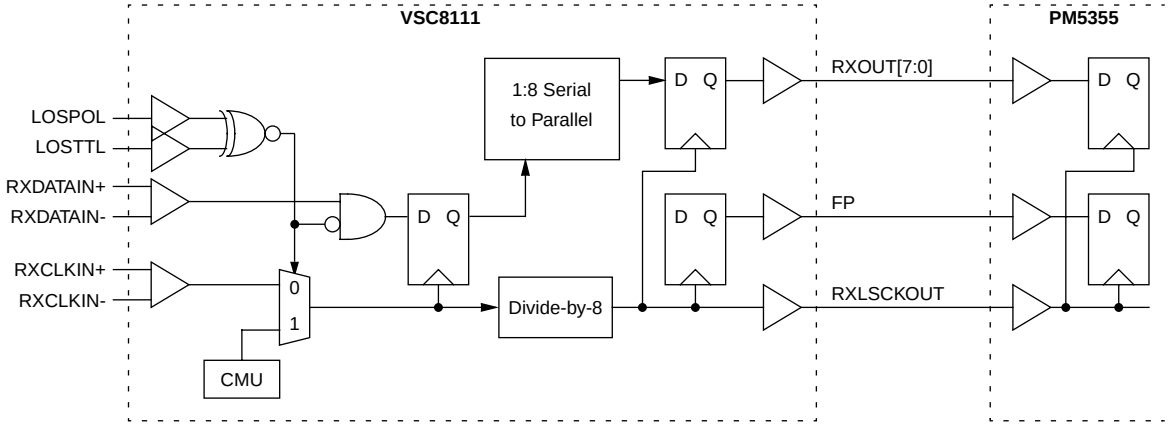
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Receive Section

High speed Non-Return to Zero (NRZ) serial data at 155Mb/s or 622Mb/s are received by the RXDATAIN inputs. RXDATAIN is clocked in on the rising edge of RXCLKIN+. See Figure 2. The serial data is converted to byte-wide parallel data and presented on RXOUT[7:0] pins. A divide-by-8 version of the high-speed clock (RXLSCKOUT) should be used to synchronize the byte-serial RXOUT[7:0] data with the receive portion of the UNI device.

The receive section also includes frame detection and recovery circuitry which detects the SONET/SDH frame, aligns the received serial data on byte boundaries, and initiates a frame pulse on FP coincident with the byte aligned data. The frame recovery is initiated when OOF is held high which must occur at least 4 byte clock cycles before the A1A2 boundary. The OOF input control is a level-sensitive signal, and the VSC8111 will continually perform frame detection and recovery as long as this pin is held high even if 1 or more frames has been detected. Frame detection and recovery occurs when a series of three A1 bytes followed by three A2 bytes has been detected. The parallel output data on RXOUT[7:0] will be byte aligned starting on the third A2 byte. When a frame is detected, a single byte clock period long pulse is generated on FP which is synchronized with the byte-aligned third A2 byte on RXOUT[7:0]. The frame detector sends an FP pulse only if OOF is high or if a frame was detected while OOF was being pulled low.

Figure 2: Data and Clock Receive Block Diagram



Loss of Signal

During a LOS condition, the VSC8111 forces the receive data low which is an indication for any downstream equipment that an optical interface failure has occurred. The receive section is clocked by the transmit section's

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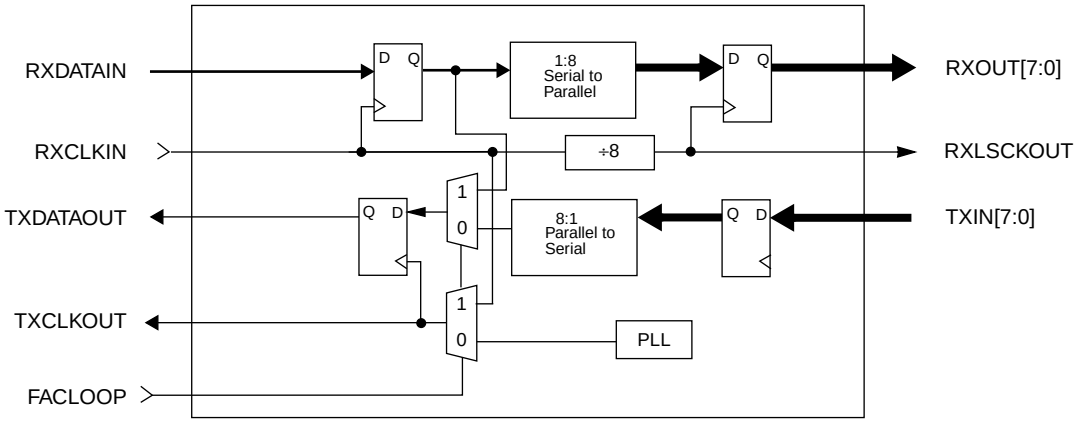
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PLL clock multiplier. The VSC8111 has two TTL inputs LOSTTL and LOSPOL one to force the part into a Loss of Signal state, the other to control the polarity. The LOSTTL and LOSPOL inputs are XNOR'd to generate an internal LOS control signal. See Figure 2. Optics have either a PECL or TTL output, usually called "SD" (Signal Detect) or "FLAG" indicating either a lack of or presence of optical power. Depending on the optics manufactured this signal is either active high or active low polarity. If the optics Signal Detect or FLAG output is a "TTL" signal it should be connected to LOSTTL. If it's a "PECL" signal it should be connected through a "PECL" to "TTL" translator (such as the Motorola "MC100ELT21") which then drives LOSPOL. The LOSTTL input should be tied low if the optics "SD" or FLAG output is active high. If it's active low tie LOSTTL high. Note: LOSPOL and LOSTTL are interchangeable. The follow on part to VSC8111 is the VSC8113, in this device the signal LOSPOL has been changed to LOSPECL a PECL input, which is why LOSTTL is being used as the polarity control input.

Facility Loopback

The Facility Loopback function is controlled by the FACLOOP signal. When the FACLOOP signal is set high, the Facility Loopback mode is activated and the high speed serial receive data (RXDATAIN) is presented at the high speed transmit output (TXDATAOUT). See Figure 3. In addition, the high speed receive clock input (RXCLKIN) is selected and presented at the high speed transmit clock output (TXCLKOUT). In Facility Loopback mode the high speed receive data (RXDATAIN) is also converted to parallel data and presented at the low speed receive data output pins (RXOUT [7:0]). The receive clock (RXCLKIN) is also divided down and presented at the low speed clock output (RXLSCKOUT).

Figure 3: Facility Loopback Data Path



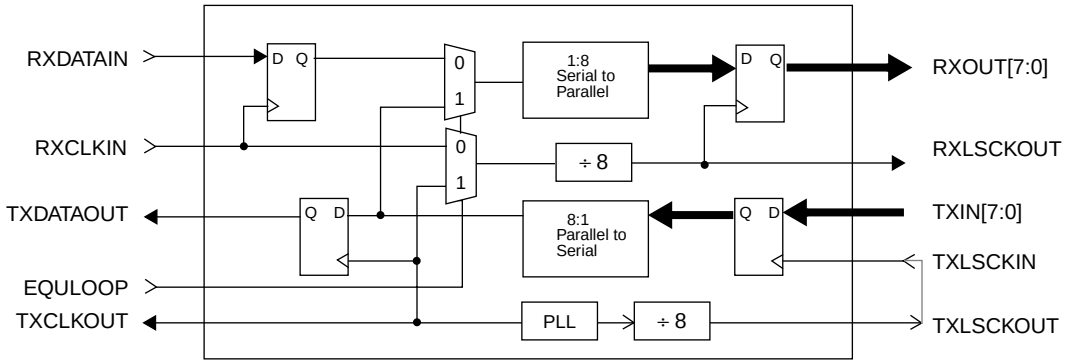
Equipment Loopback

The Equipment Loopback function is controlled by the EQULOOP signal. When the EQULOOP signal is set high, the Equipment Loopback mode is activated and the high speed transmit data generated from the paral-

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lel to serial conversion of the low speed data (TXIN [7:0]) is selected and converted back to parallel data in the receiver section and presented at the low speed parallel outputs (RXOUT [7:0]). See Figure 4. The internally generated 155MHz/622MHz clock is used to generate the low speed receive clock output (RXLSCKOUT). In Equipment Loopback mode the transmit data (TXIN [7:0]) is serialized and presented at the high speed output (TXDATAOUT) along with the high speed transmit clock (TXCLKOUT) which is generated by the on board clock multiplier unit.

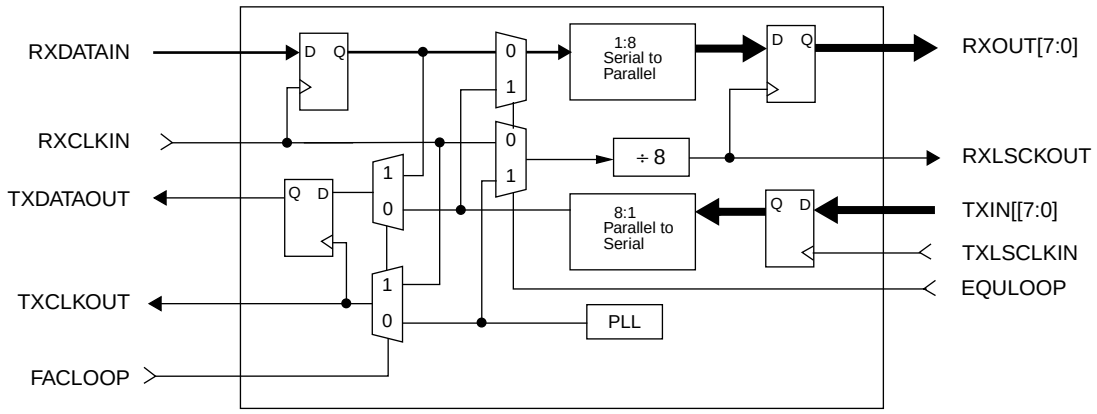
Figure 4: Equipment Loopback Data Path



Split Loopback

Equipment and facility loopback modes can be enabled simultaneously. See descriptions for equipment and facility loop modes above. The only change is, since they are both active, RXDATAIN will not be deserialized and presented to RXOUT[0:7] and TXIN[0:7] will not be serialized and present to TXDATAOUT.

Figure 5: Split Loopback Datapath



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Loop Timing

LOOPTIM0 mode bypasses the CMU when the LOOPTIM0 input is asserted high. In this mode the CMU is bypassed by using the receive clock (RXCLKIN), and the entire part is synchronously clocked from a single external source.

LOOPTIM1 mode bypasses the REFCLK input and uses the divide-by-8 version of the receive clock as the reference input to the CMU. This mode is selected by asserting the LOOPTIM1 input high. The part is forced out of this mode if it is in the Loss of Signal state or in Equipment Loopback to prevent the CMU from feeding its own clock back. The user needs to set the B[0:2] inputs to select 78MHz operation to match the RXLSCK-OUT frequency.

Clock Multiplier Unit

The VSC8111 uses an integrated phase-locked loop (PLL) for clock synthesis of the 622MHz high speed clock used for serialization in the transmitter section. The PLL is comprised of a phase-frequency detector (PFD), an integrating operation amplifier and a voltage controlled oscillator (VCO) configured in classic feedback system. The PFD compares the selected divided down version of the 622MHz VCO (select pins B0-B2 select divide-by ratios of 8, 12, 16 and 32, see Table 2) and the reference clock. The integrator provides a transfer function between input phase error and output voltage control. The VCO portion of the PLL is a voltage controlled ring-oscillator with a center frequency of 622MHz.

The reactive elements of the integrator are located off-chip and are connected to the feedback loop of the amplifier through the CP1, CP2, CN1 and CN2 pins. The configuration of these external surface mounted capacitors is shown in Figure 6. Table 1 shows the recommended external capacitor values for the configurable reference frequencies.

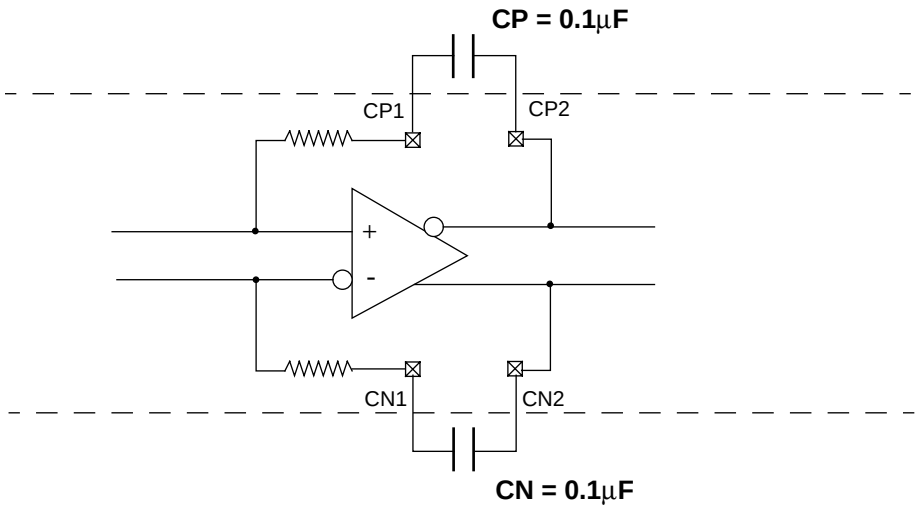
Good analog design practices should be applied to the board design for these external components. Tightly controlled analog ground and power planes should be provided for the PLL portion of the circuitry. The dedicated PLL power (VDDANA) and ground (VSSANA) pins should have quiet supply planes to minimize jitter generation within the clock synthesis unit. This is accomplished by either using a ferrite bead or a C-L-C choke (π filter) on the (VDDANA) power pins. Note: Vitesse recommends a (π filter) C-L-C choke over using a ferrite bead. All ground planes should be tied together using multiple vias.

Table 1: Recommended External Capacitor Values

Reference Frequency [MHz]	*Divide Ratio*	*CP*	*CN*	*Type*	*Size*	*Tol.*
19.44	32	0.1	0.1	X7R	0603/0803	+/-10%
38.88	16	0.1	0.1	X7R	0603/0803	+/-10%
51.84	12	0.1	0.1	X7R	0603/0803	+/-10%
77.76	8	0.1	0.1	X7R	0603/0803	+/-10%

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Figure 6: External Integrator Capacitor



Clock Multiplier Unit

Table 2: Reference Frequency Selection and Output Frequency Control

STS12	*B2*	*B1*	*B0*	*Reference Frequency [MHz]*	*Output Frequency [MHz]*
1	1	1	0	19.44	622.08
1	0	1	0	38.88	622.08
1	0	0	1	51.84	622.08
1	0	0	0	77.76	622.08
0	1	1	0	19.44	155.52
0	0	1	0	38.88	155.52
0	0	0	1	51.84	155.52
0	0	0	0	77.76	155.52

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Table 3: Clock Multiplier Unit Performance

Name	*Description*	*Min*	*Typ*	*Max*	*Units*
RCd	Reference clock duty cycle	40		60	%
RCj	Reference clock jitter (RMS) @ 77.76 MHz ref (1)			13	ps
RCj	Reference clock jitter (RMS) @ 51.84 MHz ref (1)			12	ps
RCj	Reference clock jitter (RMS) @ 38.88 MHz ref (1)			9	ps
RCj	Reference clock jitter (RMS) @ 19.44 MHz ref (1)			5	ps
RC_f	Reference clock frequency tolerance (2)	-20		+20	ppm
OCj	Output clock jitter (RMS) @ 77.76 MHz ref (3)			8	ps
OCj	Output clock jitter (RMS) @ 51.84 MHz ref (3)			10	ps
OCj	Output clock jitter (RMS) @ 38.88 MHz ref (3)			13	ps
OCj	Output clock jitter (RMS) @ 19.44 MHz ref (3)			15	ps
OCfrange	Output frequency	620		624	MHz
OCd	Output clock duty cycle	40		60	%

(1) These Reference Clock Jitter limits are required for the outputs to meet SONET system level jitter requirements (< 10 mUIrms)
(2) Needed to meet SONET output frequency stability requirements
(3) Measured

Note: Jitter specification is defined utilizing a 12KHz - 5MHz LP-HP single pole filter.

AC Timing Characteristics

Figure 7: Receive High Speed Data Input Timing Diagram

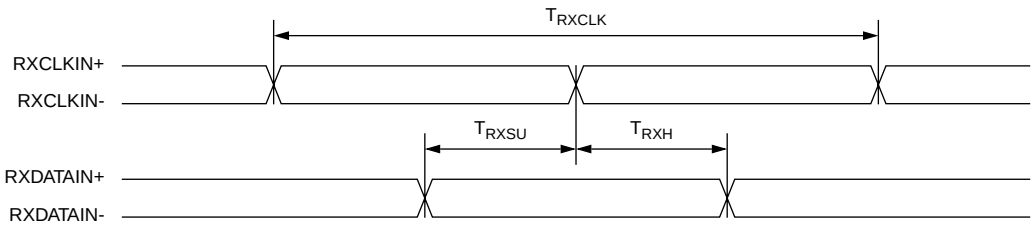


Table 4: Receive High Speed Data Input Timing Table *(STS-12 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{RXCLK}	Receive clock period	-	1.608	-	ns
T_{RXSU}	Serial data setup time with respect to RXCLKIN	250	-	-	ps
T_{RXH}	Serial data hold time with respect to RXCLKIN	250	-	-	ps

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Table 5: Receive High Speed Data Input Timing Table *(STS-3 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{RXCLK}	Receive clock period	-	6.43	-	ns
T_{RXSU}	Serial data setup time with respect to RXCLKIN	1.5	-	-	ns
T_{RXH}	Serial data hold time with respect to RXCLKIN	1.5	-	-	ns

Figure 8: Transmit Data Input Timing Diagram

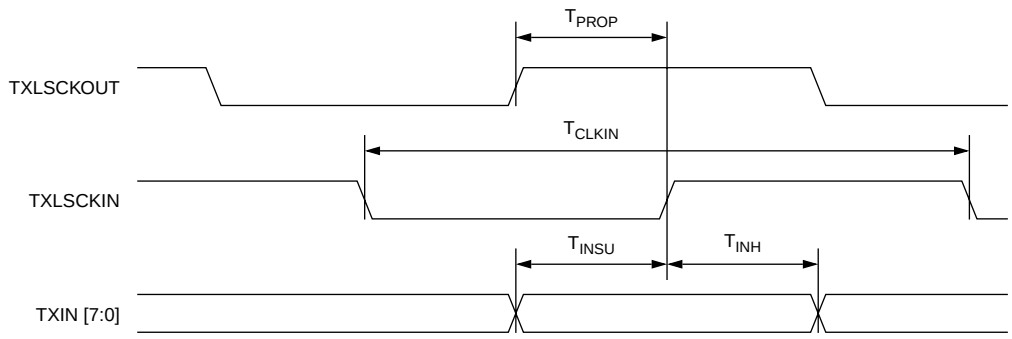


Table 6: Transmit Data Input Timing Table *(STS-12 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{CLKIN}	Transmit data input byte clock period	-	12.86	-	ns
T_{INSU}	Transmit data setup time with respect to TXLSCKIN	1.0	-	-	ns
T_{INH}	Transmit data hold time with respect to TXLSCKIN	1.0	-	-	ns
T_{PROP}	Maximum allowable propagation delay for connecting TXLSCKOUT to TXLSCKIN	-	-	3.0	ns

Table 7: Transmit Data Input Timing Table *(STS-3 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{CLKIN}	Transmit data input byte clock period	-	51.44	-	ns
T_{INSU}	Transmit data setup time with respect to TXLSCKIN	1.0	-	-	ns
T_{INH}	Transmit data hold time with respect to TXLSCKIN	1.0	-	-	ns
T_{PROP}	Maximum allowable propagation delay for connecting TXLSCKOUT to TXLSCKIN	-	-	30	ns

Note: Duty cycle for TXLSCKOUT is 50% +/- 10% worst case

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Figure 9: Receive Data Output Timing Diagram

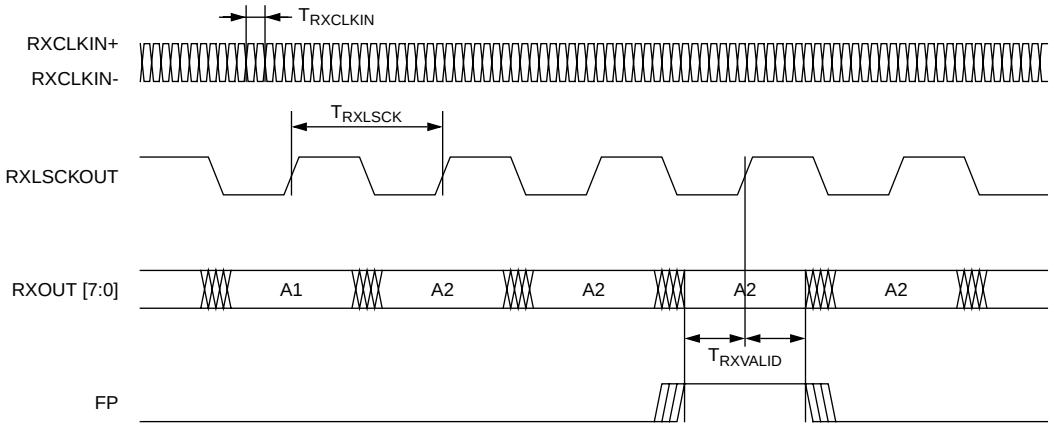


Table 8: Receive Data Output Timing Table *(STS-12 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXCLKIN}$	Receive clock period	-	1.608	-	ns
T_{RXLSCK}	Receive data output byte clock period	-	12.86	-	ns
$T_{RXVALID}$	Time data on RXOUT [7:0] and FP is valid before and after the rising edge of RXLSCKOUT	4.0	-	-	ns
T_{PW}	Pulse width of frame detection pulse FP	-	12.86	-	ns

Table 9: Receive Data Output Timing Table *(STS-3 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXCLKIN}$	Receive clock period	-	6.43	-	ns
$T_{RXLSCKT}$	Receive data output byte clock period	-	51.44	-	ns
$T_{RXVALID}$	Time data on RXOUT [7:0] and FP is valid before and after the rising edge of RXLSCKOUT	22	-	-	ns
T_{PW}	Pulse width of frame detection pulse FP	-	51.44	-	ns

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Figure 10: Transmit High Speed Data Timing Diagram

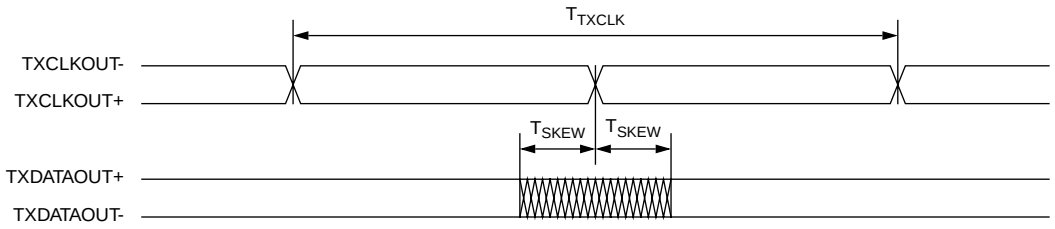


Table 10: Transmit High Speed Data Timing Table *(STS-12 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{TXCLK}	Transmit clock period	-	1.608	-	ns
T_{SKEW}	Skew between the falling edge of TXCLKOUT+ and valid data on TXDATAOUT	-	-	250	ps

Table 11: Transmit High Speed Data Timing Table *(STS-3 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{TXCLK}	Transmit clock period	-	6.43	-	ns
T_{SKEW}	Skew between the falling edge of TXCLKOUT+ and valid data on TXDATAOUT	-	-	250	ps

Data Latency

The VSC8111 contains several operating modes, each of which exercise different logic paths through the part. Table 12 bounds the data latency through each path with an associated clock signal.

Table 12: Data Latency

Circuit Mode	*Description*	*Clock Reference*	*Range of Clock cycles*
Transmit	Data TXIN [7:0] to MSB at TXDATAOUT	TXCLKOUT	4-13
Receive	MSB at RXDATAIN to data on RXOUT [7:0]	RXCLKIN	24-32
Equipment Loopback	Byte data TXIN [7:0] to byte data on RXOUT [7:0]	TXCLKOUT	27-35
Facilities Loopback	MSB at RXDATAIN to MSB at TXDATAOUT	RXCLKIN	2

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AC Characteristics

Table 13: PECL and TTL Outputs

Parameters	Description	Min	Typ	Max	Units	Conditions
$T_{R,TTL}$	TTL Output Rise Time	—	2	—	ns	10-90%
$T_{F,TTL}$	TTL Output Fall Time	—	1.5	—	ns	10-90%
$T_{R,PECL}$	PECL Output Rise Time	—	350	—	ps	20-80%
$T_{F,PECL}$	PECL Output Fall Time	—	350	—	ps	20-80%

DC Characteristics

Table 14: PECL and TTL Inputs and Outputs

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage (PECL)	—	—	V_{DD} – 0.9V	V	—
V_{OL}	Output LOW voltage (PECL)	0.7	—	—	V	—
V_{OCM}	O/P Common Mode Range (PECL)	1.1	—	V_{DD} – 1.3V	V	—
ΔV_{OUT75}	Differential Output Voltage (PECL)	600	—	1300	mV	75Ω to V_{DD} – 2.0 V
ΔV_{OUT50}	Differential Output Voltage (PECL)	600	—	1300	mV	50Ω to V_{DD} – 2.0 V
V_{IH}	Input HIGH voltage (PECL)	1.5	—	V_{DD} – 1.0V	V	—
V_{IL}	Input LOW voltage (PECL)	0	—	—	V	—
ΔV_{IN}	Differential Input Voltage (PECL)	400	—	1600	mV	—
V_{ICM}	I/P Common Mode Range (PECL)	1.5 – $\Delta V_{IN}/2$	—	V_{DD} – 1.0 – $\Delta V_{IN}/2$	V	—
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	I_{OH} = -1.0 mA

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Table 14: PECL and TTL Inputs and Outputs

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OL}	Output LOW voltage (TTL)	—	—	0.5	V	I_{OL} = +1.0 mA
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	—
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	50	500	µA	2.0V< V_{IN} < 5.5V, Typical@2.4V
I_{IL}	Input LOW current (TTL)	—	—	-500	µA	-0.5V < V_{IN} < 0.8V

Power Dissipation

Table 15: Power Supply Currents (Outputs Open)

Parameter	*Description*	*Typ*	*(Max)*	*Units*
I_{DD}	Power supply current from V_{DD}	355	403	mA
P_D	Power dissipation	1.2	1.4	W

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Absolute Maximum Ratings(1)

Power Supply Voltage (V_{DD}) Potential to GND .....-0.5V to +4V
DC Input Voltage (PECL inputs) ..... -0.5V to V_{DD} +0.5V
DC Input Voltage (TTL inputs) .....-0.5V to 5.5V
DC Output Voltage (TTL Outputs) ..... -0.5V to V_{DD} + 0.5V
Output Current (TTL Outputs) ..... +/-50mA
Output Current (PECL Outputs) ..... +/-50mA
Case Temperature Under Bias .....-55^{o} to $+125^{o}$C
Storage Temperature .....-65^{o}C to $+150^{o}$C
Maximum Input ESD (Human Body Model) ..... 1500 V

Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{DD}) .....+3.3V ±5 %
Commercial Operating Temperature Range* (*T*) ..... 0^{o} to 70^{o}C
Extended Operating Temperature Range* (*T*)..... 0^{o} to 110^{o}C
Industrial Operating Temperature Range* (*T*) ..... -40^{o} to 85^{o}C

** Lower limit of specification is ambient temperature and upper limit is case temperature.*

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Package Pin Description

Table 16: Pin Definitions

Signal	Pin	I/O	Level	Pin Description
FACLOOP	1	I	TTL	Facility loopback, active high
VDD	2		+3.3V	+3.3V Power Supply
N/C	3			No connection
RESET	4	I	TTL	Resets frame detection, dividers, controls, and tristates TTL outputs; active high
LOOPTIM0	5	I	TTL	Enable loop timing operation; active HIGH
B0	6	I	TTL	Reference clock select, refer to table 2
B1	7	I	TTL	Reference clock select, refer to table 2
B2	8	I	TTL	Reference clock select, refer to table 2
VDD	9		+3.3V	+3.3V Power Supply
TXDATAOUT+	10	O	PECL	Transmit output, high speed differential data +
TXDATAOUT-	11	O	PECL	Transmit output, high speed differential data -
VSS	12		GND	Ground
TXCLKOUT+	13	O	PECL	Transmit high speed clock differential output+
TXCLKOUT-	14	O	PECL	Transmit high speed clock differential output-
VDD	15		+3.3V	+3.3V Power Supply
N/C	16			No connection
N/C	17			No connection
VSS	18		GND	Ground
RXCLKIN+	19	I	PECL	Receive high speed differential clock input+
RXCLKIN-	20	I	PECL	Receive high speed differential clock input-
VDD	21		+3.3V	+3.3V Power Supply
OOF	22	I	TTL	Out Of Frame; Frame detection initiated with high level
N/C	23			No connection
RXDATAIN+	24	I	PECL	Receive high speed differential data input+
RXDATAIN-	25	I	PECL	Receive high speed differential data input-
NC	26			No connection
NC	27			No connection
VDD	28		+3.3V	+3.3V Power Supply
NC	29			No connection
N/C	30			No connection

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Table 16: Pin Definitions

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
VDD	31		+3.3V	+3.3V Power Supply
N/C	32			No connection
RX50MCK	33	O	TTL	Constant 51.84Mhz reference clock output, derived from the Clock Multiplier Unit
VSS	34		GND	Ground
RXOUT0	35	O	TTL	Receive output data bit0
RXOUT1	36	O	TTL	Receive output data bit1
VSS	37		GND	Ground
RXOUT2	38	O	TTL	Receive output data bit2
RXOUT3	39	O	TTL	Receive output data bit3
VSS	40		GND	Ground
RXOUT4	41	O	TTL	Receive output data bit4
RXOUT5	42	O	TTL	Receive output data bit5
VSS	43		GND	Ground
RXOUT6	44	O	TTL	Receive output data bit6
RXOUT7	45	O	TTL	Receive output data bit7
VSS	46		GND	Ground
RXLSCKOUT	47	O	TTL	Receive byte clock output
FP	48	O	TTL	Frame detection pulse
VDD	49		+3.3V	+3.3V Power Supply
N/C	50			No connection
CHNLEN	51	I	TTL	Tie Low (VSS) for normal operation
LOSTTL	52	I	TTL	Loss of Signal Control
LOSPOL	53	I	TTL	Loss of Signal Polarity
VDD	54		+3.3V	+3.3V Power Supply
VSS	55		GND	Ground
REFCLK	56	I	TTL	Reference clock input, refer to table 3
LOOPTIM1	57	I	TTL	Enable loop timing operation; active HIGH
VDD	58		+3.3V	+3.3V Power Supply
VSSA	59		GND	Analog Ground (CMU)
VSSA	60		GND	Analog Ground (CMU)
N/C	61			No connection
N/C	62			No connection

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Table 16: Pin Definitions

Signal	Pin	I/O	Level	Pin Description
CP1	63		Analog	CMU external capacitor (see Figure 6)
CN1	64		Analog	CMU external capacitor (see Figure 6)
CN2	65		Analog	CMU external capacitor (see Figure 6)
CP2	66		Analog	CMU external capacitor (see Figure 6)
VDDA	67		+3.3V	Analog Power Supply (CMU)
VDDA	68		+3.3V	Analog Power Supply (CMU)
VDDA	69		+3.3V	Analog Power Supply (CMU)
VSSA	70		GND	Analog Ground (CMU)
VSSA	71		GND	Analog Ground (CMU)
VSS	72		GND	Ground
N/C	73			No connection
N/C	74			No connection
VSS	75		GND	Ground
VDD	76		+3.3V	+3.3V Power Supply
N/C	77			No connection
N/C	78			No connection
N/C	79			No connection
N/C	80			No connection
VDD	81		+3.3V	+3.3V Power Supply
TXLSCKOUT	82	O	TTL	Transmit byte clock out
TXLSCKIN	83	I	TTL	Transmit byte clock in
VSS	84		GND	Ground
TXIN7	85	I	TTL	Transmit input data bit7
TXIN6	86	I	TTL	Transmit input data bit6
VSS	87		GND	Ground
TXIN5	88	I	TTL	Transmit input data bit5
TXIN4	89	I	TTL	Transmit input data bit4
N/C	90			No connection
TXIN3	91	I	TTL	Transmit input data bit3
TXIN2	92	I	TTL	Transmit input data bit2
VSS	93		GND	Ground
TXIN1	94	I	TTL	Transmit input data bit1
TXIN0	95	I	TTL	Transmit input data bit0

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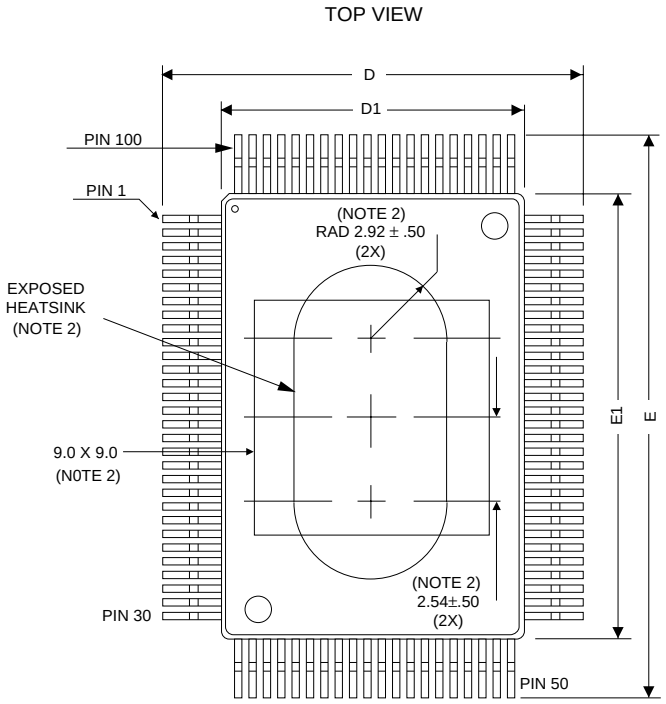
Table 16: Pin Definitions

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
N/C	96			No connection
STS12	97	I	TTL	155Mb/s or 622Mb/s mode select, refer to table 2
N/C	98			No connection
VDD	99		+3.3V	+3.3V Power Supply
EQULOOP	100	I	TTL	Equipment loopback, active high

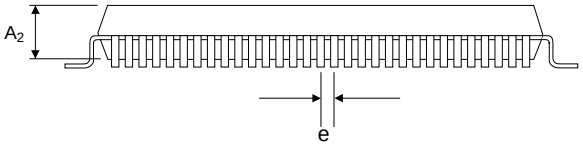
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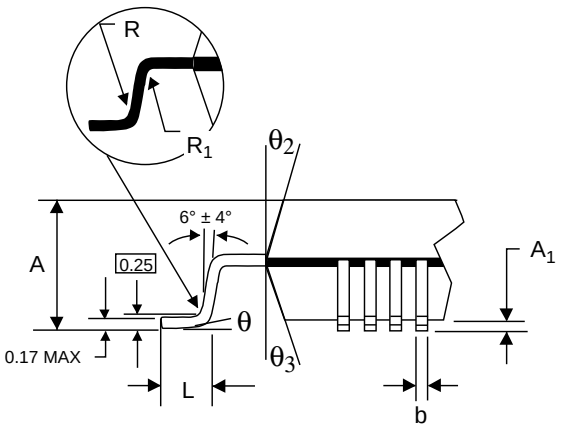
Package Information

100 PQFP Package Drawings



Key	mm	Tolerance
A	3.40	MAX
A1	0.25	MIN.
A2	2.7	±.10
D	17.20	±.20
D1	14.00	±.10
E	23.20	±.20
E1	20.00	±.10
L	0.80	±.2
e	0.65	NOM
b	0.30	±.10
θ	0°-7°	
R	.30	+0/-.1
R1	.2	NOM
θ2	15°	
θ3	15°	





NOTES:
(1) Drawings not to scale.
(2) Two styles of exposed heat spreaders may be used; square or oval.
(3) All units in millimeters unless otherwise noted

Package #: 101-202-4
Issue #: 2

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The VSC8111 is manufactured in a 100PQFP package which is supplied by two different vendors. The critical dimensions in the drawing represent the superset of dimensions for both packages. The significant difference between the two packages is in the shape and size of the heatspreader which needs to be considered when attaching a heatsink.

Package Thermal Characteristics

The VSC8111 is packaged in a thermally enhanced 100PQFP with an embedded heat sink. The heat sink surface configurations are shown in the package drawings. With natural convection, the case to air thermal resistance is estimated to be 27.5°C/W. The air flow versus thermal resistance relationship is shown in Table 17.

Table 17: Theta Case to Ambient versus Air Velocity

Air Velocity (LFPM)	*Case to air thermal resistance °C/W*
0	27.5
100	23.1
200	19.8
400	17.6
600	16

Junction to case thermal resistance is 1.2 °C/W.

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Ordering Information

The order number for this product are:

Part Number	Device Type
VSC8111QB:	155Mb/s-622Mb/s Mux/Dmux with CMU in 100 Pin PQFP Commercial Temperature, 0°C ambient to 70°C case
VSC8111QB1	155Mb/s-622Mb/s Mux/Dmux with CMU in 100 Pin PQFP Extended Temperature, 0°C ambient to 110°C case
VSC8111QB2	155Mb/s-622Mb/s Mux/Dmux with CMU in 100 Pin PQFP Industrial Temperature, -40°C ambient to 85°C case

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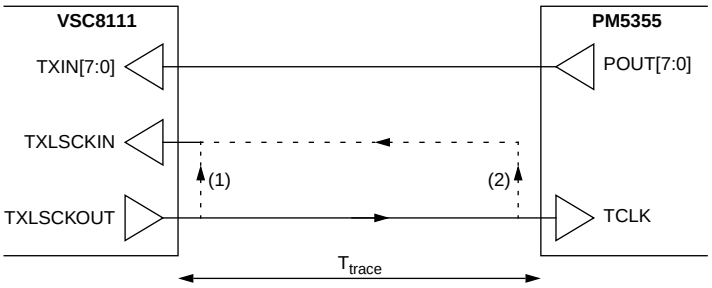
Application Notes

Interconnecting the Byte Clocks (TXLSCKOUT and TXLSCKIN)

The byte clock (TXLSCKOUT and TXLSCKIN) on the VSC8111 has been brought off-chip to allow as much flexibility in system-level clocking schemes as possible. Since the byte clock (TXLSCKOUT) clocks both the VSC8111 and the UNI devices, it is important to pay close attention to the routing of this signal. The UNI device in general is a CMOS part which can have very wide spreads in timing (1-11ns clock in to parallel data out for the PM5355), which utilizes most of the 12.86ns period (at 78MHz), leaving little for the trace delays and set-up times required to interconnect the 2 devices.

The VSC8111 and the UNI device should be placed as close to each other as possible to provide maximum setup and hold time margin at the inputs of the VSC8111. Figure 11 suggests two different ways of routing the TXLSCKOUT-to-TXLSCKIN clock trace when used in a 622MHz mode; which ever method is used, the transmission line trace impedance should be no lower than 75 ohms.

Figure 11: Interconnecting the Byte Clocks



(1) TXLSCKOUT and TXLSCKIN are tied together at the pins of the VSC8111. This provides a setup and hold time margin for the TXIN input of

- $T_{su,margin} = T_{clk} - T_{TCLK\text{-}POUT,max}(PM5355) - T_{su,min}(VSC8111) - 2xT_{trace} = 0.86ns - 2xT_{trace}$
- $T_{hold,margin} = T_{TCLK\text{-}POUT,min}(PM5355) - T_{hold,min}(VSC8111) + 2xT_{trace} = 2xT_{trace}$

(2) TXLSCKOUT is daisy chained to the UNI device and then routed back to the VSC8111 along with the byte data. This interface provides a setup and hold time margin for the TXIN input of

- $T_{su,margin} = T_{clk} - T_{TCLK\text{-}POUT,max}(PM5355) - T_{su,min}(VSC8111) = 0.86ns$
- $T_{hold,margin} = T_{TCLK\text{-}POUT,min}(PM5355) - T_{hold,min}(VSC8111) = 0ns$

Option (2) does not provide any hold time margin, while option (1) requires the one-way trace delay (T_{trace}) to be less than 0.43ns (~3 inches).

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Important note: The 11 ns max Tpd on the PM5355 assumes a 50pf load @ 60ps/pf, therefore 3 ns of the max delay is due to loading. The VSC8113 input (TXLSCKIN) plus package is about 6pf. Assuming about 1 pf/inch of 75 ohm trace on FR4 plus the VSC8113 6pf load, the user would in most cases choose option 1.

AC Coupling and Terminating High-speed PECL I/Os

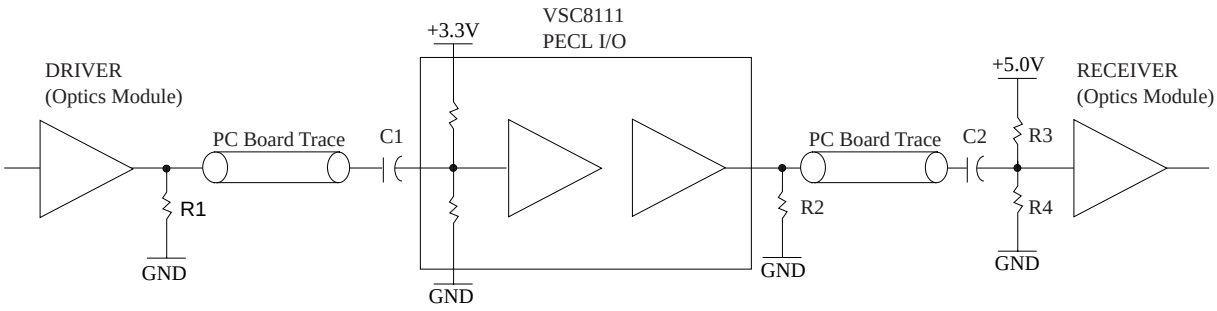
The high speed signals on the VSC8111 (RXDATAIN, RXCLKIN, TXDATAOUT, TXCLKOUT) use 3.3V PECL levels which are essentially ECL levels shifted positive by 3.3 volts. The PECL I/Os are referenced to the V_{DD} supply (VDD) and are terminated to ground. Since most optics modules use either ECL or 5.0V PECL levels, the high speed ports need to be either AC-coupled to overcome the difference in dc levels, or DC translated (DC level shift).

The PECL receiver inputs of the VSC8111 are internally biased at VDD/2. Therefore, AC-coupling to the VSC8111 inputs is accomplished by providing the pull-down resistor for the open-source PECL output and an AC-coupling capacitor used to eliminate the DC component of the output signal. This capacitor allows the PECL receivers of the VSC8111 to self-bias via its internal resistor divider network (see Figure 13).

The PECL output drivers are capable of sourcing current but not sinking it. To establish a LOW output level, a pull-down resistor, traditionally connected to VDD-2.0V, is needed when the output FET is turned off. Since VDD-2.0V is usually not present in the system, the resistor should be terminated to ground for convenience. The VSC8111 output drivers should be either AC-coupled to the 5.0V PECL inputs of the optics module, or translated (DC level shift). Appropriate biasing techniques for setting the DC-level of these inputs should be employed.

The DC biasing and 50 ohm termination requirements can easily be integrated together using a thevenin equivalent circuit as shown in Figure 12. The figure shows the appropriate termination values when interfacing 3.3V PECL to 5.0V PECL. This network provides the equivalent 50 ohm termination for the high speed I/Os and also provides the required dc biasing for the receivers of the optics module. Table 18 contains recommended values for each of the components.

Figure 12: AC Coupled High Speed I/O



Note: Only one side of a differential signal is shown.

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Table 18: AC Coupling Component Values

Component	*Value*	*Tolerance*
R1	270 ohms	5%
R2	75 ohms	5%
R3	68 ohms	1%
R4	190 ohms	1%
C1, C2, C3, C4	.01uf High Frequency	10%

TTL Input Structure

The TTL inputs of the VSC8111 are 3.3V TTL which can accept 5.0V TTL levels within a given set of tolerances (see Table 14). The input structure, shown in Figure 13, uses a current limiter to avoid overdriving the input FETs.

Layout of the High Speed Signals

The routing of the High Speed signals should be done using good high speed design practices. This would include using controlled impedance lines (50 ohms) and keeping the distance between components to an absolute minimum. In addition, stubs should be kept at a minimum as well as any routing discontinuities. This will help minimize reflections and ringing on the high speed lines and insure the maximum eye opening. In addition the output pull down resistor R2 should be placed as close to the VSC8111 pin as possible while the AC-coupling capacitor C2 and the biasing resistors R3, R4 should be placed as close as possible to the optics input pin. The same is true on the receive circuit side. Using small outline components and minimum pad sizes also helps in reducing discontinuities.

Ground Planes

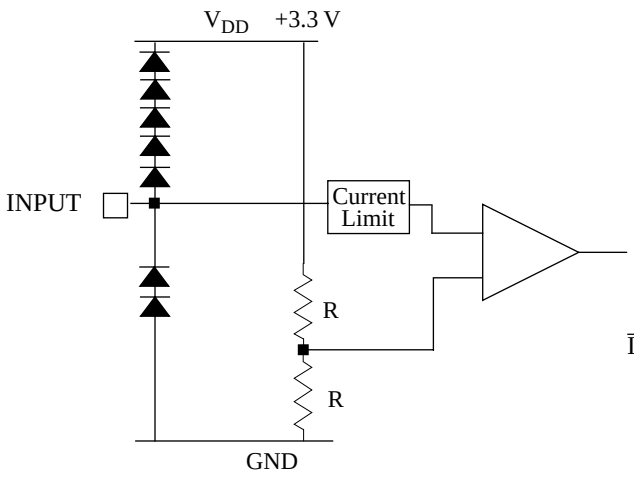
The ground plane for the components used in the High Speed interface should be continuous and not sectioned in an attempt to provide isolation to various components. Sectioning of the ground planes tends to interfere with the ground return currents on the signal lines. In addition, the smaller the ground planes the less effective they are in reducing ground bounce noise and the more difficult to decouple. Sectioning of the positive supplies can provide some isolation benefits.

Analog Power Supplies

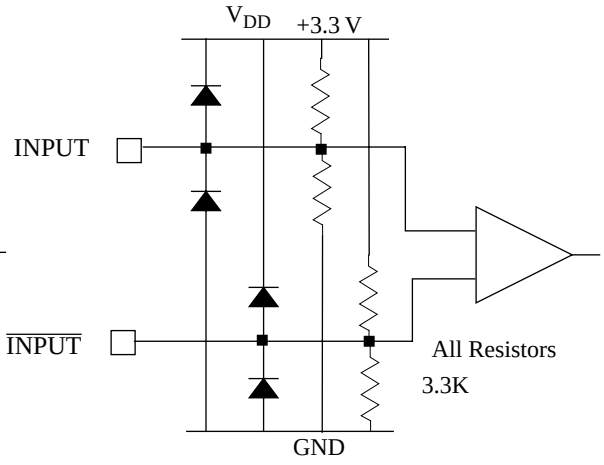
Good analog design practices should be applied to the board design for the analog ground and power planes. The dedicated PLL power (VDDA) and ground (VSSA) pins need to have quiet supply planes to minimize jitter generation within the clock synthesis unit. This is accomplished by either using a ferrit bead or a C-L-C choke (π filter).

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Figure 13: Input Structures



REFCLK and TTL Inputs



High Speed Differential Input
(RXDATAIN+/RXDATAIN-)
(RXCLKIN+/RXCLKIN-)

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