



**4Mb: 256K x 18, 128K x 32/36
FLOW-THROUGH SYNCBURST SRAM**

4Mb SYNCBURST™ SRAM

MT58L256L18F1, MT58L128L32F1,
MT58L128L36F1; MT58L256V18F1,
MT58L128V32F1, MT58L128V36F1

3.3V V_{DD}, 3.3V or 2.5V I/O, Flow-Through

FEATURES

- Fast clock and OE# access times
- Single +3.3V +0.3V/-0.165V power supply (V_{DD})
- Separate +3.3V or +2.5V isolated output buffer supply (V_{DDQ})
- SNOOZE MODE for reduced-power standby
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control pin (interleaved or linear burst)
- Automatic power-down
- 165-pin FBGA package
- 100-pin TQFP package
- Low capacitive bus loading
- x18, x32, and x36 versions available

OPTIONS

- Timing (Access/Cycle/MHz)
6.8ns/7.5ns/133 MHz
7.5ns/8.8ns/113 MHz
8.5ns/10ns/100 MHz
10ns/15ns/66 MHz

- Configurations
3.3V I/O

256K x 18
128K x 32
128K x 36

- 2.5V I/O

256K x 18
128K x 32
128K x 36

- Packages
100-pin TQFP
165-pin FBGA

- Operating Temperature Range
Commercial (0°C to +70°C)
Industrial (-40°C to +85°C)**

MARKING

-6.8
-7.5
-8.5
-10

MT58L256L18F1
MT58L128L32F1
MT58L128L36F1

MT58L256V18F1
MT58L128V32F1
MT58L128V36F1

T
F*

None
IT

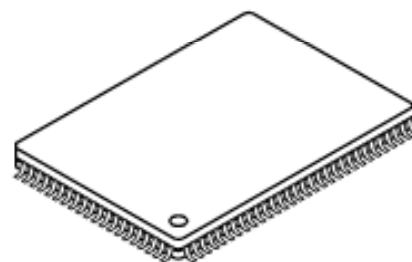
Part Number Example:

MT58L256L18F1T-8.5

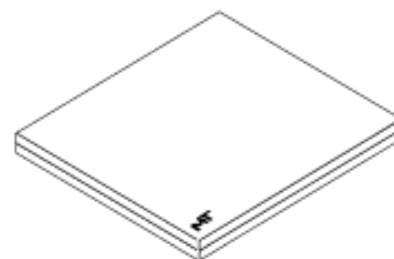
* A Part Marking Guide for the FBGA devices can be found on Micron's Web site—<http://www.micron.com/support/index.html>.

** Industrial temperature range offered in specific speed grades and configurations. Contact factory for more information.

100-Pin TQFP¹



165-Pin FBGA



NOTE: 1. JEDEC-standard MS-026 BHA (LQFP).

GENERAL DESCRIPTION

The Micron® SyncBurst™ SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

Micron's 4Mb SyncBurst SRAMs integrate a 256K x 18, 128K x 32, or 128K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2#, CE2), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#) and global write (GW#).

4Mb: 256K x 1B, 128K x 2/3B Flow-Through SyncBurst SRAM
MITSUBISHI 256L10E1 E.pds - Rev. 2002



4Mb: 256K x 18, 128K x 32/36 FLOW-THROUGH SYNCBURST SRAM

GENERAL DESCRIPTION (continued)

Asynchronous inputs include the output enable (OE#), clock (CLK) and snooze enable (ZZ). There is also a burst mode input (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE#, is also asynchronous. WRITE cycles can be from one to two bytes wide (x18) or from one to four bytes wide (x32/x36), as controlled by the write control inputs.

Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) inputs. Subsequent burst addresses can be internally generated as controlled by the burst advance input (ADV#).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During WRITE cycles on the x18 device,

BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb. During WRITE cycles on the x32 and x36 devices, BWa# controls DQa pins and DQPa; BWb# controls DQb pins and DQPb; BWc# controls DQc pins and DQPc; Bwd# controls DQd pins and DQPd. GW# LOW causes all bytes to be written. Parity bits are only available on the x18 and x36 versions.

Micron's 4Mb SyncBurst SRAMs operate from a +3.3V VDD power supply, and all inputs and outputs are TTL-compatible. Users can choose either a 2.5V or 3.3V I/O version. The device is ideally suited for 486, Pentium®, and PowerPC systems and those systems that benefit from a wide synchronous data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64-, and 72-bit-wide applications.

Please refer to Micron's Website (www.micron.com/srams) for the latest data sheet.

TQFP PIN ASSIGNMENT TABLE

PIN #	x18	x32/x36
1	NC	NC/DQPC*
2	NC	DQc
3	NC	DQc
4	VDDQ	
5	VSS	
6	NC	DQc
7	NC	DQc
8	DQb	DQc
9	DQb	DQc
10	VSS	
11	VDDQ	
12	DQb	DQc
13	DQb	DQc
14	VSS	
15	VDD	
16	NC	
17	VSS	
18	DQb	DQd
19	DQb	DQd
20	VDDQ	
21	VSS	
22	DQb	DQd
23	DQb	DQd
24	DQPa	DQd
25	NC	DQd

PIN #	x18	x32/x36
26	VSS	
27	VDDQ	
28	NC	DQd
29	NC	DQd
30	NC	NC/DQPd*
31	MODE	
32	SA	
33	SA	
34	SA	
35	SA	
36	SA1	
37	SA0	
38	DNU	
39	DNU	
40	VSS	
41	VDD	
42	NF**	
43	NF**	
44	SA	
45	SA	
46	SA	
47	SA	
48	SA	
49	SA	
50	SA	

PIN #	x18	x32/x36
51	NC	NC/DQPa*
52	NC	DQa
53	NC	DQa
54	VDDQ	
55	VSS	
56	NC	DQa
57	NC	DQa
58	DQa	
59	DQa	
60	VSS	
61	VDDQ	
62	DQa	
63	DQa	
64	ZZ	
65	VDD	
66	NC	
67	VSS	
68	DQa	DQb
69	DQa	DQb
70	VDDQ	
71	VSS	
72	DQa	DQb
73	DQa	DQb
74	DQPa	DQb
75	NC	DQb

PIN #	x18	x32/x36
76	VSS	
77	VDDQ	
78	NC	DQb
79	NC	DQb
80	SA	NC/DQPb*
81	SA	
82	SA	
83	ADV#	
84	ADSP#	
85	ADSC#	
86	OE#	
87	BWE#	
88	GW#	
89	CLK	
90	VSS	
91	VDD	
92	CE2#	
93	BWb#	
94	BWb#	
95	NC	BWc#
96	NC	BWd#
97	CE2	
98	CE#	
99	SA	
100	SA	

*No Connect (NC) is used on the x32 version. Parity (DQPx) is used on the x36 version.

**Pins 43 and 42 are reserved for address expansion, 8Mb and 16Mb respectively.