LF3320
Horizontal Digital Image Filter

FEATURES

- 83 MHz Data Rate
- 12-bit Data or Coefficients (Expandable to 24-bit)
- 32-Tap FIR Filter, Cascadable for More Filter Taps
- Over 49 K-bits of on-board Memory
- LF Interface™ Allows All 256 Coefficient Sets to be Updated Within Vertical Blanking
- Various Operating Modes: Dual Filter, Single Filter, Double Wide Data or Coefficient, Matrix Multiplication, and Accumulator Access.
- Selectable 16-bit Data Output with User-Defined Rounding and Limiting
- Supports Interleaved Data Streams
- Supports Decimation up to 16:1 for Increasing Number of Filter Taps
- 3.3 Volt Supply
- 144 Lead PQFP

DESCRIPTION

The **LF3320** filters digital images in the horizontal dimension at real-time video rates. The input and coefficient data are both 12 bits and in two's complement format. The output is also in two's complement format and may be rounded to 16 bits.

The LF3320 is designed to take advantage of symmetric coefficient sets. When symmetric coefficient sets are used, the device can be configured as a single 32-tap FIR filter or as two separate 16-tap FIR filters.

When asymmetric coefficient sets are used, the device can be configured as a single 16-tap FIR filter or as two separate 8-tap FIR filters. Multiple LF3320s can be cascaded to create larger filters.

Interleave / Decimation Registers (I / D Registers) allow interleaved data to be fed directly into the device and filtered without separating the data into individual data streams.

The LF3320 can handle a maximum of sixteen data sets interleaved together. The I / D Registers and on-chip accumulators facilitate using decimation to increase the number of filter taps. Decimation of up to 16:1 is supported.

The LF3320 contains enough on-board memory to store 256 coefficient sets. Two separate LF Interfaces™ allow all 256 coefficient sets to be updated within vertical blanking.

LF3320 BLOCK DIAGRAM

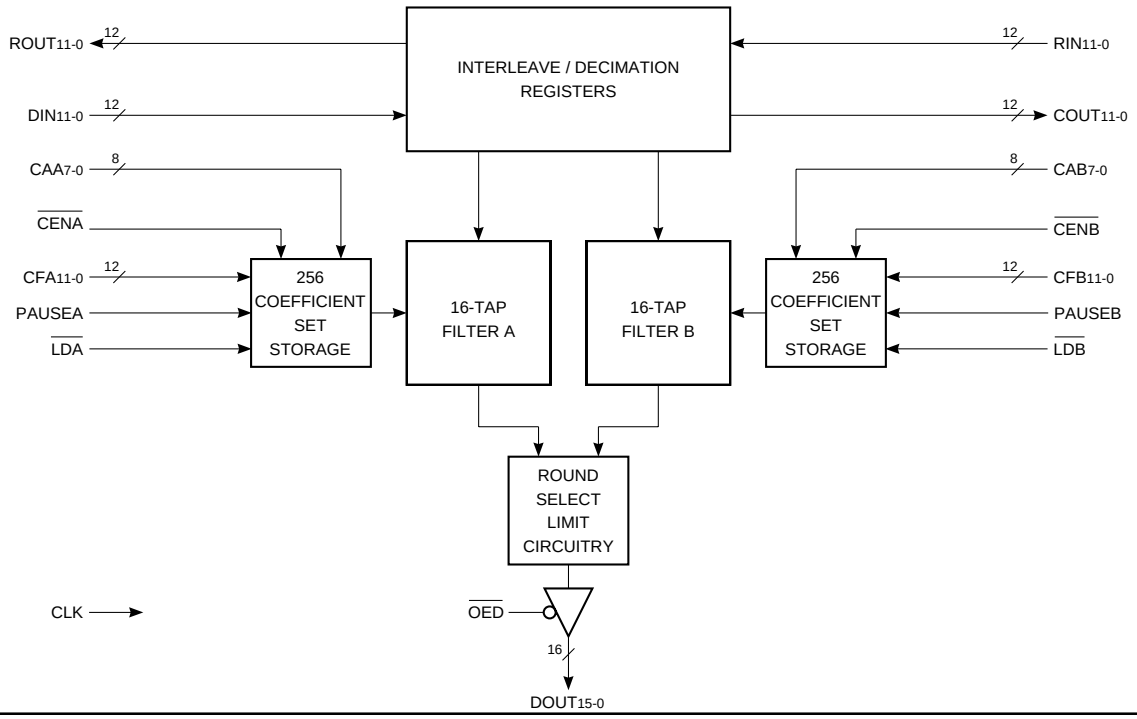
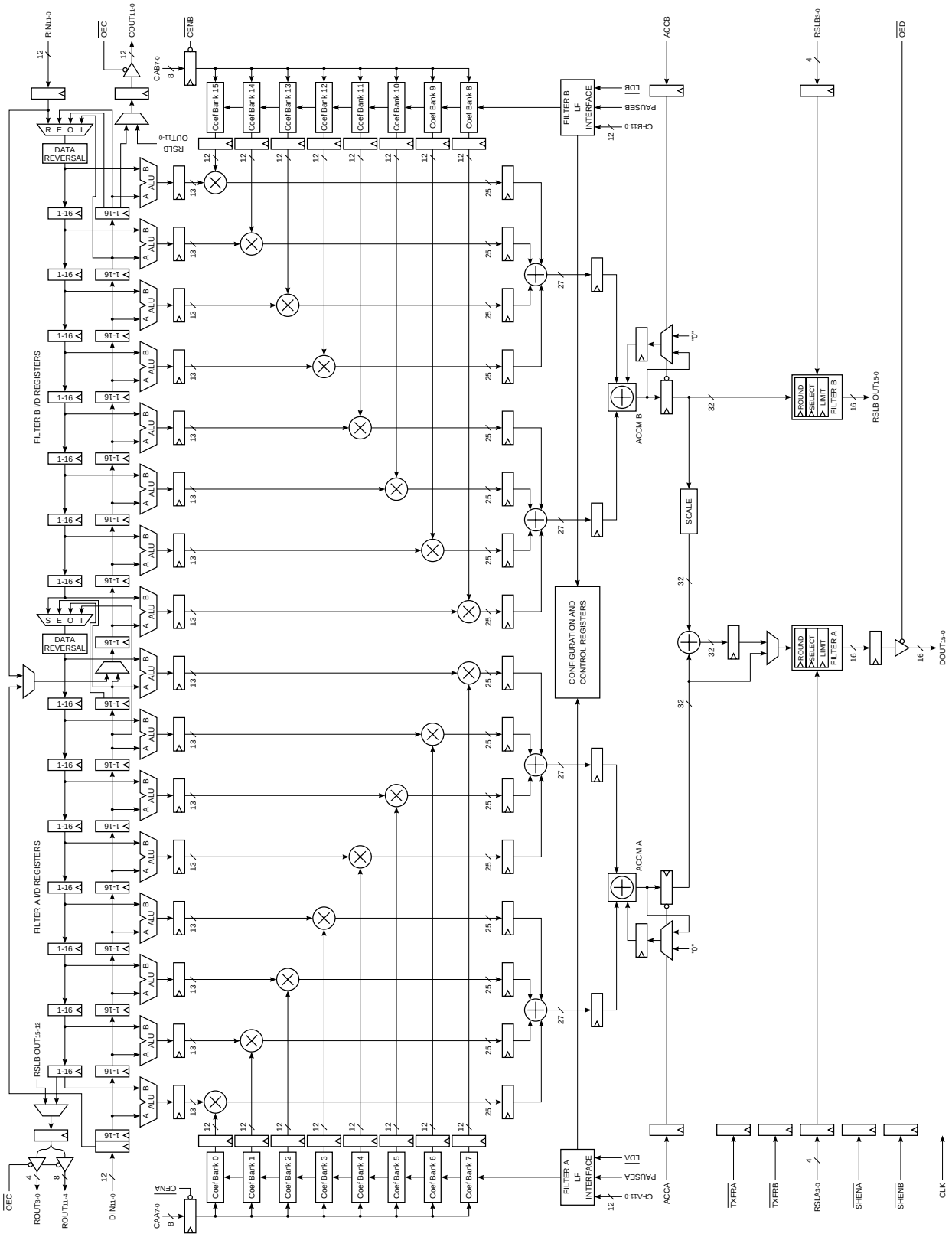


FIGURE 1. LF3320 FUNCTIONAL BLOCK DIAGRAM



SIGNAL DEFINITIONS

Power

VCC and GND

+3.3 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers.

Inputs

DIN11-0 — Data Input

DIN11-0 is the 12-bit data input port to Filter A. In Dual Filter Mode, DIN11-0 can also be the 12-bit input port to Filter B. Data is latched on the rising edge of CLK.

RIN11-0 — Reverse Cascade Input

In Single Filter Mode, RIN11-0 is the 12-bit reverse cascade input port. This port is connected to ROUT11-0 of another LF3320. In Dual Filter Mode, RIN11-0 can be the 12-bit input port to Filter B. Data is latched on the rising edge of CLK.

CFA11-0 — Coefficient A Input

CFA11-0 is used to load data into the Filter A coefficient banks (banks 0 through 7) and the configuration / control registers. Data present on CFA11-0 is latched into the Filter A LF Interface™ on the rising edge of CLK when LDA is LOW (see the LF Interface™ section for a full discussion).

CAA7-0 — Coefficient Address A

CAA7-0 determines which row of data in coefficient banks 0 through 7 is fed to the multipliers. CAA7-0 is latched into Coefficient Address Register A on the rising edge of CLK when CENA is LOW.

FIGURE 2. INPUT FORMATS



FIGURE 3. ACCUMULATOR OUTPUT FORMATS



TABLE 1. OUTPUT FORMATS

SLCT4-0	S15	S14	S13	· · ·	S8	S7	· · ·	S2	S1	S0
00000	F15	F14	F13	· · ·	F8	F7	· · ·	F2	F1	F0
00001	F16	F15	F14	· · ·	F9	F8	· · ·	F3	F2	F1
00010	F17	F16	F15	· · ·	F10	F9	· · ·	F4	F3	F2
·	·	·	·		·	·		·	·	·
·	·	·	·		·	·		·	·	·
·	·	·	·		·	·		·	·	·
01110	F29	F28	F27	· · ·	F22	F21	· · ·	F16	F15	F14
01111	F30	F29	F28	· · ·	F23	F22	· · ·	F17	F16	F15
10000	F31	F30	F29	· · ·	F24	F23	· · ·	F18	F17	F16

CFB11-0 — Coefficient B Input

CFB11-0 is used to load data into the Filter B coefficient banks (banks 8 through 15) and the configuration / control registers. Data present on CFB11-0 is latched into the Filter B LF Interface™ on the rising edge of CLK when LDB is LOW (see the LF Interface™ section for a full discussion).

CAB7-0 — Coefficient Address B

CAB7-0 determines which row of data in coefficient banks 8 through 15 is fed to the multipliers. CAB7-0 is latched into Coefficient Address Register B on the rising edge of CLK when CENB is LOW.

Outputs

DOUT15-0 — Data Output

DOUT15-0 is the 16-bit registered data output port for the overall filter (Single Filter Mode) or Filter A (Dual Filter Mode).

COUT11-0 — Cascade Output

In Single Filter Mode, COUT11-0 is a 12-bit registered cascade output port. COUT11-0 should be connected to DIN11-0 of another LF3320. In Dual Filter Mode, COUT11-0 is a 12-bit registered output port for the lower twelve bits of the 16-bit Filter B output.

ROUT11-0 — Reverse Cascade Output

In Single Filter Mode, ROUT11-0 is a 12-bit registered cascade output port. ROUT11-0 on one device should be connected to RIN11-0 of another LF3320. In Dual Filter Mode, ROUT3-0 is a 4-bit registered output port for the upper four bits of the 16-bit Filter B output. In this mode, ROUT11-4 is disabled.

Controls

$\overline{LDA}$ — Coefficient A Load

When $\overline{LDA}$ is LOW, data on CFA11-0 is latched into the Filter A LF Interface™ on the rising edge of CLK. When $\overline{LDA}$ is HIGH, data is not loaded into the Filter A LF Interface™. When enabling the LF Interface™ for data input, a HIGH to LOW transition of $\overline{LDA}$ is required in order for the input circuitry to function properly. Therefore, $\overline{LDA}$ must be set HIGH immediately after power up to ensure proper operation of the input circuitry (see the LF Interface™ section for a full discussion).

$\overline{CENA}$ — Coefficient Address Enable A

When $\overline{CENA}$ is LOW, data on CAA7-0 is latched into Coefficient Address Register A on the rising edge of CLK. When $\overline{CENA}$ is HIGH, data on CAA7-0 is not latched and the register's contents will not be changed.

$\overline{LDB}$ — Coefficient B Load

When $\overline{LDB}$ is LOW, data on CFB11-0 is latched into the Filter B LF Interface™ on the rising edge of CLK. When $\overline{LDB}$ is HIGH, data is not loaded into the Filter B LF Interface™. When enabling the LF Interface™ for data input, a HIGH to LOW transition of LDB is required in order for the input circuitry to function properly. Therefore, LDB must be set HIGH immediately after power up to ensure proper operation of the input circuitry (see the LF Interface™ section for a full discussion).

$\overline{CENB}$ — Coefficient Address Enable B

When $\overline{CENB}$ is LOW, data on CAB7-0 is latched into Coefficient Address Register B on the rising edge of CLK. When $\overline{CENB}$ is HIGH, data on CAB7-0 is not latched and the register's contents will not be changed.

$\overline{TXFRA}$ — Filter A LIFO Transfer Control

$\overline{TXFRA}$ is used to change which LIFO in the data reversal circuitry sends data to the reverse data path and which LIFO receives data from the forward data path in Filter A. When TXFRA goes LOW, the LIFO sending data to the reverse data path becomes the LIFO receiving data from the forward data path, and the LIFO receiving data from the forward data path becomes the LIFO sending data to the reverse data path. The device must see a HIGH to LOW transition of $\overline{TXFRA}$ in order to switch LIFOs. $\overline{TXFRA}$ is latched on the rising edge of CLK.

$\overline{TXFRB}$ — Filter B LIFO Transfer Control

$\overline{TXFRB}$ is used to change which LIFO in the data reversal circuitry sends data to the reverse data path and which LIFO receives data from the forward data path in Filter B. When TXFRB goes LOW, the LIFO sending data to the reverse data path becomes the LIFO receiving data from the forward data path, and the LIFO receiving data from the forward data path becomes the LIFO sending data to the reverse data path. The device must see a HIGH to LOW transition of $\overline{TXFRB}$ in order to switch LIFOs. $\overline{TXFRB}$ is latched on the rising edge of CLK.

ACCA — Accumulator A Control

When ACCA is HIGH, Accumulator A is enabled for accumulation and the Accumulator A Output Register is disabled for loading. When ACCA is LOW, no accumulation is performed and the Accumulator A Output Register is enabled for loading. ACCA is latched on the rising edge of CLK.

ACCB — Accumulator B Control

When ACCB is HIGH, Accumulator B is enabled for accumulation and the Accumulator B Output Register is disabled for loading. When ACCB is LOW, no accumulation is performed and the Accumulator B Output Register is enabled for loading. ACCB is latched on the rising edge of CLK.

$\overline{SHENA}$ — Filter A Shift Enable

In Dual Filter Mode, $\overline{SHENA}$ enables or disables the loading of data into the Input (DIN11-0) and Filter A I/D Registers. When $\overline{SHENA}$ is LOW, data is latched into the Input/Cascade Registers and shifted through the I/D Registers on the rising edge of CLK. When $\overline{SHENA}$ is HIGH, data can not be loaded into the Input/Cascade Registers or shifted through the I/D Registers and their contents will not be changed.

In Single Filter Mode, $\overline{SHENA}$ also enables or disables the loading of data into the Reverse Cascade Input (RIN11-0), Cascade Output (COUT11-0), Reverse Cascade Output (ROUT11-0) and Filter B I/D Registers. It is important to note that in Single Filter Mode, both $\overline{SHENA}$ and $\overline{SHENB}$ should be connected together. Both must be active to enable data loading in Single Filter Mode. $\overline{SHENA}$ is latched on the rising edge of CLK.

$\overline{SHENB}$ — Filter B Shift Enable

In Dual Filter Mode, $\overline{SHENB}$ enables or disables the loading of data into the Reverse Cascade Input (RIN11-0), Cascade Output (COUT11-0), Reverse Cascade Output (ROUT3-0) and Filter B I/D Registers. When $\overline{SHENB}$ is LOW, data is latched into the Cascade Registers and shifted through the I/D

Registers on the rising edge of CLK. When $\overline{SHENB}$ is HIGH, data can not be loaded into the Cascade Registers or shifted through the I / D Registers and their contents will not be changed.

In Single Filter Mode, $\overline{SHENB}$ also enables or disables the loading of data into the Input (DIN11-0), Reverse Cascade Output (ROUT11-0) and Filter A I / D Registers. It is important to note that in Single Filter Mode, both $\overline{SHENA}$ and $\overline{SHENB}$ should be connected together. Both must be active to enable data loading in Single Filter Mode. $\overline{SHENB}$ is latched on the rising edge of CLK.

RSLA3-0 — Filter A Round/Select/Limit Control

RSLA3-0 determines which of the sixteen user-programmable Round / Select / Limit registers (RSL registers) are used in the Filter A RSL circuitry. A value of 0 on RSLA3-0 selects RSL register 0. A value of 1 selects RSL register 1 and so on. RSLA3-0 is latched on the rising edge of CLK (see the round, select, and limit sections for a complete discussion).

RSLB3-0 — Filter B Round/Select/Limit Control

RSLB3-0 determines which of the sixteen user-programmable RSL registers are used in the Filter B RSL circuitry. A value of 0 on RSLB3-0 selects RSL register 0. A value of 1 selects RSL register 1 and so on. RSLB3-0 is latched on the rising edge of CLK (see the round, select, and limit sections for a complete discussion).

$\overline{OED}$ — DOUT Output Enable

When $\overline{OED}$ is LOW, DOUT15-0 is enabled for output. When $\overline{OED}$ is HIGH, DOUT15-0 is placed in a high-impedance state.

$\overline{OEC}$ — COUT/ROUT Output Enable

When $\overline{OEC}$ is LOW, COUT11-0 and ROUT3-0 are enabled for output. When $\overline{OEC}$ is HIGH, COUT11-0 and ROUT3-0 are placed in a high-impedance state.

PAUSEA — LF Interface™ Pause

When PAUSEA is HIGH, the Filter A LF Interface™ loading sequence is halted until PAUSEA is returned to a LOW state. This effectively allows the user to load coefficients and control registers at a slower rate than the master clock (see the LF Interface™ section for a full discussion).

PAUSEB — LF Interface™ Pause

When PAUSEB is HIGH, the Filter B LF Interface™ loading sequence is halted until PAUSEB is returned to a LOW state. This effectively allows the user to load coefficients and control registers at a slower rate than the master clock (see the LF Interface™ section for a full discussion).

FIGURE 4. SINGLE FILTER MODE

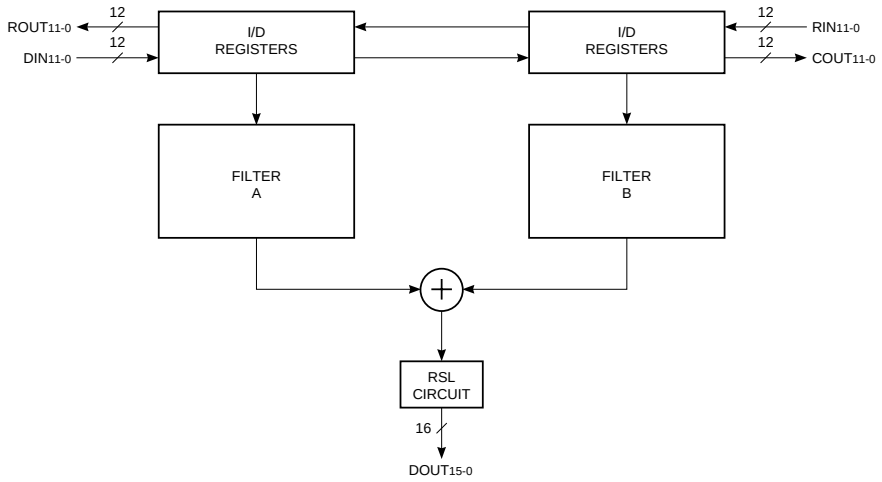
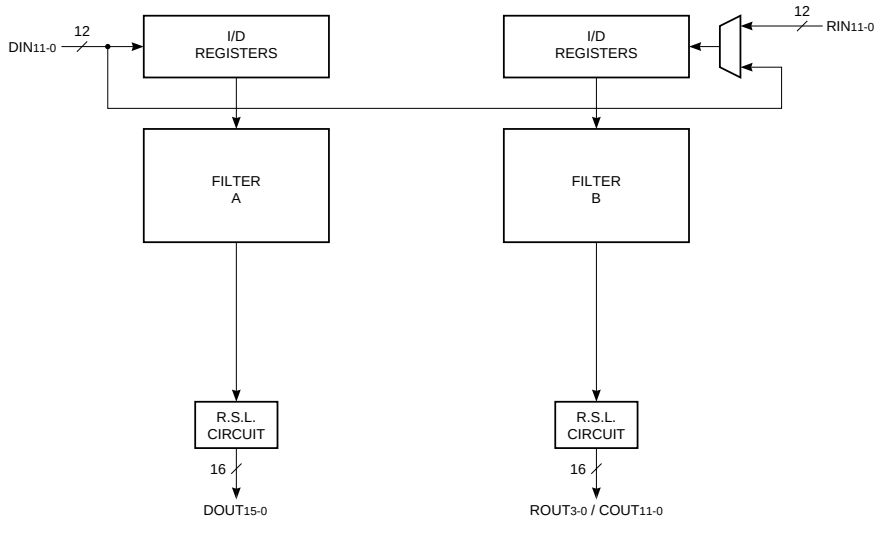


FIGURE 5. DUAL FILTER MODE



OPERATIONAL MODES

Single Filter Mode

In this mode, the device operates as a single FIR filter (see Figure 4). It can be configured to have as many as 32 taps if symmetric coefficient sets are used. If asymmetric coefficient sets are used, the device can be configured to have as many as 16 taps. Cascade ports are provided to facilitate cascading multiple devices to increase the number of filter taps. Bit 1 in Configuration Register 5 determines the filter mode. In Single Filter Mode, DIN_{11-0} is the data input for the filter and $DOUT_{15-0}$ is the data output for the filter.

Dual Filter Mode

In this mode, the device operates as two separate FIR filters (see Figure 5). Each filter can be configured to have as many as 16 taps if symmetric coefficient sets are used. If asymmetric coefficient sets are used, each filter can be configured to have as many as 8 taps. In Dual Filter Mode, DIN11-0 is the data input for Filter A. Either RIN11-0 or DIN11-0 can be the data input for Filter B. The Filter B input is determined by Bit 2 in Configuration Register 5. DOUT15-0 is the data output for Filter A. COUT11-0 and ROUT3-0 together form the data output for Filter B. COUT11-0 is the twelve least significant bits and ROUT3-0 is the four most significant bits of the 16-bit Filter B output.

Matrix-vector Multiply Mode

In this mode, the LF3320 can be configured to multiply a square matrix of maximum size N (N = 8 or 16), multiplied by a matrix-vector of maximum size [8,1] or [16,1]. The mathematical representation for this operation is in Figure 7. When configured in the dual filter mode, the LF3320 can process two matrix-vector multipliers simultaneously (i.e. [8x8][8x1]). In the single filter mode, the LF3320 can process a single matrix-vector multiply (i.e. [16x16][16x1]). This mode of operation allows the user to organize data values (e.g. pixels) into an array (e.g. blocks). This function is useful for any application requiring the operation of matrix multiplication; a function that is used when generating Discrete Cosine Transform coefficients (DCT) for the purpose of further processing.

When configuring the LF3320 for an [8x8][8x1] matrix-vector operation, the coefficient banks will require 8 coefficient sets to be loaded into the coefficient memory banks; each coefficient set will have 8, 12-bit coefficients. The input data, [8x1] column-vector, will be loaded through DIN11-0 for Filter A; either RIN11-0 or DIN11-0 can be the data input for Filter B. Conversely, when configured for a [16x16][16x1] matrix-vector operation, the coefficient banks will require 16 coefficient sets to be loaded into the coefficient memory banks; each coefficient set will have 16, 12-bit coefficients. The input data, [16x1] column-vector, will be loaded through DIN11-0.

To configure the LF3320 for matrix-vector multiplication, bit 4 of Configuration Register 5 must be set to 1 (Table 7). The configuration for single filter mode or dual filter mode will still apply. Writing 012H or 016H to Configuration Register 5 will configure the device for dual filter mode, [8x8][8x1] matrix-vector multiplication. Subsequently, writing 014H to Configuration Register 5 will configure the device for single filter

FIGURE 6. MATRIX-VECTOR MULTIPLY MODE

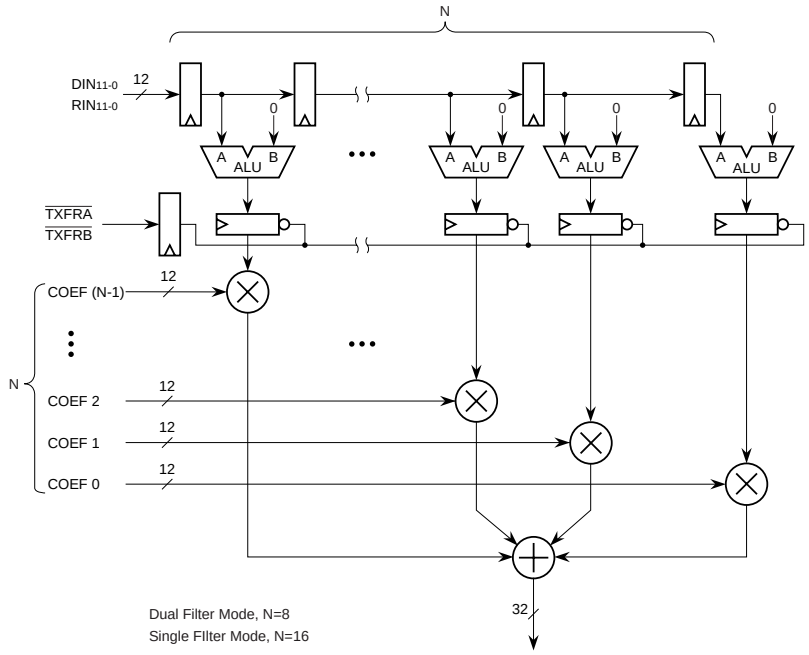


FIGURE 7. MATRIX EQUATION

C = COEFFICIENTS
D = DATA INPUT
R = DATA OUTPUT

$$\begin{bmatrix} R_0 \\ R_1 \\ R_2 \\ \vdots \\ R_i \end{bmatrix} = \begin{bmatrix} C_{00} & C_{01} & C_{02} & \cdots & C_{0j} \\ C_{10} & C_{11} & C_{12} & \cdots & C_{1j} \\ C_{20} & C_{21} & C_{22} & \cdots & C_{2j} \\ \vdots & & & & \vdots \\ C_{i0} & C_{i1} & C_{i2} & \cdots & C_{ij} \end{bmatrix} \cdot \begin{bmatrix} D_0 \\ D_1 \\ D_2 \\ \vdots \\ D_i \end{bmatrix}$$

$$\left[R_i\right] = \sum_{i=0}^{(N-1)} \left[C_{ij} \bullet D_i\right]$$

For j=0,1,2,...,(N-1)
N=8 or 16

mode, [16x16][16x1] matrix-vector multiplication.

Some functions of the LF3320 must be disabled when configured for matrix-vector multiplication. This will apply to both the single filter mode and the dual filter mode; these functions are data reversal and interleave / decimation. The LF3320 can be cascaded to realize larger matrices.

Data reversal can be disabled by setting bit 6, of Configuration Register 1 (Filter A) and Configuration Register 3 (Filter B), both to 1. The Odd-Tap, interleave mode will need to be disabled. Writing a 0 to bit 0 of Configuration Register 1 and Configuration Register 3 will disable the odd-tap interleave mode for Filter A and Filter B. When data is not being interleaved or decimated, the I / D Register length should be set to a length of one (Table 3 and Table 5). Therefore, writing 040H to Configuration Register 1 and 3 will disable the data reversal and set the corresponding inherent characteristics for the desired matrix function.

The Filter A ALU and Filter B ALU are to be configured for A+B (Table 2 and Table 4); so that condition A+0 is satisfied. To accomplish this, bit 0 is to be reset to 0, bit 1 is to be set to 1, and bit 2 is to be reset to 0. Writing 002H to Configuration Register 0 (Filter A) and Configuration Register 2 (Filter B) will set the corresponding registers to satisfy the A+0 condition.

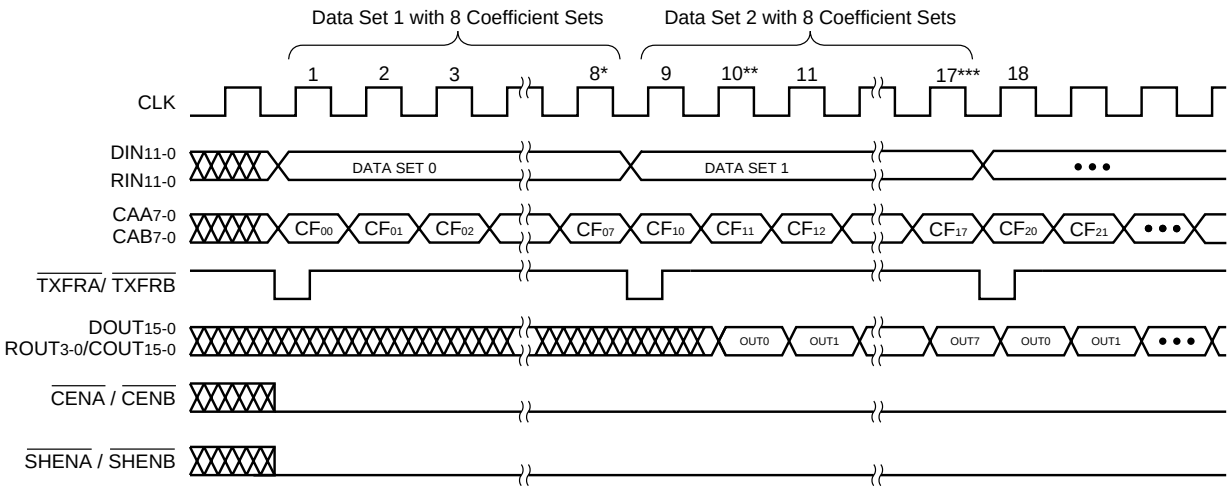
The timing diagrams in Figure 8 and 9 will assume that the Configuration Registers, the coefficient sets, and the first set of data values (data set) have been loaded. Loading input data for an [8x8][8x1] matrix operation requires 9 clock cycles and loading input data for a [16x16][16x1] matrix operation requires 17 clock cycles. When configured for an [8x8][8x1] matrix-vector operation, 8 data values are required for loading. When configured for a [16x16][16x1] matrix-vector operation, 16 data values are required for loading. Each data value is fed through the I / D Registers, using the corresponding input.

Once the final data value, of the data set, has been loaded $\overline{\text{TXFRA}}$ / $\overline{\text{TXFRB}}$ should be brought LOW for one clock cycle to complete the loading. Once this occurs, the data set is then bank loaded into the respective registers ready to begin the matrix-vector multiplication operation. The current data set will not change until $\overline{\text{TXFRA}}$ / $\overline{\text{TXFRB}}$ is brought LOW again. To satisfy the matrix equation (see Figure 7), the current data set is held for the duration of the required matrix dimension while cycling through each coefficient set ($\overline{\text{CENA}}$ / $\overline{\text{CENB}}$ must be held LOW). During this time new data values can be loaded serially, ready for the next activation of $\overline{\text{TXFRA}}$ / $\overline{\text{TXFRB}}$. To insure the correct evaluation of the matrix-vector multiplication equation, it is imperative that the coefficient values are paired with their corresponding data values.

For the [8x8][8x1] matrix-vector configuration (dual filter mode), the first result will appear 19 clock cycles from the first data input, DIN15-0 (Filter A) and RIN15-0 (Filter B); device latency for the first result is 10 clock cycles (10+9 = 19).

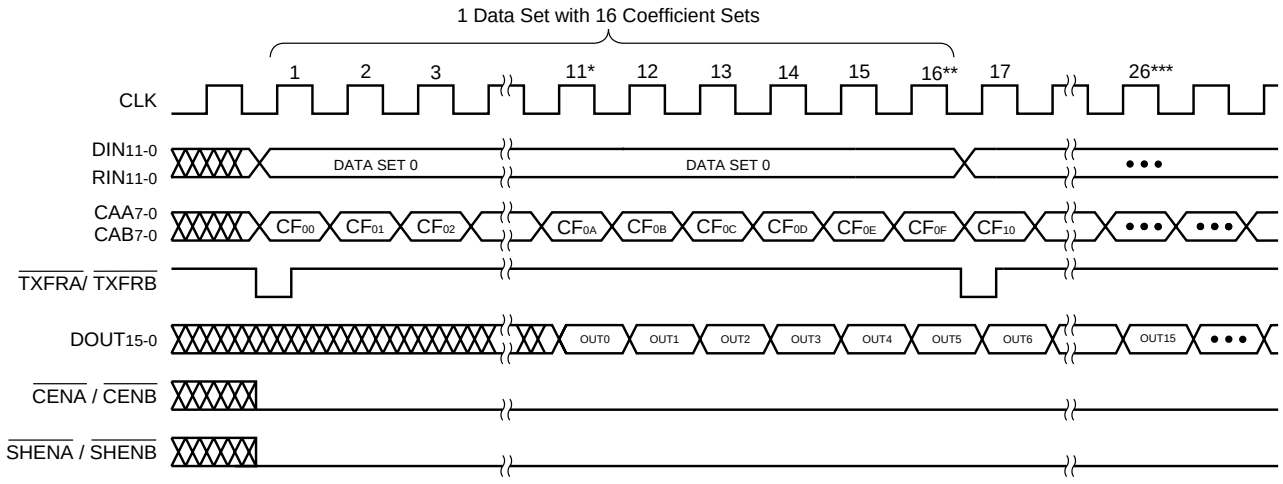
The result will appear at the corresponding filter output, DOUT15-0 (Filter A) and ROUT3-0 / COUT11-0 (Filter B). For the [16x16][16x1] matrix-vector configuration (single filter mode), the first result will appear

FIGURE 8. DUAL FILTER, MATRIX MULTIPLY TIMING SEQUENCE



* 8 Clocks - End of First Data/Coefficient Set
** 10 Clocks - First Output of First Data/Coefficient Set
*** 17 Clocks - Final Output of First Data/Coefficient Set

FIGURE 9. SINGLE FILTER, MATRIX MULTIPLY TIMING SEQUENCE

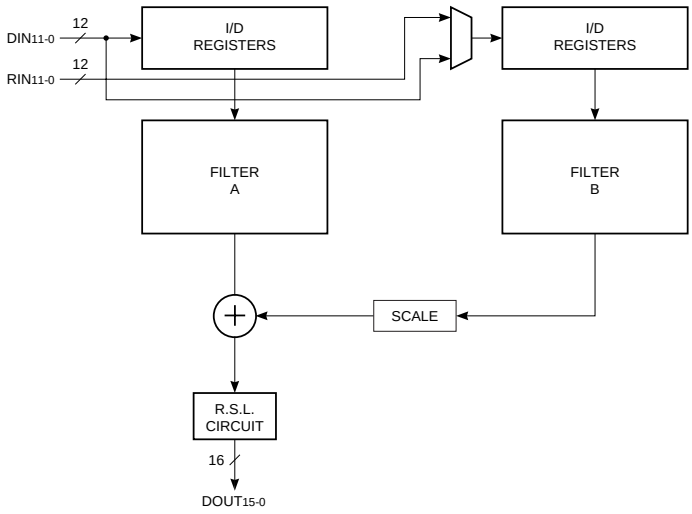


* 11 Clocks - First Output of First Data/Coefficient Set
** 16 Clocks - End of First Data/Coefficient Set
*** 26 Clocks - Final Output of First Data/Coefficient Set

28 clock cycles from the first data input, DIN15-0; device latency for the first result is 11 clock cycles (11+17 = 28). The result will appear at the corresponding filter output, DOUT15-0. Subsequently, for both dual and single filter mode configurations, the sum of products will continue to appear every clock cycle thereafter until the matrix dimension has been realized. The total pipeline latency for a complete [8x8][8x1] matrix-vector operation is 26 clock cycles and the total pipeline latency for a complete [16x16][16x1] matrix-vector operation is 43 clock cycles. Therefore, to process two square matrices simultaneoulsy, of size N=8, a total of 73 clock cycles are all that is required. Similarly, to process a single square matrix, of size N=16, a total of 283 clock cycles are required.

Once again, the timing diagrams (see Figure 8 and 9) will assume that the Configuration Registers, the coefficient sets, and the data values have been loaded. The corresponding timing diagram loading sequence for the coefficient banks and Configuration / Control registers are included in the LF3320 data sheets

FIGURE 10. DOUBLE WIDE DATA/COEFFICIENT MODE



(Figure 11 and Figure 12 respectively). Further reference to timing diagram loading sequence for the RSL registers are also included in the device data sheet (Figure 15, Figure 14, and Figure 13). The Filter A and Filter B LF Interface™ are used to load data into the Filter A and Filter B Configuration Registers and coefficient banks.

The Matrix Multiplication Mode is valid in the Double Wide Data / Coefficient Mode. However, there are some special considerations when this mode is desired. The LF3320 must be configured for single filter mode only, for a maximum (8x8) matrix. The user must disable the cascaded filter mode, the accumulator access mode, and the data reversal (see Table 7).

Double Wide Data/Coefficient Mode

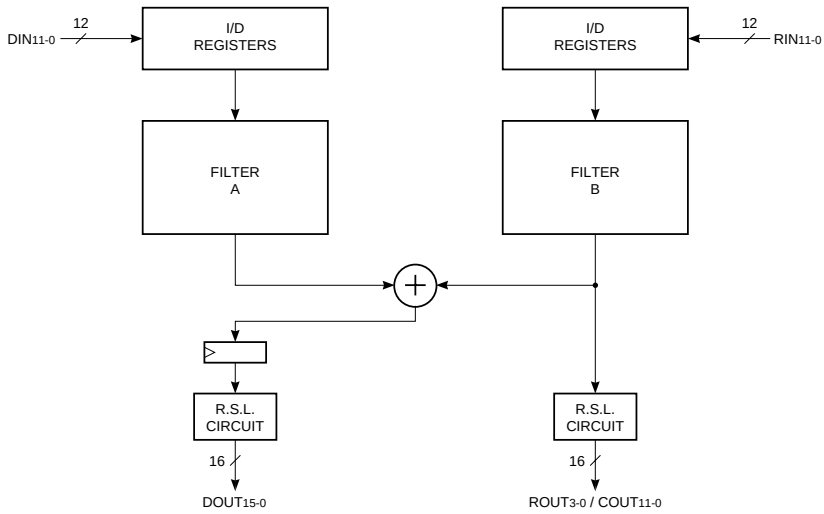
The LF3320 is capable of supporting 24-bit data and 12-bit coefficients or 12-bit data and 24-bit coefficients. When configured for this mode of operation, the Filter B output is scaled by 2^{-12} before adding it to the Filter A output. This mode of operation is only valid in single filter mode.

To configure the LF3320 for this mode, bit 3 of Configuration Register 5 must be set to 1; this will account for the scaling function (Table 7). For 24-bit data, DIN11-0 becomes the MSB (Filter A) and RIN11-0 becomes the LSB (Filter B), bit 2 of Configuration Register 5 must be set to 0. To insure correct results, the coefficient sets must be aligned appropriately; that is to say, the coefficient set used for the MSB must be the same for the LSB. For 24-bit coefficients, the coefficient banks for Filter A will correspond to the coefficient MSB and the coefficient banks for Filter B will correspond to the coefficient LSB; therefore, bit 2 must be set to 1.

Once again, to insure correct results, the coefficient sets must be aligned appropriately; that is to say, the MSB coefficients must correspond to their LSB coefficients. The output data will appear at DOUT15-0; output appearing at ROUT3-0 / COUT11-0 will not be of any value. Bit 1 is set to 0 (for single filter mode) and bit 0 is set to 0 (cascade mode must be disabled). Therefore, to realize 24-bit data / 12-bit coefficients the user must write 008H to Configuration Register 5; conversely, for 12-bit data / 24-bit coefficients the user must write 00CH to Configuration Register 5.

The Double Wide Data / Coefficient Mode is valid in the Matrix Multiplication Mode; however, special considerations must be observed when these two modes are combined. The LF3320 must be configured for single filter mode only, for a maximum (8x8) matrix. In addition, the user must disable the cascaded filter mode, the accumulator access mode, and the data reversal (Table 7). For additional considerations, refer to the corresponding mode of operation section.

FIGURE 11. ACCUMULATOR ACCESS MODE



Accumulator Access Mode

Accumulator access allows the user to accumulate the Filter A output with the Filter B output. Therefore, this mode is only valid when the device has been configured for dual filter operation. To configure the device for this mode, bit 1 and bit 5 must be set to 1; bit 5 is the corresponding accumulator access bit (Table 7). Writing 022H to Configuration Register 5 configures the device to accumulate the Filter A output with the Filter B output. All remaining Configuration Registers, 0 through 4 inclusive, will depend on specific application requirements (see Tables 2 through 4). In this mode of operation, the accumulated output is realized at DOUT15-0. The output data at ROUT15-0 / COUT15-0 is the Filter B output that is normally expected; however, the accumulated output data (DOUT15-0) will be delayed by one clock cycle, compared to the Filter B output data.

This type of operation is useful when two filtered data streams (i.e. I+jQ) need to be accumulated. Such is the requirement to satisfy the equation, $y(t) = \cos(vt)+j\sin(vt)$. The complex data can be streamed and filtered using a respective 'I' filter and 'Q' filter. To convert the complex result into a real result, as seen at the LF3320 output, two multiplies and one accumulation is required. The cosine and sine functions are realized through the coefficient sets; consequently, multiplied by the corresponding 'I' and 'Q' data streams. To satisfy the remainder of the equation, Filter A and Filter B must be accumulated.

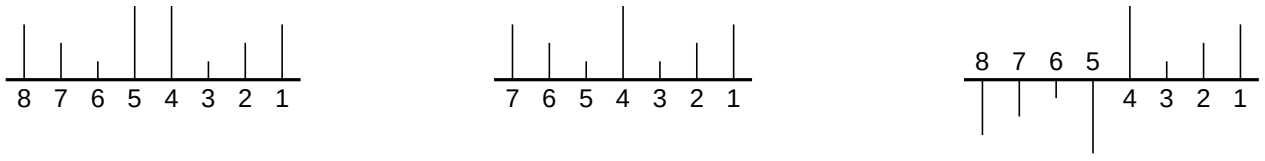
As previously stated, this mode of operation is only valid with the dual filter mode configuration. All modes of operation, that are valid in the dual filter mode, are valid with the accumulator access mode. For additional considerations, refer to the corresponding mode of operation section.

FUNCTIONAL DESCRIPTION

ALUs

The ALUs double the number of filter taps available, when symmetric coefficient sets are used, by pre-adding data values which are then multiplied by a common coefficient (see Figure 12).

FIGURE 12. SYMMETRIC COEFFICIENT SET EXAMPLES

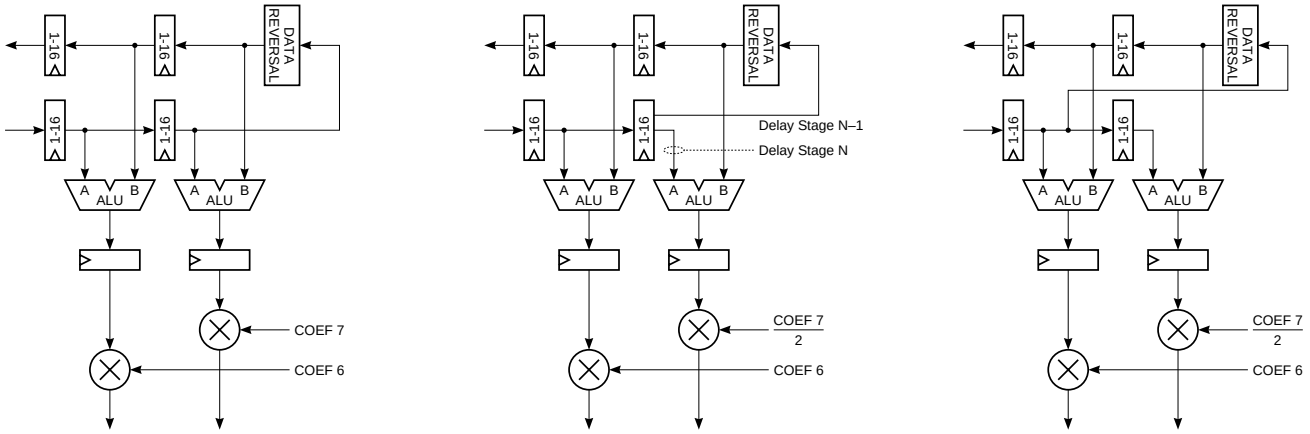


Even-Tap, Even-Symmetric Coefficient Set

Odd-Tap, Even-Symmetric Coefficient Set

Even-Tap, Odd-Symmetric Coefficient Set

FIGURE 13. I/D REGISTER DATA PATHS



EVEN-TAP MODE

ODD-TAP MODE

ODD-TAP INTERLEAVE MODE

The ALUs can perform two operations: A+B and B–A. Bit 0 of Configuration Register 0 determines the operation of the ALUs in Filter A.

Bit 0 of Configuration Register 2 determines the operation of the ALUs in Filter B. A+B is used with even-symmetric coefficient sets. B–A is used with odd-symmetric coefficient sets.

Also, either the A or B operand may be set to 0. Bits 1 and 2 of Configuration Register 0 and Configuration Register 2 control the ALU inputs in Filters A and B respectively. A+0 or B+0 are used with asymmetric coefficient sets.

Interleave/Decimation Registers

The Interleave / Decimation Registers (I / D Registers) feed the ALU inputs. They allow the device to filter up to sixteen data sets interleaved into the same data stream without having to separate the data sets. The I / D Registers should be set to a length equal to the number of data sets interleaved together.

For example, if two data sets are interleaved together, the I / D Registers should be set to a length of two. Bits 1 through 4 of Configuration Register 1 and Configuration Register 3 determine the length of the I / D Registers in Filters A and B respectively.

The I / D Registers also facilitate using decimation to increase the number of filter taps. Decimation by N is accomplished by reading the filter's output once every N clock cycles. The device supports decimation up to 16:1. With no decimation, the maximum number of filter taps is sixteen. When decimating by N, the number of filter taps becomes 16N because there are N–1 clock cycles when the filter's output is not being read. The extra clock cycles are used to calculate more filter taps.

When decimating, the I / D Registers should be set to a length equal to the decimation factor. For example, when performing a 4:1 decimation, the I / D Registers should be set to a length of four. When decimation is disabled or when only one data set (non-interleaved data) is fed into the device, the I / D Registers should be set to a length of one.

TABLE 2. CONFIGURATION REGISTER 0 – ADDRESS 200H

BITS	FUNCTION	DESCRIPTION
0	ALU Mode Filter A	0 : A + B 1 : B – A
1	Pass A Filter A	0 : ALU Input A = 0 1 : ALU Input A = Forward Register Path
2	Pass B Filter A	0 : ALU Input B = 0 1 : ALU Input B = Reverse Register Path
11-3	Reserved	Should be set to “0”

TABLE 3. CONFIGURATION REGISTER 1 – ADDRESS 201H

BITS	FUNCTION	DESCRIPTION
0	Filter A Odd-Tap Interleave Mode	0 : Odd-Tap Interleave Mode Disabled 1 : Odd-Tap Interleave Mode Enabled
4-1	Filter A I/D Register Length	0000 : 1 Register 0001 : 2 Registers 0010 : 3 Registers 0011 : 4 Registers 0100 : 5 Registers 0101 : 6 Registers 0110 : 7 Registers 0111 : 8 Registers 1000 : 9 Registers 1001 : 10 Registers 1010 : 11 Registers 1011 : 12 Registers 1100 : 13 Registers 1101 : 14 Registers 1110 : 15 Registers 1111 : 16 Registers
5	Filter A Tap Number	0 : Even Number of Taps 1 : Odd Number of Taps
6	Filter A Data Reversal	0 : Data Reversal Enabled 1 : Data Reversal Disabled
11-7	Reserved	Should be set to “0”

I/D Register Data Path Control

The three multiplexers in the I / D Register data path control how data is routed through the forward and reverse data paths.

The forward data path contains the I / D Registers in which data flows from left to right in the block diagram in Figure 1. The reverse data path contains the I / D Registers in which data flows from right to left.

In Single or Dual Filter Modes, data is fed from the forward data path to the reverse data path as follows. When the filter is configured for an even number of taps, data from the last I / D Register in the forward data path is fed into the first I / D Register in the reverse data path (see Figure 13). When the filter is configured for an odd number of taps, the data which will appear at the output of the last I / D Register in the forward data path on the next clock cycle is fed into the first I / D Register in the reverse data path. Bit 5 in Configuration Register 1 and Configuration Register 3 configures Filters A and B respectively for an even or odd number of taps.

When interleaved data is fed through the device and an even tap filter is desired, the filter should be configured for an even number of taps and the I / D Register length should match the number of data sets interleaved together. When interleaved data is fed through the device and an odd tap filter is desired, the filter should be set to Odd-Tap Interleave Mode. Bit 0 of Configuration Register 1 and Configuration Register 3 configures Filters A and B respectively for Odd-Tap Interleave Mode. When the filter is configured for Odd-Tap Interleave Mode, data from the next to last I / D Register in the forward data path is fed into the first I / D Register in the reverse data path.

When the filter is configured for an odd number of taps (interleaved or non-interleaved modes), the filter is structured such that the center data value is aligned simultaneously at the A and B inputs of the last ALU in the forward data path. In order to achieve the correct result, the user must divide the coefficient by two.

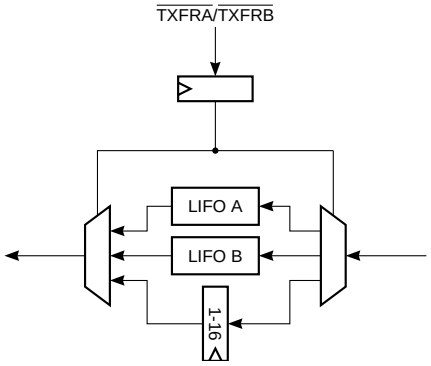
Data Reversal

Data reversal circuitry is placed after the multiplexers which route data from the forward data path to the reverse data path (see Figure 14). When decimating, the data stream must be reversed in order for data to be properly aligned at the inputs of the ALUs.

When data reversal is enabled, the circuitry uses a pair of LIFOs to reverse the order of the data sent to the reverse data path. TXFRA and TXFRB control the LIFOs in Filters A and B respectively. When TXFRA / TXFRB goes LOW, the LIFO sending data to the reverse data path becomes the LIFO receiving data from the forward data path, and the LIFO receiving data from the forward data path becomes the LIFO sending data to

the reverse data path. The device must see a HIGH to LOW transition of TXFRA / TXFR B in order to switch LIFOs. If decimating by N, TXFRA / TXFRB should go LOW once every N clock cycles. When data reversal is disabled, the circuitry functions like an I / D Register. When feeding interleaved data through the filter, data reversal should be disabled. Bit 6 of Configuration Register 1 and Configuration Register 3 enables or disables data reversal for Filters A and B respectively.

FIGURE 14. DATA REVERSAL



Cascading

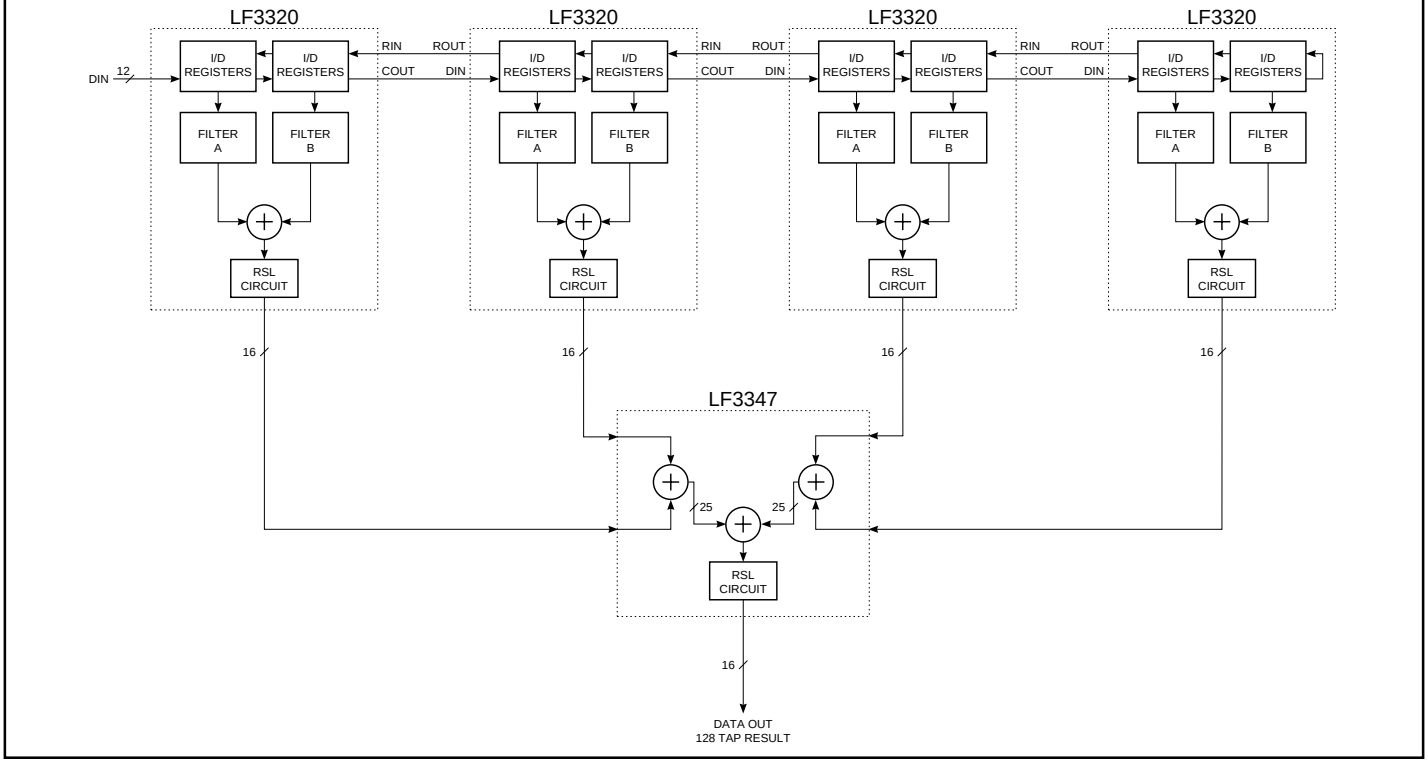
Three cascade ports are provided to allow cascading of multiple devices for more filter taps (see Figure 15). COUT11-0 of one device should be connected to DIN11-0 of another device. ROUT11-0 of one device should be connected to RIN11-0 of another device. As many LF3320s as desired may be cascaded together. However, the outputs of the LF3320s must be added together with external adders.

Bit 0 of Configuration Register 5 determines how the device will send data to the reverse data path when multiple LF3320s are cascaded together. If a LF3320 is the last in the cascade chain, Bit 0 of Configuration Register 5 should be set to a "0". This will cause the data from the end of the forward data path to be routed to the beginning of the reverse data path based on how the filter is configured (even / odd number of taps or interleave mode). If a LF3320 is not the last in the cascade chain, Bit 0 of Configuration Register 5 should be set to a "1". This will cause RIN11-0 to feed data to the reverse data path. When not cascading, Bit 0 of Configuration Register 5 should be set to a "0".

Special data routing circuitry is used to feed the COUT and ROUT output registers. The data routing circuitry is required to correctly align data in the forward and reverse data paths as data passes from one LF3320 to another.

The COUT and ROUT registers are loaded with data which is two clock cycles behind the current output of the I / D Register just before the ROUT or COUT register. This correctly accounts for the extra delays added to the forward and reverse data paths by the input / output cascade registers.

FIGURE 15. MULTIPLE LF3320S CASCADED TOGETHER



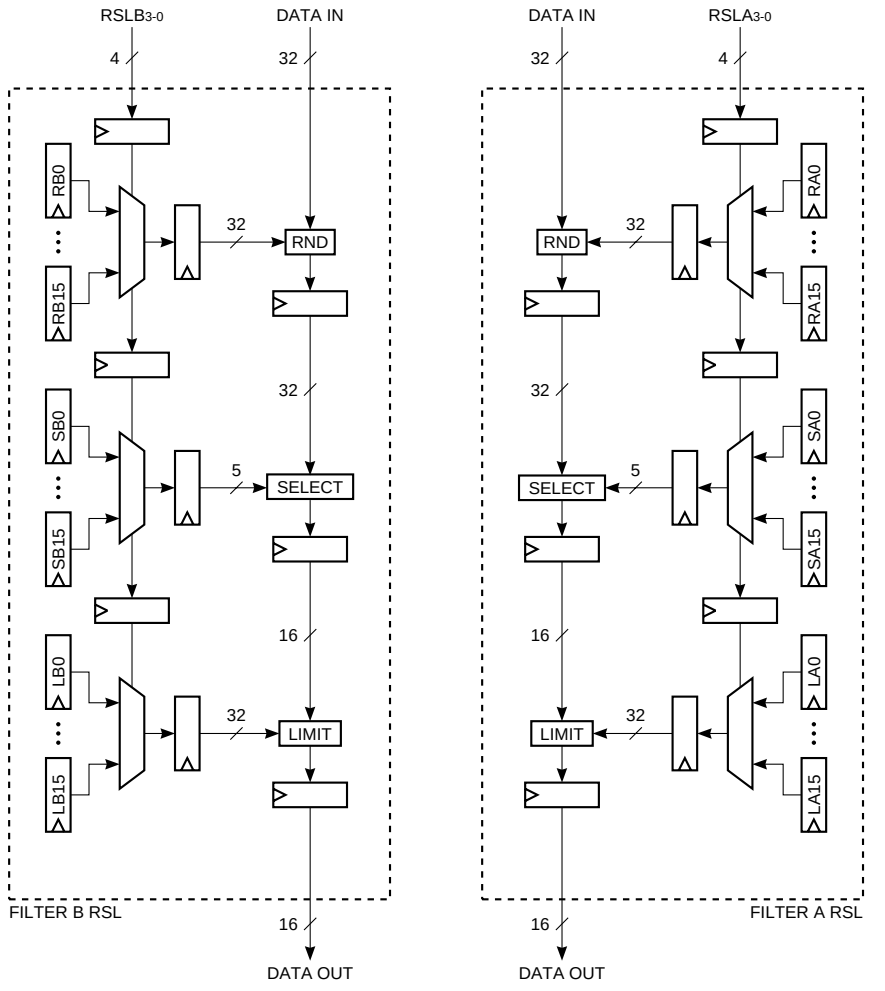
Output Adder

The Output Adder adds the Filter A and B outputs together when the device is in Single Filter Mode. If 24-bit data and 12-bit coefficients or 12-bit data and 24-bit coefficients are desired, the LF3320 can facilitate this by scaling the Filter B output by 2^{-12} before adding it to the Filter A output. Bit 3 in Configuration Register 5 determines if the Filter B output is scaled before being added to the Filter A output.

Rounding

The overall filter output (Single Filter Mode) or Filter A and B outputs (Dual Filter Mode) may be rounded by adding the contents of one of the sixteen Filter A or B round registers to the overall filter, Filter A, or Filter B outputs (see Figure 10). The Filter A round registers are used for the overall filter (Single Filter Mode) or Filter A (Dual Filter Mode). The Filter B round registers are used for Filter B (Dual Filter Mode). Each round register is 32-bits wide and user-programmable. This allows the filter's output to be rounded to any precision required. Since any 32-bit value may be programmed into the round registers, the device can support complex rounding algorithms as well as standard Half-LSB rounding. RSLA3-0 determines which of the sixteen Filter A round registers are used in the Filter A rounding circuitry. RSLB3-0 determines which of the sixteen Filter B round registers are used in the Filter B rounding circuitry. A value of 0 on RSLA / RSLB3-0 selects Filter A / B round register 0. A value of 1 selects Filter A / B round register 1 and so on. RSLA / RSLB3-0 may be changed every clock cycle if desired. This allows the rounding algorithm to be changed every clock cycle. This is useful when filtering interleaved data. If rounding is not desired, a round register should be loaded with 0 and selected as the register used for rounding. Round register loading is discussed in the LF Interface™ section.

FIGURE 16. FILTER A AND B ROUND/SELECT/LIMIT CIRCUITRY



Output Select

The word width of the overall filter, Filter A, and Filter B outputs is 32-bits. However, only 16-bits may be sent to DOUT15-0 (Single or Dual Filter Modes) and COUT11-0 / ROUT3-0 (Dual Filter Mode). The Filter A / B select circuitry determines which 16-bits are passed (see Table 1). The Filter A / B select registers control the Filter A / B select circuitry. There are sixteen Filter A and B select registers.

The Filter A select registers are used for the overall filter (Single Filter Mode) or Filter A (Dual Filter Mode). The Filter B select registers are used for Filter B (Dual Filter Mode). Each select register is 5 bits wide and user-programmable. RSLA3-0 determines which of the sixteen Filter A select registers are used in the Filter A select circuitry. RSLB3-0 determines which of the sixteen Filter B select registers are used in the Filter B select circuitry. A value of 0 on RSLA / RSLB3-0 selects Filter A / B select register 0. A value of 1 selects Filter A / B select register 1 and so on. RSLA / RSLB3-0 may be changed every clock cycle if desired. This allows the 16-bit window to be changed every clock cycle. This is useful when filtering interleaved data. Select register loading is discussed in the LF Interface™ section.

TABLE 4. CONFIGURATION REGISTER 2 – ADDRESS 202H

BITS	FUNCTION	DESCRIPTION
0	ALU Mode Filter B	0 : A + B 1 : B – A
1	Pass A Filter B	0 : ALU Input A = 0 1 : ALU Input A = Forward Register Path
2	Pass B Filter B	0 : ALU Input B = 0 1 : ALU Input B = Reverse Register Path
11-3	Reserved	Must be set to “0”

TABLE 5. CONFIGURATION REGISTER 3 – ADDRESS 203H

BITS	FUNCTION	DESCRIPTION
0	Filter B Odd-Tap Interleave Mode	0 : Odd-Tap Interleave Mode Disabled 1 : Odd-Tap Interleave Mode Enabled
4-1	Filter B I/D Register Length	0000 : 1 Register 0001 : 2 Registers 0010 : 3 Registers 0011 : 4 Registers 0100 : 5 Registers 0101 : 6 Registers 0110 : 7 Registers 0111 : 8 Registers 1000 : 9 Registers 1001 : 10 Registers 1010 : 11 Registers 1011 : 12 Registers 1100 : 13 Registers 1101 : 14 Registers 1110 : 15 Registers 1111 : 16 Registers
5	Filter B Tap Number	0 : Even Number of Taps 1 : Odd Number of Taps
6	Filter B Data Reversal	0 : Data Reversal Enabled 1 : Data Reversal Disabled
11-7	Reserved	Must be set to “0”

Output Limiting

An output limiting function is provided for the overall filter, Filter A, and Filter B outputs. The Filter A limiting circuitry is used to limit the overall filter output (Single Filter Mode) and the Filter A output (Dual Filter Mode). The Filter B limiting circuitry is used to limit the Filter B output (Dual Filter Mode). The Filter A and B limit registers determine the valid range of output values for the Filter A and B limiting circuitry respectively. There are sixteen 32-bit user-programmable limit registers for both Filters A and B. The Filter A limit registers are used for the overall filter (Single Filter Mode) or Filter A (Dual Filter Mode). The Filter B limit registers are used for Filter B (Dual Filter Mode). RSLA3-0 determines which of the sixteen Filter A limit registers are used in the Filter A limit circuitry. RSLB3-0 determines which of the sixteen Filter B limit registers are used in the Filter B limit circuitry. A value of 0 on RSLA / RSLB3-0 selects Filter A / B limit register 0. A value of 1 selects Filter A / B limit register 1 and so on. Each limit register contains an upper and lower limit value. If the value fed to the limiting circuitry is less than the lower limit, the lower limit value is passed as the filter output. If the value fed to the limiting circuitry is greater than the upper limit, the upper limit value is passed as the filter output. Bit 1 and 0 in Configuration Register 4 enable and disable Filter A and B limiting respectively. RSLA / RSLB3-0 may be changed every clock cycle if desired. This allows the limit range to be changed every clock cycle. This is useful when filtering interleaved data. When loading limit values into the device, the upper limit must be greater than the lower limit. Limit register loading is discussed in the LF Interface™ section.

Coefficient Banks

The coefficient banks store the coefficients which feed into the multipliers in Filters A and B. There is a separate bank for each multiplier. Each bank can hold 256 12-bit coefficients. The banks are loaded using an LF Interface™. There is a separate LF Interface™ for the Filter A and B banks. Coefficient bank loading is discussed in the LF Interface™ section.

Configuration and Control Registers

The configuration registers determine how the LF3320 operates. Tables 2 through 7 show the formats of the six configuration registers. There are three types of control registers: round, select, and limit. There are sixteen round registers for Filter A and sixteen for Filter B. Each register is 32 bits wide. RSLA3-0 and RSLB3-0 determine which Filter A and B round registers respectively are used for rounding.

There are sixteen select registers for Filter A and sixteen for Filter B. Each register is 5 bits wide. RSLA3-0 and RSLB3-0 determine which Filter A and B select registers respectively are used in the select circuitry.

There are sixteen limit registers for Filter A and sixteen for Filter B. Each register is 32-bits wide and stores both an upper and lower limit value. The lower limit is stored in bits 15-0 and the upper limit is stored in bits 31-16. RSLA3-0 and RSLB3-0 determine which Filter A and B limit registers respectively are used for limiting when limiting is enabled. Configuration and control register loading is discussed in the LF Interface™ section.

LF Interface™

The Filter A and B LF Interfaces™ are used to load data into the Filter A and B coefficient banks respectively. They are also used to load data into the configuration and control registers.

The following section describes how the Filter A LF Interface™ works. The Filter A and B LF Interfaces™ are identical in function. If $\overline{LDA}$ and CFA11-0 are replaced with $\overline{LDB}$ and CFB11-0, the following section will describe how the Filter B LF Interface™ works.

$\overline{LDA}$ is used to enable and disable the Filter A LF Interface™. When $\overline{LDA}$ goes LOW, the Filter A LF Interface™ is enabled for data input. The first value fed into the interface on CFA11-0 is an address which determines what the interface is going to load. The three most significant bits (CFA11-9) determine if the LF Interface™ will load coefficient banks or Configuration / control registers (see Table 8). The nine least significant bits (CFA8-0) are the address for whatever is to be loaded (see Tables 9 through 14). For example, to load address 15 of the Filter A coefficient banks, the first data value into the LF Interface™ should be 00FH. To load Filter A limit register 10, the first data value should be C0AH. The first address value should be loaded into the interface on the same clock cycle that latches the HIGH to LOW transition of $\overline{LDA}$ (see Figures 17 and 18).

TABLE 6. CONFIGURATION REGISTER 4 – ADDRESS 204H

BITS	FUNCTION	DESCRIPTION
0	Filter B Limit Enable	0 : Limiting Disabled 1 : Limiting Enabled
1	Filter A Limit Enable	0 : Limiting Disabled 1 : Limiting Enabled
11-2	Reserved	Must be set to “0”

TABLE 7. CONFIGURATION REGISTER 5 – ADDRESS 205H

BITS	FUNCTION	DESCRIPTION
0	Cascade Mode	0 : Last In Line 1 : First or Middle in Line
1	Single/Dual Filter Mode	0 : Single Filter Mode 1 : Dual Filter Mode
2	Filter B Input	0 : RIN11-0 1 : DIN11-0
3	Output Adder Control	0 : Filter A + Filter B 1 : Filter A + Filter B (Filter B Scaled by 2^{-12})
4	Matrix Multiply Mode	0 : Disabled 1 : Enabled
5	Accumulator Access Mode	0 : Disabled 1 : Enabled
11-6	Reserved	Must be set to “0”

The next value(s) loaded into the interface are the data value(s) which will be stored in the bank or register defined by the address value. When loading coefficient banks, the interface will expect eight values to be loaded into the device after the address value. The eight values are coefficients 0 through 7. When loading configuration or select registers, the interface will expect one value after the address value. When loading round or limit registers, the interface will expect four values after the address value. Figures 11 and 12 show the data loading sequences for the coefficient banks and Configuration / control registers.

Both PAUSEA and PAUSEB allow the user to effectively slow the rate of data loading through the LF Interface™. When PAUSEA is HIGH, the LF Interface™ affecting the data used for Filter A is held until PAUSEA is returned to a LOW. When PAUSEB is HIGH, the LF Interface™ affecting the data used for Filter B is held until PAUSEB is returned to a LOW. Figures 19 through 22 display the effects of both PAUSEA and PAUSEB while loading coefficient and control data.

Table 15 shows an example of loading data into the coefficient banks. The following data values are written into address 10 of coefficient banks 0 through 7: 210H, 543H, C76H, 9E3H, 701H, 832H, F20H, 143H. Table 16 shows an example of loading data into a Configuration Register. Data value 003H is written into Configuration Register 4. Table 17 shows an example of loading data into a round register. Data value 7683F4A2H is written into Filter A round register 12.

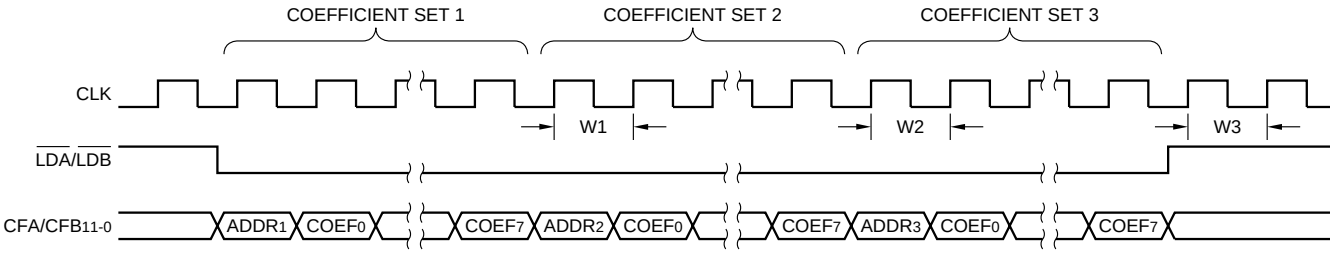
Table 18 shows an example of loading data into a select register. Data value 00FH is loaded into Filter A select register 2. Table 19 shows an example

of loading data into Filter B limit register 7. Data value 3B60H is loaded as the lower limit and 72A4H is loaded as the upper limit.

It takes 9S clock cycles to load S coefficient sets into the device. Therefore, it takes 2304 clock cycles to load all 256 coefficient sets. Assuming an 83 MHz clock rate, all 256 coefficient sets can be updated in less than 27.7 µs, which is well within vertical blanking time. It takes 5S clock cycles to load S round or limit registers. Therefore, it takes 320 clock cycles to update all round and limit registers (both Filters A and B). Assuming an 83 MHz clock rate, all Filter A and B round / limit registers can be updated in 3.84 µs.

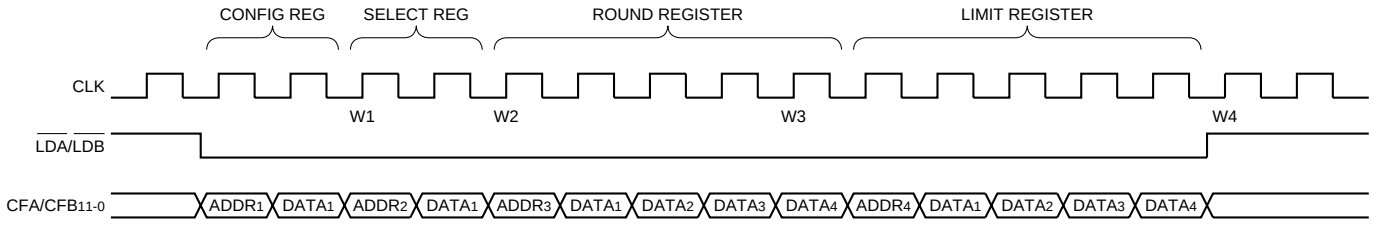
The coefficient banks and Configuration / Control registers are not loaded with data until all data values for the specified address are loaded into the LF Interface™. In other words, the coefficient banks are not written to until all eight coefficients have been loaded into the LF Interface™. A round register is not written to until all four data values are loaded.

FIGURE 17. COEFFICIENT BANK LOADING SEQUENCE



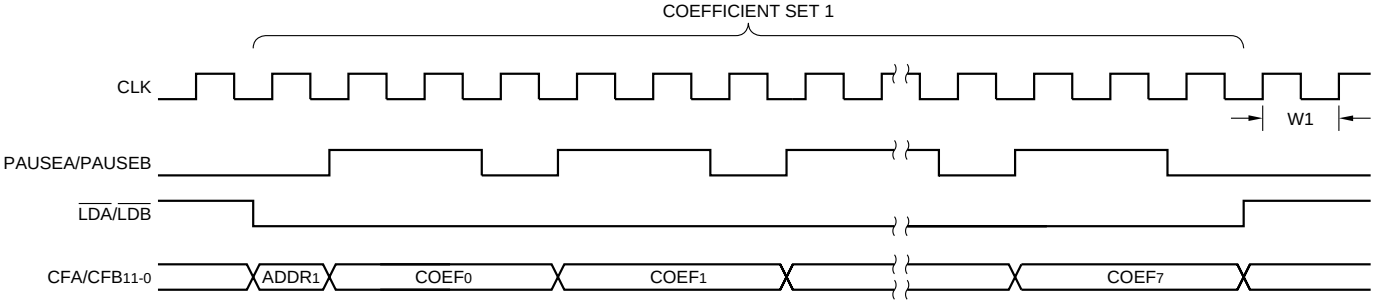
W1: Coefficient Set 1 written to coefficient banks during this clock cycle.
W2: Coefficient Set 2 written to coefficient banks during this clock cycle.
W3: Coefficient Set 3 written to coefficient banks during this clock cycle.

FIGURE 18. CONFIGURATION/CONTROL REGISTER LOADING SEQUENCE



W1: Configuration Register loaded with new data on this rising clock edge.
W2: Select Register loaded with new data on this rising clock edge.
W3: Round Register loaded with new data on this rising clock edge.
W4: Limit Register loaded with new data on this rising clock edge.

FIGURE 19. COEFFICIENT BANK LOADING SEQUENCE WITH PAUSE IMPLEMENTATION



W1: Coefficient Set 1 written to coefficient banks during this clock cycle.

After the last data value is loaded, the interface will expect a new address value on the next clock cycle. After the next address value is loaded, data loading will begin again as previously discussed. As long as data is loaded into the interface, $\overline{LDA}$ must remain LOW. After all desired coefficient banks and Configuration / Control registers are loaded with data, the LF Interface™ must be disabled. This is done by setting $\overline{LDA}$ HIGH on the clock cycle after the clock cycle which latches the last data value. It is important that the LF Interface™ remain disabled when not loading data into it.

The Filter A coefficient banks may only be loaded with the Filter A LF Interface™ and the Filter B coefficient banks may only be loaded with the Filter B LF Interface™.

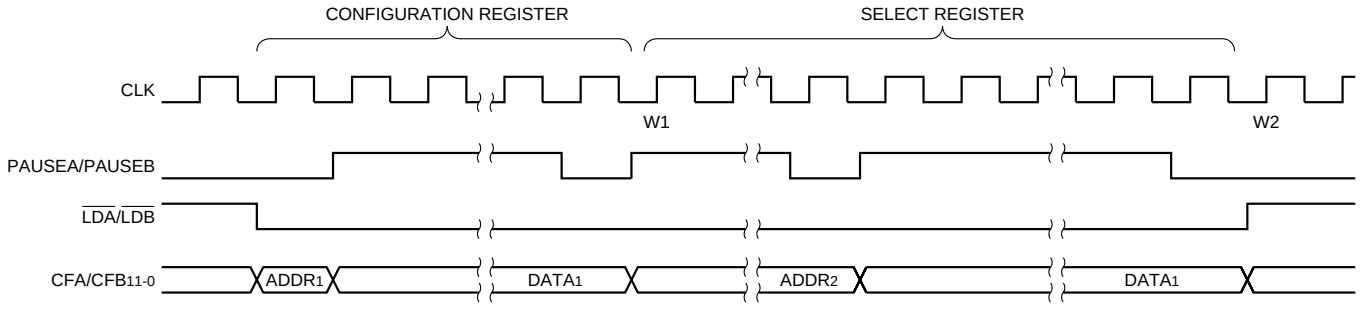
The Configuration and Control registers may be loaded with either the Filter A or B LF Interfaces™.

Since both LF Interfaces™ operate independently of each other, both LF Interfaces™ can load data into their respective coefficient banks at the same time. Or, one LF Interface™ can load the Configuration / Control registers while the other loads it's respective coefficient banks. If both LF Interfaces™ are used to load a Configuration or Control register at the same time, the Filter B LF Interface™ will be given priority over the Filter A LF Interface™. For example, if the Filter A LF Interface™ attempts to load data into a configuration register at the same time that the Filter B LF Interface™ attempts to load a Filter A round register, the Filter B LF Interface™ will be allowed to load the round register while the Filter A LF Interface™ will not be allowed to load the configuration register. However, the Filter A LF Interface™ will continue to function as if the write occurred.

TABLE 8. CFA/CFB11-9 DECODE

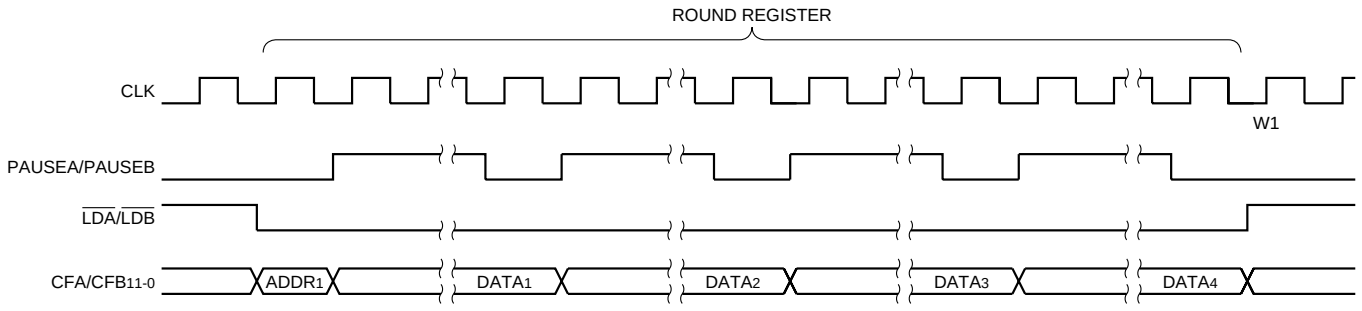
11	10	9	DESCRIPTION
0	0	0	Coefficient Banks
0	0	1	Configuration Registers
0	1	0	Filter A Select Registers
0	1	1	Filter B Select Registers
1	0	0	Filter A Round Registers
1	0	1	Filter B Round Registers
1	1	0	Filter A Limit Registers
1	1	1	Filter B Limit Registers

FIGURE 20. CONFIGURATION AND SELECT REGISTER LOADING SEQUENCE WITH PAUSE IMPLEMENTATION



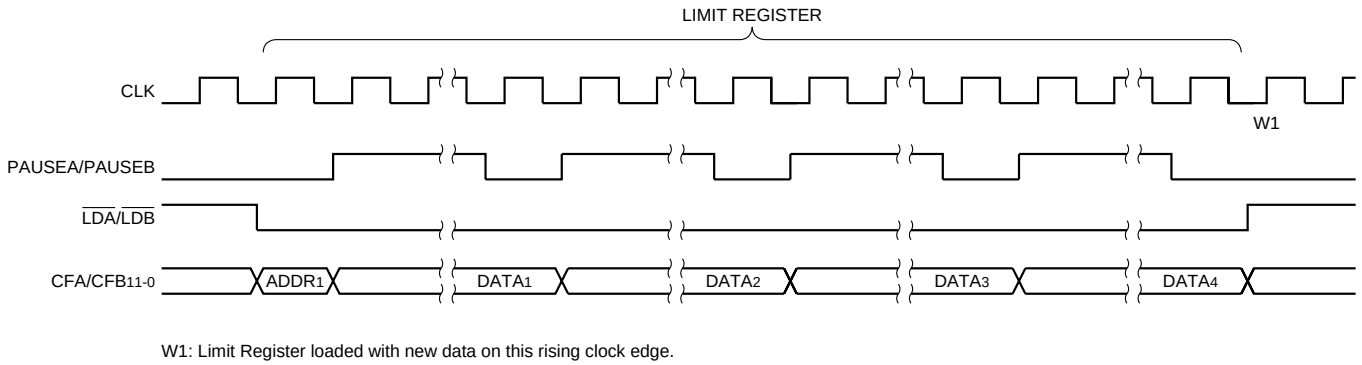
W1: Configuration Register loaded with new data on this rising clock edge.
W2: Select Register loaded with new data on this rising clock edge.

FIGURE 21. ROUND REGISTER LOADING SEQUENCE WITH PAUSE IMPLEMENTATION



W1: Round Register loaded with new data on this rising clock edge.

FIGURE 22. LIMIT REGISTER LOADING SEQUENCE WITH PAUSE IMPLEMENTATION



W1: Limit Register loaded with new data on this rising clock edge.

TABLE 9. FLTR. A ROUND REGISTERS

REGISTER	ADDRESS (HEX)
0	800
1	801
•	•
•	•
•	•
14	80E
15	80F

TABLE 10. FLTR.A SELECT REGISTERS

REGISTER	ADDRESS (HEX)
0	400
1	401
•	•
•	•
•	•
14	40E
15	40F

TABLE 11. FLTR. A LIMIT REGISTERS

REGISTER	ADDRESS (HEX)
0	C00
1	C01
•	•
•	•
•	•
14	C0E
15	C0F

TABLE 12. FLTR. B ROUND REGISTERS

REGISTER	ADDRESS (HEX)
0	A00
1	A01
•	•
•	•
•	•
14	A0E
15	A0F

TABLE 13. FLTR.B SELECT REGISTERS

REGISTER	ADDRESS (HEX)
0	600
1	601
•	•
•	•
•	•
14	60E
15	60F

TABLE 14. FLTR. B LIMIT REGISTERS

REGISTER	ADDRESS (HEX)
0	E00
1	E01
•	•
•	•
•	•
14	E0E
15	E0F

TABLE 15. COEFFICIENT BANK LOADING FORMAT

	CFA/B11	CFA/B10	CFA/B9	CFA/B8	CFA/B7	CFA/B6	CFA/B5	CFA/B4	CFA/B3	CFA/B2	CFA/B1	CFA/B0
1st Word - Address	0	0	0	0	0	0	0	0	1	0	1	0
2nd Word - Bank 0	0	0	1	0	0	0	0	1	0	0	0	0
3rd Word - Bank 1	0	1	0	1	0	1	0	0	0	0	1	1
4th Word - Bank 2	1	1	0	0	0	1	1	1	0	1	1	0
5th Word - Bank 3	1	0	0	1	1	1	1	0	0	0	1	1
6th Word - Bank 4	0	1	1	1	0	0	0	0	0	0	0	1
7th Word - Bank 5	1	0	0	0	0	0	1	1	0	0	1	0
8th Word - Bank 6	1	1	1	1	0	0	1	0	0	0	0	0
9th Word - Bank 7	0	0	0	1	0	1	0	0	0	0	1	1

TABLE 16. CONFIGURATION REGISTER LOADING FORMAT

	CFA/B11	CFA/B10	CFA/B9	CFA/B8	CFA/B7	CFA/B6	CFA/B5	CFA/B4	CFA/B3	CFA/B2	CFA/B1	CFA/B0
1st Word - Address	0	0	1	0	0	0	0	0	0	1	0	0
2nd Word - Data	0	0	0	0	0	0	0	0	0	0	1	1

TABLE 17. ROUND REGISTER LOADING FORMAT

	CFA/B11	CFA/B10	CFA/B9	CFA/B8	CFA/B7	CFA/B6	CFA/B5	CFA/B4	CFA/B3	CFA/B2	CFA/B1	CFA/B0
1st Word - Address	1	0	0	0	0	0	0	0	1	1	0	0
2nd Word - Data	R	R	R	R	1	0	1	0	0	0	1	0*
3rd Word - Data	R	R	R	R	1	1	1	1	0	1	0	0
4th Word - Data	R	R	R	R	1	0	0	0	0	0	1	1
5th Word - Data	R	R	R	R	0**	1	1	1	0	1	1	0

TABLE 18. SELECT REGISTER LOADING FORMAT

	CFA/B11	CFA/B10	CFA/B9	CFA/B8	CFA/B7	CFA/B6	CFA/B5	CFA/B4	CFA/B3	CFA/B2	CFA/B1	CFA/B0
1st Word - Address	0	1	0	0	0	0	0	0	0	0	1	0
2nd Word - Data	0	0	0	0	0	0	0	0	1	1	1	1

TABLE 19. LIMIT REGISTER LOADING FORMAT

	CFA/B11	CFA/B10	CFA/B9	CFA/B8	CFA/B7	CFA/B6	CFA/B5	CFA/B4	CFA/B3	CFA/B2	CFA/B1	CFA/B0
1st Word - Address	1	1	1	0	0	0	0	0	0	1	1	1
2nd Word - Data	R	R	R	R	0	1	1	0	0	0	0	0
3rd Word - Data	R	R	R	R	0*	0	1	1	1	0	1	1
4th Word - Data	R	R	R	R	1	0	1	0	0	1	0	0
5th Word - Data	R	R	R	R	0**	1	1	1	0	0	1	0

R = Reserved. Must be set to "0".
* This bit represents the MSB of the Lower Limit.
** This bit represents the MSB of the Upper Limit.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
V_{CC} supply voltage with respect to ground ..... –0.5 V to +4.5 V
Input signal with respect to ground ..... –0.5 V to 5.5 V
Signal applied to high impedance output ..... –0.5 V to 5.5 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA
ESD Classification (MIL-STD-883E METHOD 3015.7) ..... Class 3

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	3.00 V ≤ V_{CC} ≤ 3.60 V
Active Operation, Military	–55°C to +125°C	3.00 V ≤ V_{CC} ≤ 3.60 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

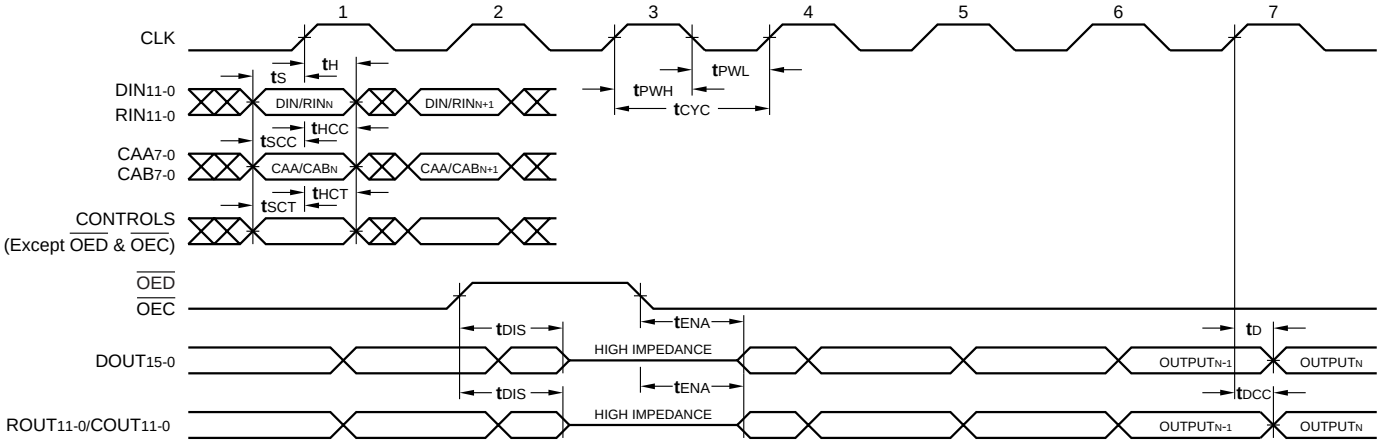
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		5.5	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			140	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			2	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF3320–							
		25*		18*		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	25		18		15		12	
t_{PWL}	Clock Pulse Width Low	10		8		7		5	
t_{PWH}	Clock Pulse Width High	10		8		7		5	
t_S	Input Setup Time	8		6		5		4	
t_H	Input Hold Time	0		0		0		0	
t_{SCT}	Setup Time Control Inputs	8		6		5		4	
t_{HCT}	Hold Time Control Inputs	0		0		0		0	
t_{SCC}	Setup Time Coefficient Control Inputs	8		6		5		4	
t_{HCC}	Hold Time Coefficient Control Inputs	0		0		0		0	
t_D	Output Delay		13		11		9		7
t_{DCC}	Cascade Output Delay		13		11		9		7.5
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		13		12		10
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		13		12		10

SWITCHING WAVEFORMS: DATA I/O

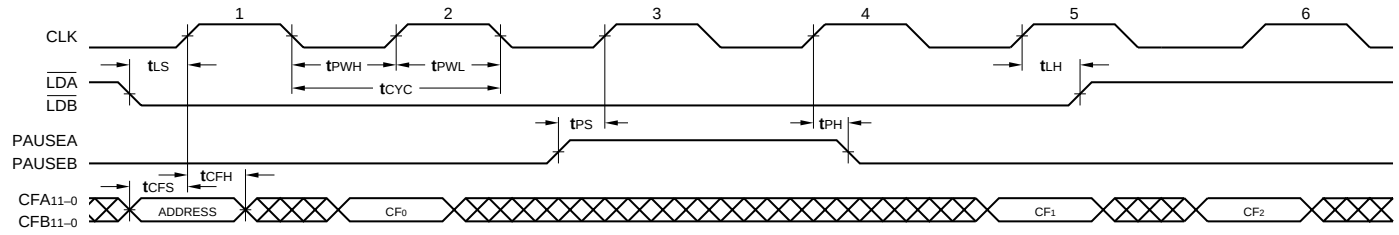


*DISCONTINUED SPEED GRADE

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF3320–							
		25*		18*		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{CFS}	Coefficient Input Setup Time	8		6		6		5.5	
t_{CFH}	Coefficient Input Hold Time	0		0		0		0	
t_{LS}	Load Setup Time	8		7		6		4	
t_{LH}	Load Hold Time	0		0		0		0	
t_{PS}	PAUSE Setup Time	8		6		5		4	
t_{PH}	PAUSE Hold Time	0		0		0		0	

SWITCHING WAVEFORMS: LF INTERFACE™



*DISCONTINUED SPEED GRADE

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. The device can withstand indefinite operation with inputs or outputs in the range of –0.5 V to +5.5 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with outputs changing every cycle and no load, at a 40 MHz clock rate.

7. Tested with all inputs within 0.1 V of **V**CC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except **t**DIS test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified **I**OH and **I**OL at an output voltage of **V**OH min and **V**OL max respectively. Alternatively, a diode bridge with upper and lower current sources of **I**OH and **I**OL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on / turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between **V**CC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device **V**CC and the tester common, and device ground and tester common.

b. Ground and **V**CC supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages on a test fixture should be adjusted to compensate for inductive ground and **V**CC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the **t**ENA test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the **t**DIS test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, VTH, is set at 3.0 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

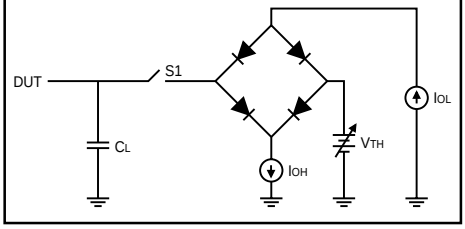
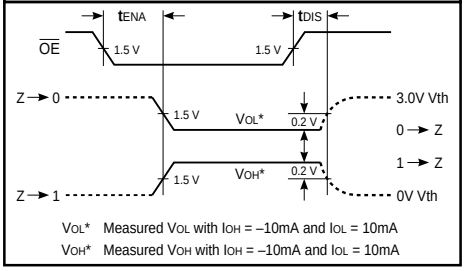
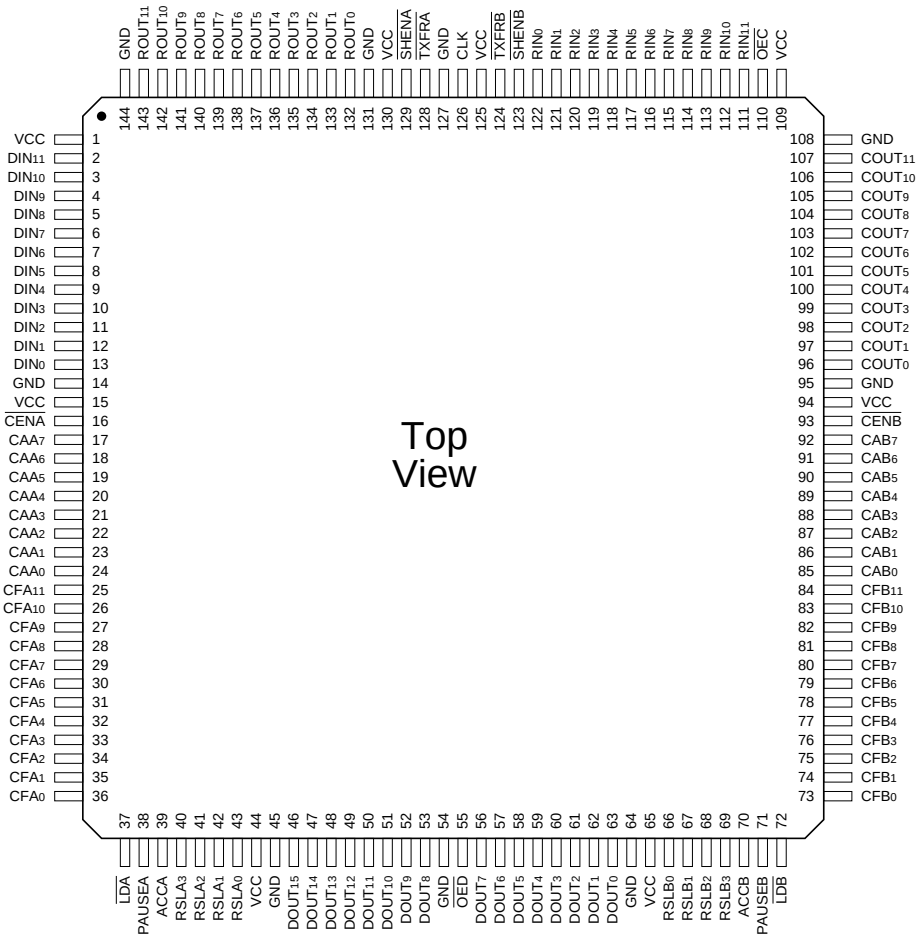


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

144-pin



Speed	Plastic Quad Flatpack (Q5)
	0°C to +70°C — COMMERCIAL SCREENING
15 ns	LF3320QC15
12 ns	LF3320QC12