

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

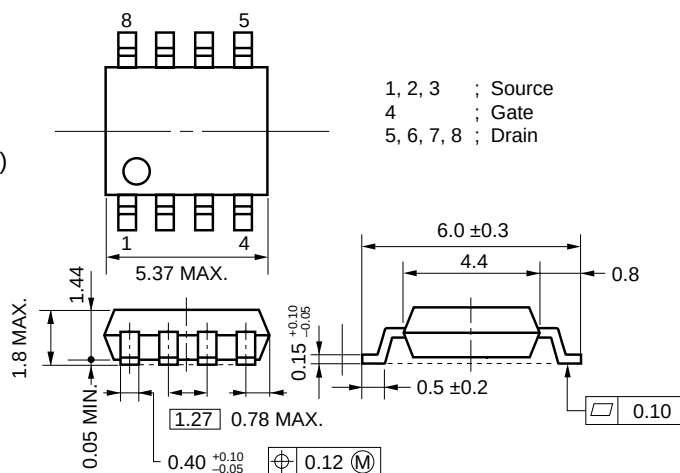
DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for power management applications of notebook computers.

FEATURES

- Super Low On-Resistance
 $R_{DS(on)1} = 10.5 \text{ m}\Omega$ MAX. ($V_{GS} = 10 \text{ V}$, $I_D = 5.0 \text{ A}$)
 $R_{DS(on)2} = 17 \text{ m}\Omega$ MAX. ($V_{GS} = 4 \text{ V}$, $I_D = 5.0 \text{ A}$)
- Low C_{iss} $C_{iss} = 2180 \text{ pF}$ TYP.
- Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

PACKAGE DIMENSIONS (in millimeter)

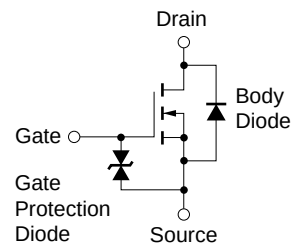


ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, all terminals are connected)

Drain to Source Voltage	V_{DS}	30	V
Gate to Source Voltage	V_{GS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 10	A
Drain Current (pulse) ^{Notes1}	$I_{D(pulse)}$	± 40	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$) ^{Notes2}	P_T	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 0.7 \text{ mm}$

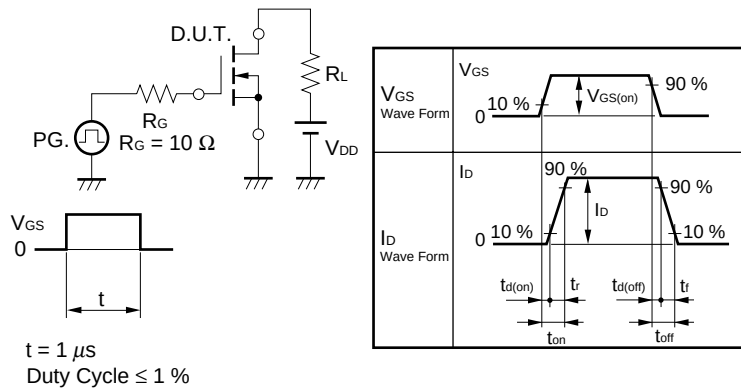


The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if voltage exceeding the rated voltage may be applied to this device.

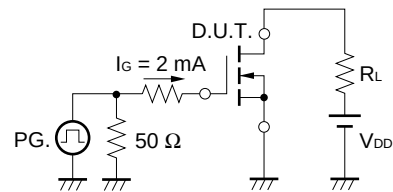
ELECTRICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, all terminals are connected)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	$V_{GS} = 10\text{ V}$, $I_D = 5.0\text{ A}$		8.5	10.5	$\text{m}\Omega$
	$R_{DS(on)2}$	$V_{GS} = 4\text{ V}$, $I_D = 5.0\text{ A}$		12	17	$\text{m}\Omega$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 10\text{ V}$, $I_D = 1\text{ mA}$	1.0	1.6	2.0	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS} = 10\text{ V}$, $I_D = 5.0\text{ A}$	8.0	18		S
Drain Leakage Current	I_{DSS}	$V_{DS} = 30\text{ V}$, $V_{GS} = 0$			10	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0$			± 10	μA
Input Capacitance	C_{iss}	$V_{DS} = 10\text{ V}$		2180		pF
Output Capacitance	C_{oss}	$V_{GS} = 0$		890		pF
Reverse Transfer Capacitance	C_{rss}	$f = 1\text{ MHz}$		370		pF
Turn-On Delay Time	$t_{d(on)}$	$I_D = 5.0\text{ A}$		25		ns
Rise Time	t_r	$V_{GS(on)} = 10\text{ V}$		210		ns
Turn-Off Delay Time	$t_{d(off)}$	$V_{DD} = 15\text{ V}$		120		ns
Fall Time	t_f	$R_G = 10\text{ }\Omega$		75		ns
Total Gate Charge	Q_G	$I_D = 10\text{ A}$		40		nC
Gate to Source Charge	Q_{GS}	$V_{DD} = 24\text{ V}$		5.6		nC
Gate to Drain Charge	Q_{GD}	$V_{GS} = 10\text{ V}$		9.6		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	$I_F = 10\text{ A}$, $V_{GS} = 0$		0.73		V
Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}$, $V_{GS} = 0$		46		ns
Reverse Recovery Charge	Q_{rr}	$di/dt = 100\text{ A}/\mu\text{s}$		45		nC

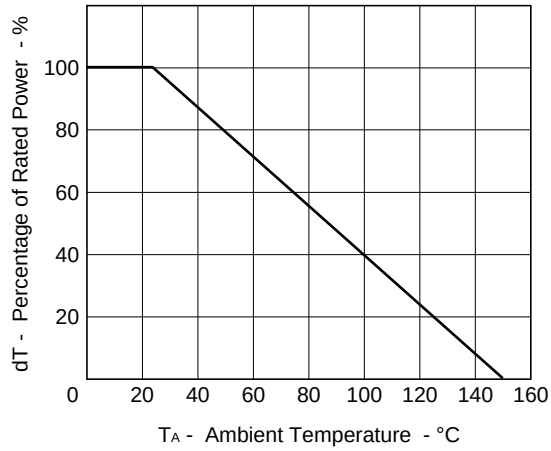
Test Circuit 1 Switching Time



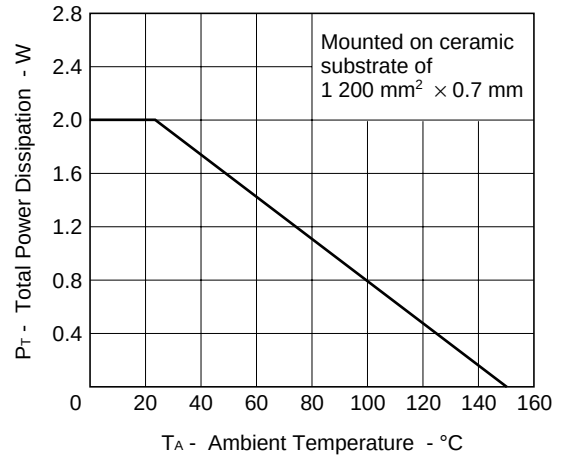
Test Circuit 2 Gate Charge



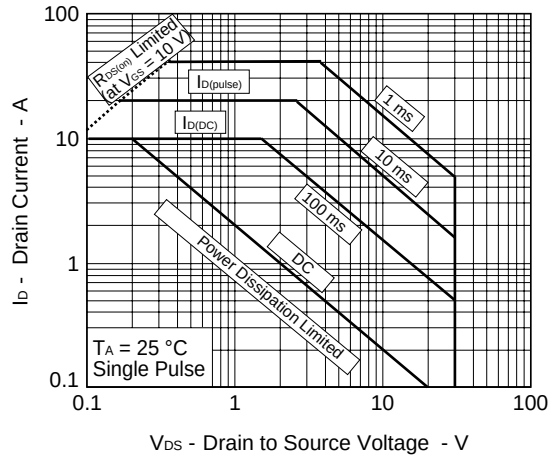
DERATING FACTOR OF FORWARD BIAS
SAFE OPERATING AREA



TOTAL POWER DISSIPATION vs.
AMBIENT TEMPERATURE

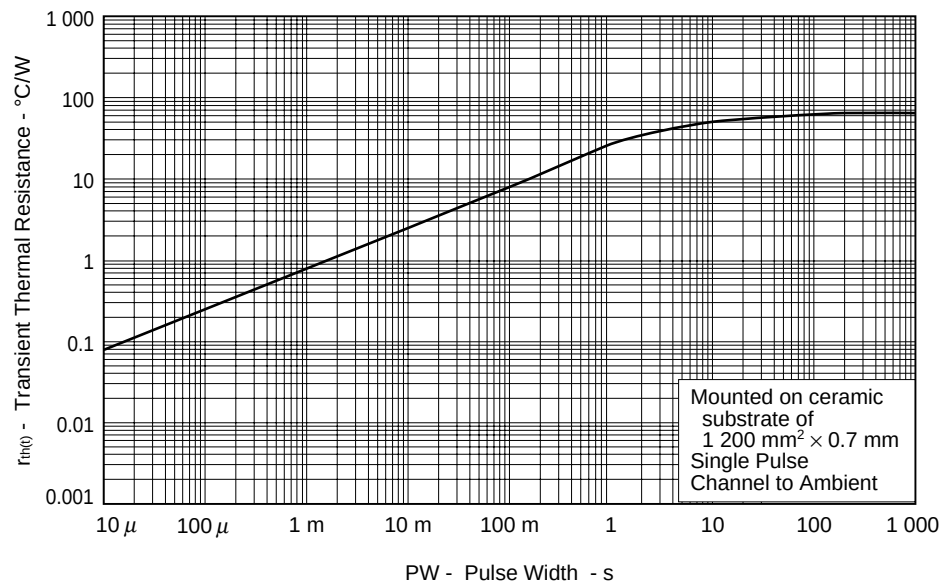


FORWARD BIAS SAFE OPERATING AREA

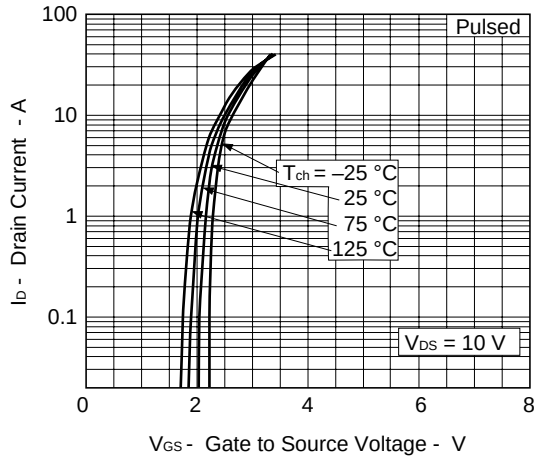


Note:
Mounted on ceramic substrate of 1 200 mm² × 0.7 mm

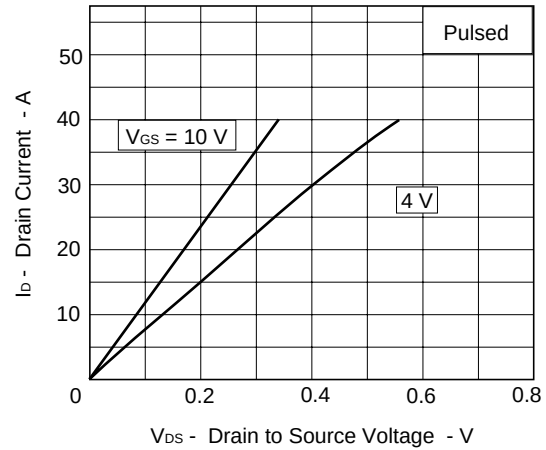
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



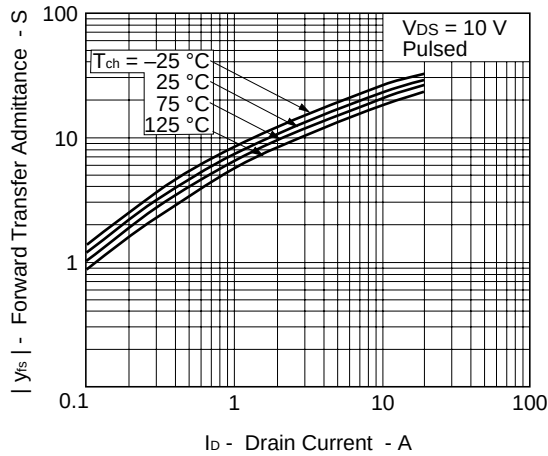
FORWARD TRANSFER CHARACTERISTICS



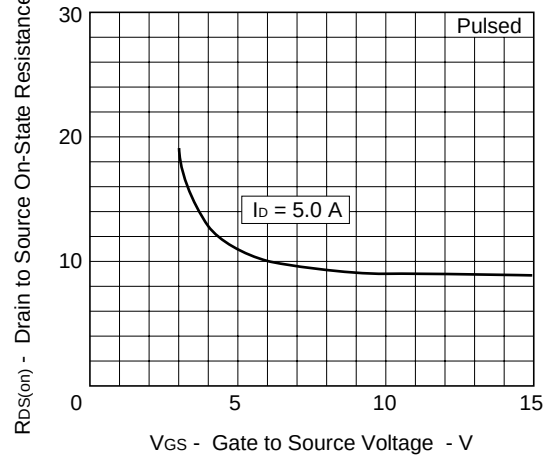
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



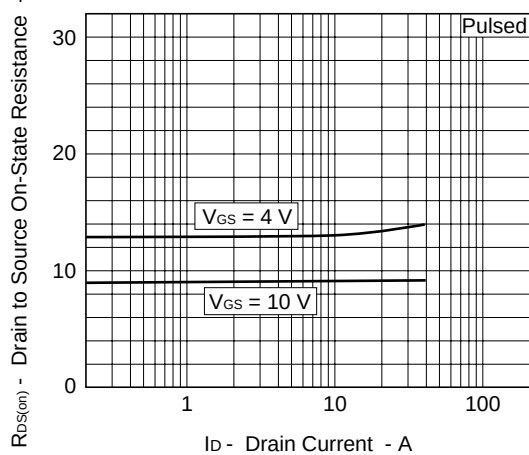
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



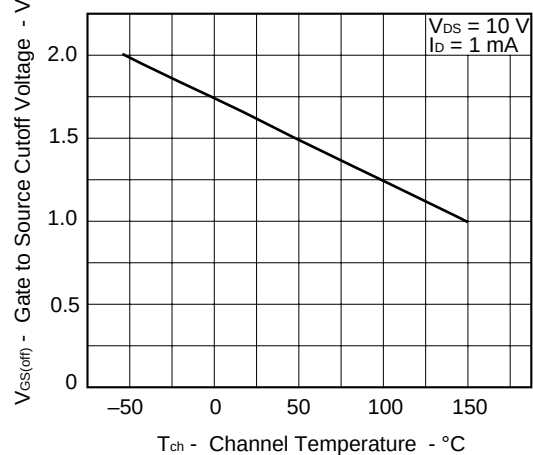
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

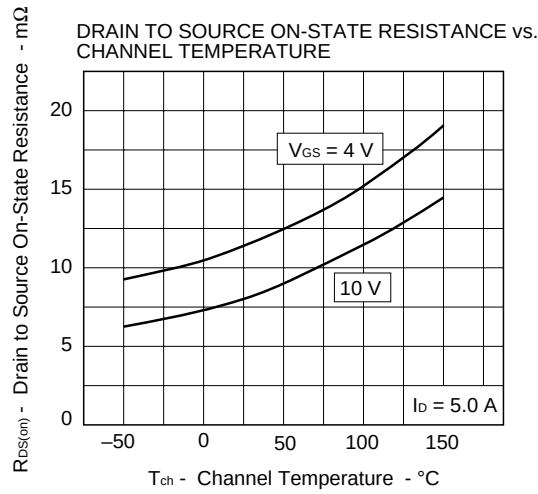
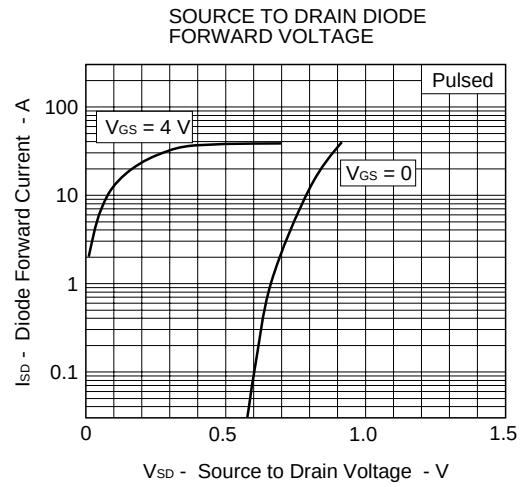
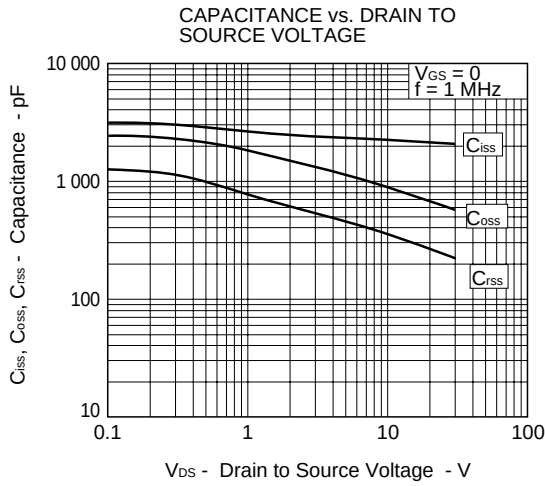
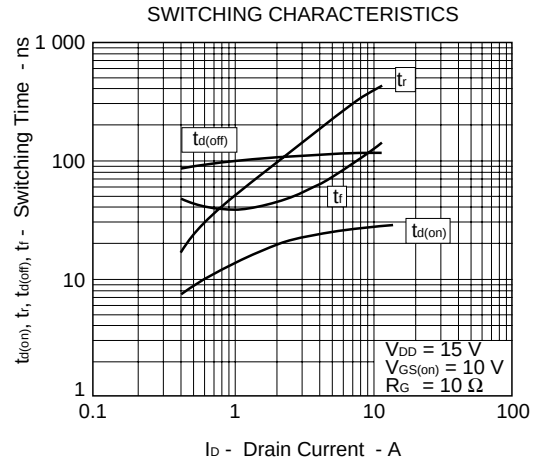
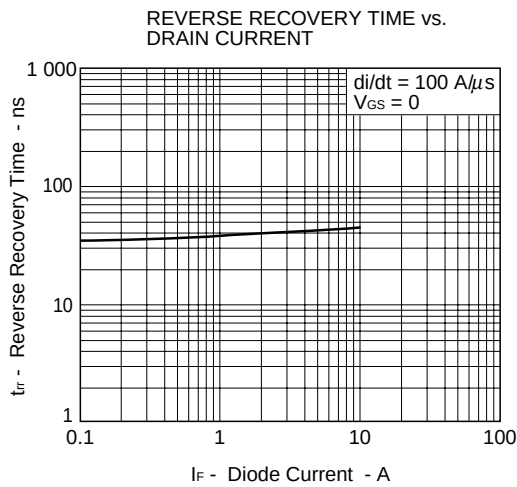
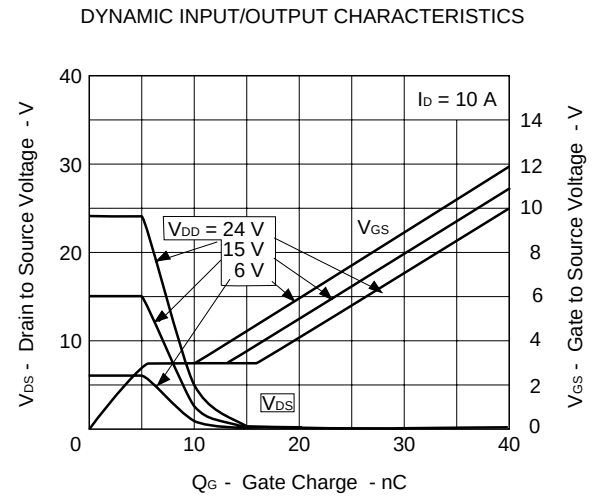


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	C11745E
Quality grade on NEC semiconductor devices	C11531E
Semiconductor device mounting technology manual	C10535E
Semiconductor device package manual	C10943X
Guide to quality assurance for semiconductor devices	MEI-1202
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

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Anti-radioactive design is not implemented in this product.