

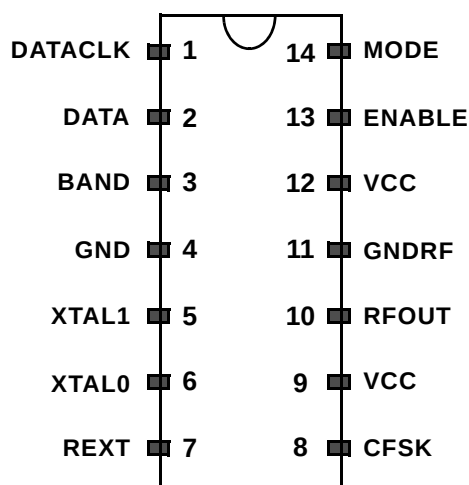
## PLL Tuned UHF Transmitter for Data Transfer Applications

- Selectable frequency bands:  
315—434 MHz and 868—928 MHz
- OOK and FSK modulation
- Adjustable output power range
- Fully integrated voltage control oscillator (VCO)
- Supply voltage range: 1.9—3.6 V
- Very low standby current: 0.1 nA @  $T_A = 25^\circ\text{C}$
- Low-supply voltage shutdown
- Data clock output for microcontroller
- Extended temperature range:  $-40$  to  $125^\circ\text{C}$
- Low external component count
- Typical application compliant with European  
Telecommunications Standards Institute (ETSI)  
standard

## MC33493



### PIN CONNECTIONS



### Ordering Information

| Device     | Ambient Temperature Range                  | Package        |
|------------|--------------------------------------------|----------------|
| MC33493DTB | $-40^\circ\text{C}$ to $125^\circ\text{C}$ | TSSOP14        |
| MC3493DTBE | $-40^\circ\text{C}$ to $125^\circ\text{C}$ | TSSOP14 (ROHS) |

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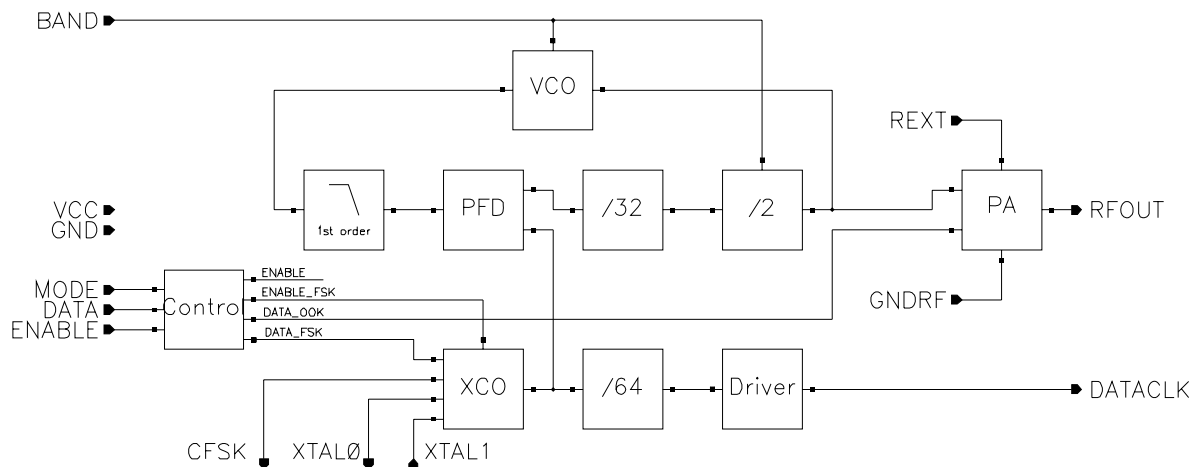


**Figure 1. Simplified Block Diagram**

**Table 1. Pin Function Description**

| Pin | Name    | Description                                  |
|-----|---------|----------------------------------------------|
| 1   | DATACLK | Clock output to the microcontroller          |
| 2   | DATA    | Data input                                   |
| 3   | BAND    | Frequency band selection                     |
| 4   | GND     | Ground                                       |
| 5   | XTAL1   | Reference oscillator input                   |
| 6   | XTAL0   | Reference oscillator output                  |
| 7   | REXT    | Power amplifier output current setting input |
| 8   | CFSK    | FSK switch output                            |
| 9   | VCC     | Power supply                                 |
| 10  | RFOUT   | Power amplifier output                       |
| 11  | GNDRF   | Power amplifier ground                       |
| 12  | VCC     | Power supply                                 |
| 13  | ENABLE  | Enable input                                 |
| 14  | MODE    | Modulation type selection input              |

**Table 2. Absolute Maximum Ratings**

| Parameter                                                    | Symbol   | Value                             | Unit |
|--------------------------------------------------------------|----------|-----------------------------------|------|
| Supply voltage                                               | $V_{CC}$ | $V_{GND} - 0.3$ to $3.7$          | V    |
| Voltage allowed on each pin                                  |          | $V_{GND} - 0.3$ to $V_{CC} + 0.3$ | V    |
| ESD HBM voltage capability on each pin <sup>1</sup> (note 1) |          | $\pm 2000$                        | V    |
| ESD MM voltage capability on each pin <sup>2</sup> (note 2)  |          | $\pm 150$                         | V    |
| Storage temperature                                          | $T_s$    | $-65$ to $+150$                   | °C   |
| Junction temperature                                         | $T_j$    | $+150$                            | °C   |

<sup>1</sup> Human Body model, AEC-Q100-002 Rev. C.

<sup>2</sup> Machine Model, AEC-Q100-003 Rev. E.

# 1 Transmitter Functional Description

MC33493 is a PLL-tuned low-power UHF transmitter. The different modes of operation are controlled by the microcontroller through several digital input pins. The power supply voltage ranges from 1.9 V to 3.6 V, allowing operation with a single lithium cell.

## 2 Phase Locked Loop and Local Oscillator

The VCO is a completely integrated relaxation oscillator. The phase frequency detector (PFD) and the loop filter are fully integrated. The exact output frequency is equal to:  $f_{RFOUT} = f_{XTAL} \times [\text{PLL divider ratio}]$ . The frequency band of operation is selected through the BAND pin.

Table 3 shows details for each frequency band selection.

**Table 3. Band Selection and Associated Divider Ratios**

| BAND Input Level | Frequency Band (MHz) | PLL Divider Ratio | Crystal Oscillator Frequency (MHz) |
|------------------|----------------------|-------------------|------------------------------------|
| High             | 315                  | 32                | 9.84                               |
|                  | 434                  |                   | 13.56                              |
| Low              | 868                  | 64                |                                    |

An out-of-lock function is performed by monitoring the PFD output voltage. When it exceeds defined limits, the RF output stage is disabled.

## 3 Radio Frequency (RF) Output Stage

The radio frequency (RF) output stage source is a single-ended square-wave switched current. Harmonics are present in the output current drive. Their radiated absolute level depends on the antenna characteristics and output power. Typical application demonstrates compliance to ETSI standard.

A resistor,  $R_{ext}$ , connected to the REXT pin controls the output power allowing a trade-off between radiated power and current consumption.

The output voltage is internally clamped to  $V_{cc} \pm 2 V_{be}$  (typ.  $V_{cc} \pm 1.5 \text{ V}$  @  $T_A=25^\circ\text{C}$ ).

## 4 Modulation

To select the On Off Keying (OOK) modulation, a low-logic level must be applied on the MODE pin. This modulation is performed by switching the RF output stage on or off. The logic level applied on the DATA pin controls the output stage state:

DATA = 0 → output stage off,  
 DATA = 1 → output stage on.

Applying a high-logic level on the MODE pin selects Frequency Shift Keying (FSK) modulation. This modulation is achieved by crystal pulling. An internal switch connected to the CFSK pin enables switching the external crystal load capacitors. Figure 2 shows the possible configurations: serial and parallel.

The logic level applied on pin DATA controls the state of this internal switch:

DATA=0 → switch off,  
 DATA=1 → switch on.

DATA input is internally re-synchronized by the crystal reference signal. The corresponding jitter on the data duty cycle cannot exceed  $\pm 1$  reference period ( $\pm 75 \text{ ns}$  for a 13.56 MHz crystal).

This crystal pulling solution implies that the RF output frequency deviation equals the crystal frequency deviation multiplied by the PLL Divider ratio (see Table 3).

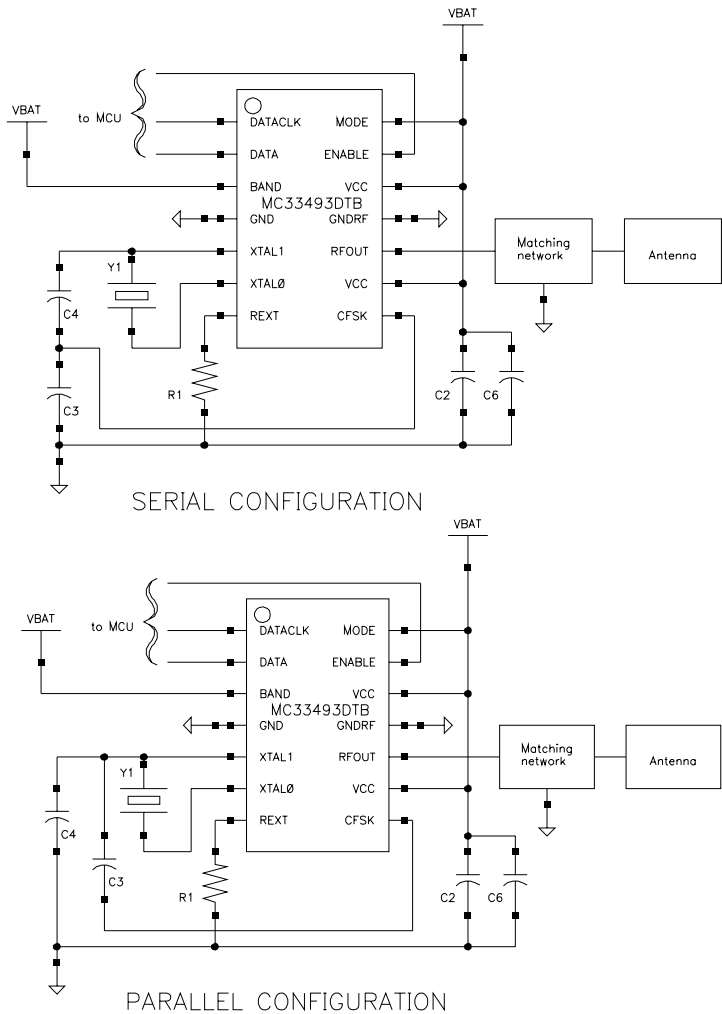


Figure 2. Crystal Pulling Configurations

## 5 Microcontroller Interface

Four digital input pins (ENABLE, DATA, BAND, and MODE) enable the circuit to be controlled by a microcontroller. The band frequency and the modulation type should be configured before enabling the circuit.

One digital output pin, DATACLK, provides the microcontroller with a reference frequency for data clocking. This frequency is equal to the crystal oscillator frequency divided by 64 (see [Table 4](#)).

Table 4. DATACLK Frequency vs Crystal Oscillator Frequency

| Crystal Oscillator Frequency (MHz) | DATACLK Frequency (kHz) |
|------------------------------------|-------------------------|
| 9.84                               | 154                     |
| 13.56                              | 212                     |

## 6 State Machine

Figure 3 details the state machine.

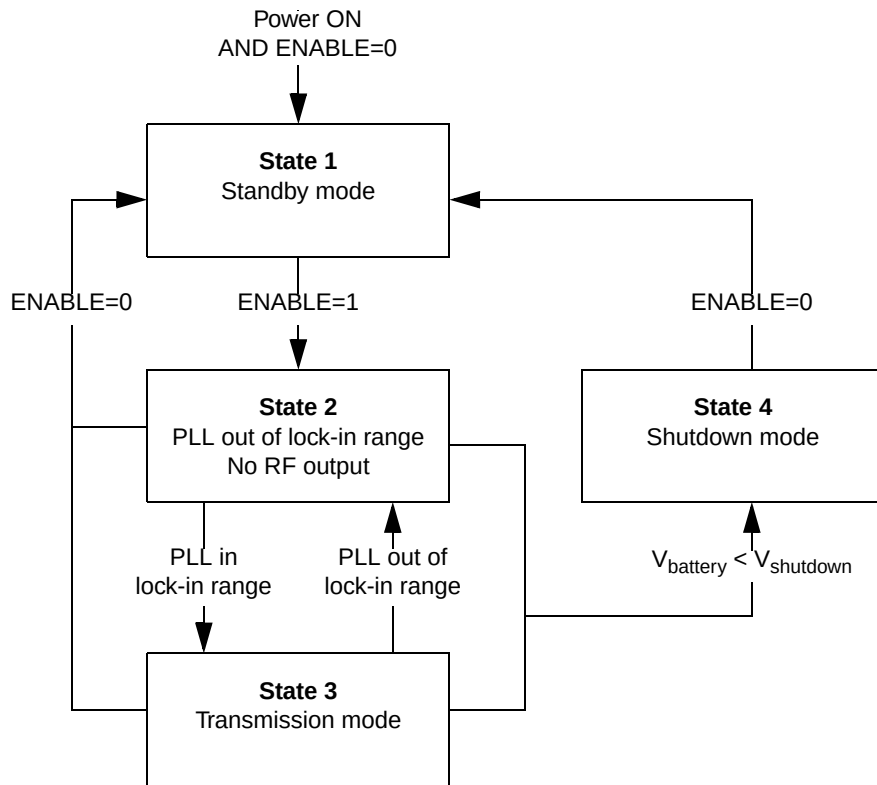


**Figure 3. State machine**

State 1: The circuit is in standby mode and draws only a leakage current from the power supply.

State 2: In this state, the PLL is out of the lock-in range; therefore, the RF output stage is switched off, preventing RF transmission. Data clock is available on the DATACLK pin. Each time the device is enabled, the state machine passes through this state.

State 3: In this state, the PLL is within the lock-in range. If  $t < t_{\text{PLL\_lock\_in}}$ , the PLL may be in acquisition mode. If  $t \geq t_{\text{PLL\_lock\_in}}$ , then the PLL is locked. Data entered on the DATA pin are output on the RFOUT pin according to the modulation selected by the level applied on the MODE pin.

State 4: When the supply voltage falls below the shutdown voltage threshold ( $V_{\text{SDWN}}$ ), the entire circuit switches off. After this shutdown, applying a low level on the ENABLE pin unlatches the circuit.

Figure 4 shows the waveforms of the main signals for a typical application cycle.

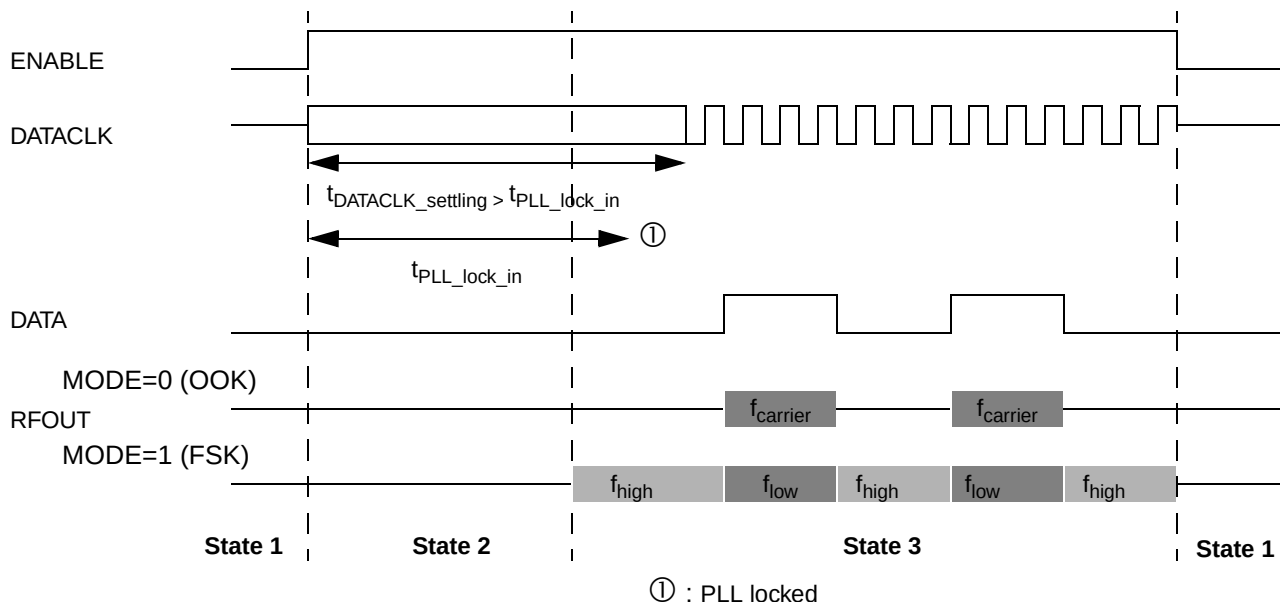


Figure 4. Signals Waveform and Timing Definition

## 7 Power Management

When the battery voltage falls below the shutdown voltage threshold ( $V_{SDWN}$ ) the entire circuit switches off. After this shutdown, the circuit is latched until a low level is applied on pin ENABLE (see State 4 of the state machine).

## 8 Data Clock

At start-up, data clock timing is valid after the data clock settling time. Because the clock is switched off asynchronously, the last period duration cannot be guaranteed.

## 9 Electrical Characteristics

Unless otherwise specified, voltage range  $V_{CC} = [V_{shutdown}; 3.6 \text{ V}]$ , temperature range  $TA = [-40 \text{ }^{\circ}\text{C}; +125 \text{ }^{\circ}\text{C}]$ ,  $R_{ext} = 12 \text{ k}\Omega \pm 5\%$ , RF output frequency  $f_{carrier} = 433.92 \text{ MHz}$ , reference frequency  $f_{reference} = 13.560 \text{ MHz}$ , output load  $RL = 50 \text{ }\Omega \pm 1\%$  (Figure 9). Values refer to the circuit shown in the recommended application schematics: Figure 12 shows OOK modulation and Figure 14 shows FSK modulation. Typical values reflect average measurement at  $V_{CC} = 3 \text{ V}$ ,  $TA = 25 \text{ }^{\circ}\text{C}$ .

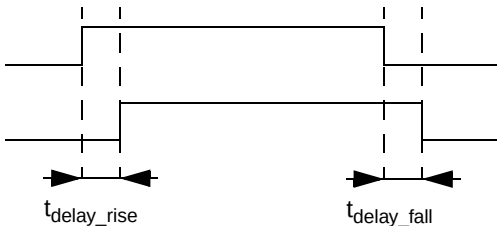
Table 5. Electrical Characteristics

|      | Parameter                                                     | Test Conditions, Comments                                                                                                           | Limits |                |      | Unit           |
|------|---------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|--------|----------------|------|----------------|
|      |                                                               |                                                                                                                                     | Min.   | Typ.           | Max. |                |
| 1    | General Parameters                                            |                                                                                                                                     |        |                |      |                |
| 1.1  | Supply current in standby mode                                | $T_A \leq 25\text{ }^{\circ}\text{C}$                                                                                               | —      | 0.1            | 5    | nA             |
| 1.2  |                                                               | $T_A = 60\text{ }^{\circ}\text{C}$                                                                                                  | —      | 7              | 30   | nA             |
| 1.3  |                                                               | $T_A = 85\text{ }^{\circ}\text{C}$                                                                                                  | —      | 40             | 100  | nA             |
| 1.4  |                                                               | $T_A = 125\text{ }^{\circ}\text{C}$                                                                                                 | —      | 800            | 1700 | nA             |
| 1.5  | Supply current in transmission mode                           | 315 and 434 bands, OOK and FSK modulation, continuous wave, $T_A = 25\text{ }^{\circ}\text{C}$                                      | —      | 11.6           | 13.5 | mA             |
| 1.6  |                                                               | 315 and 434 bands, DATA=0, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$                                  | —      | 4.4            | 6.0  | mA             |
| 1.7  |                                                               | 868 MHz band, DATA=0, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$                                       | —      | 4.6            | 6.2  | mA             |
| 1.8  |                                                               | 315 and 434 bands, OOK and FSK modulation, continuous wave, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$ | —      | 11.6           | 14.9 | mA             |
| 1.9  |                                                               | 868 MHz band, OOK and FSK modulation, continuous wave, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$      | —      | 11.8           | 15.1 | mA             |
| 1.10 | Supply voltage                                                |                                                                                                                                     | —      | 3              | 3.6  | V              |
| 1.11 | Shutdown voltage threshold                                    | $T_A = -40\text{ }^{\circ}\text{C}$                                                                                                 | —      | 2.04           | 2.11 | V              |
| 1.12 |                                                               | $T_A = -20\text{ }^{\circ}\text{C}$                                                                                                 | —      | 1.99           | 2.06 | V              |
| 1.13 |                                                               | $T_A = 25\text{ }^{\circ}\text{C}$                                                                                                  | —      | 1.86           | 1.95 | V              |
| 1.14 |                                                               | $T_A = 60\text{ }^{\circ}\text{C}$                                                                                                  | —      | 1.76           | 1.84 | V              |
| 1.15 |                                                               | $T_A = 85\text{ }^{\circ}\text{C}$                                                                                                  | —      | 1.68           | 1.78 | V              |
| 1.16 |                                                               | $T_A = 125\text{ }^{\circ}\text{C}$                                                                                                 | —      | 1.56           | 1.67 | V              |
| 2    | RF Parameters                                                 |                                                                                                                                     |        |                |      |                |
| 2.1  | R <sub>ext</sub> value                                        |                                                                                                                                     | 12     | —              | 21   | kΩ             |
| 2.2  | Output power                                                  | 315 and 434 MHz bands, with 50 Ω matching network                                                                                   | —      | 5              | —    | dBm            |
| 2.3  |                                                               | 868 MHz band, with 50 Ω matching network                                                                                            | —      | 1              | —    | dBm            |
| 2.4  |                                                               | 315 and 434 MHz bands, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$                                      | -3     | 0              | 3    | dBm            |
| 2.8  |                                                               | 868 MHz band, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$                                               | -7     | -3             | 0    | dBm            |
| 2.12 | Current and output power variation vs. R <sub>ext</sub> value | 315 and 434 MHz bands, with 50 Ω matching network                                                                                   | —      | -0.35<br>-0.25 | —    | dB/kΩ<br>mA/kΩ |

Table 5. Electrical Characteristics (continued)

|      | Parameter                                                         | Test Conditions, Comments                                                                       | Limits |      |      | Unit          |
|------|-------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|--------|------|------|---------------|
|      |                                                                   |                                                                                                 | Min.   | Typ. | Max. |               |
| 2.13 | Harmonic 2 level                                                  | 315 and 434 MHz bands, with 50 $\Omega$ matching network                                        | —      | –34  | —    | dBc           |
| 2.14 |                                                                   | 868 MHz band, with 50 $\Omega$ matching network                                                 | —      | –49  | —    | dBc           |
| 2.15 |                                                                   | 315 and 434 MHz bands                                                                           | —      | –23  | –17  | dBc           |
| 2.16 |                                                                   | 868 MHz band                                                                                    | —      | –38  | –27  | dBc           |
| 2.17 | Harmonic 3 level                                                  | 315 and 434 MHz bands, with 50 $\Omega$ matching network                                        | —      | –32  | —    | dBc           |
| 2.18 |                                                                   | 868 MHz band, with 50 $\Omega$ matching network                                                 | —      | –57  | —    | dBc           |
| 2.19 |                                                                   | 315 and 434 MHz bands                                                                           | —      | –21  | –15  | dBc           |
| 2.20 |                                                                   | 868 MHz band                                                                                    | —      | –48  | –39  | dBc           |
| 2.21 | Spurious level<br>@ $f_{\text{carrier}} \pm f_{\text{DATA CLK}}$  | 315 and 434 MHz bands                                                                           | —      | –36  | –24  | dBc           |
| 2.22 |                                                                   | 868 MHz band                                                                                    | —      | –29  | –17  | dBc           |
| 2.23 | Spurious level<br>@ $f_{\text{carrier}} \pm f_{\text{reference}}$ | 315 MHz band                                                                                    | —      | –37  | –30  | dBc           |
| 2.24 |                                                                   | 434 MHz band                                                                                    | —      | –44  | –34  | dBc           |
| 2.25 |                                                                   | 868 MHz band                                                                                    | —      | –37  | –27  | dBc           |
| 2.41 | Spurious level<br>@ $f_{\text{carrier}}/2$                        | 315 MHz band                                                                                    | —      | –62  | –53  | dBc           |
| 2.26 |                                                                   | 434 MHz band                                                                                    | —      | –80  | –60  | dBc           |
| 2.27 |                                                                   | 868 MHz band                                                                                    | —      | –45  | –39  | dBc           |
| 2.30 | Phase noise                                                       | 315 and 434 MHz bands, $\pm 175$ kHz from $f_{\text{carrier}}$                                  | —      | –75  | –68  | dBc/Hz        |
| 2.31 |                                                                   | 868 MHz band, $\pm 175$ kHz from $f_{\text{carrier}}$                                           | —      | –73  | –66  | dBc/Hz        |
| 2.32 | PLL lock-in time,<br>$t_{\text{PLL\_lock\_in}}$                   | $f_{\text{carrier}}$ within 30 kHz from the final value, crystal series resistor = 150 $\Omega$ | —      | 400  | 1600 | $\mu\text{s}$ |
| 2.33 | XTAL1 input capacitance                                           |                                                                                                 | —      | 1    | —    | pF            |
| 2.34 | Crystal resistance                                                | OOK modulation                                                                                  | —      | 20   | 200  | W             |
| 2.44 |                                                                   | FSK modulation                                                                                  |        | 20   | 50   |               |
| 2.35 | OOK modulation depth                                              |                                                                                                 | 75     | 90   | —    | dBc           |
| 2.36 | FSK modulation<br>carrier frequency<br>total deviation            | 315 and 434 MHz bands, see note Note:                                                           | —      | —    | 100  | kHz           |
| 2.37 |                                                                   | 868 MHz band, see note Note:                                                                    | —      | —    | 200  | kHz           |
| 2.38 | CFSK output resistance                                            | MODE = 0, DATA = x<br>MODE = 1, DATA = 0                                                        | 50     | 70   | —    | k $\Omega$    |
| 2.39 |                                                                   | MODE = 1, DATA = 1                                                                              | —      | 90   | 300  | W             |
| 2.43 | CFSK output capacitance                                           |                                                                                                 | —      | 1    | —    | pF            |
| 2.40 | Data rate                                                         | Manchester coding                                                                               | —      | —    | 10   | kbit/s        |

Table 5. Electrical Characteristics (continued)

|                                                                                                                                                                                                                                                                                                                                            | Parameter                                                                                    | Test Conditions, Comments                                                        | Limits                      |      |                             | Unit          |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------|-----------------------------|------|-----------------------------|---------------|
|                                                                                                                                                                                                                                                                                                                                            |                                                                                              |                                                                                  | Min.                        | Typ. | Max.                        |               |
| 2.41                                                                                                                                                                                                                                                                                                                                       | Data to RF delay difference between falling and rising edges, $t_{\text{delay\_difference}}$ | MODE = 0, see note                                                               | 3.5                         | 5.25 | 7.5                         | $\mu\text{s}$ |
| 2.42                                                                                                                                                                                                                                                                                                                                       |                                                                                              | MODE = 1, see note                                                               | −200                        | —    | 200                         | ns            |
| <b>Note:</b> This parameter is depending on crystal characteristics, load capacitor values (see <a href="#">Table 4</a> ) and PCB track capacitance.                                                                                                                                                                                       |                                                                                              |                                                                                  |                             |      |                             |               |
| <b>Note:</b> Delay difference definition                                                                                                                                                                                                                                                                                                   |                                                                                              |                                                                                  |                             |      |                             |               |
| <div><div><div>Input data</div><div>Demodulated data</div></div><div>From 50% of data edge to corresponding demodulated signal envelope edge:<br/><math>t_{\text{delay\_difference}} = t_{\text{delay\_fall}} - t_{\text{delay\_rise}}</math></div></div> |                                                                                              |                                                                                  |                             |      |                             |               |
| <b>3</b>                                                                                                                                                                                                                                                                                                                                   | <b>Microcontroller Interfaces</b>                                                            |                                                                                  |                             |      |                             |               |
| 3.1                                                                                                                                                                                                                                                                                                                                        | Input low voltage                                                                            | Pins: BAND, MODE, ENABLE, and DATA                                               | 0                           | —    | $0.3 \times V_{\text{CC}}$  | V             |
| 3.2                                                                                                                                                                                                                                                                                                                                        | Input high voltage                                                                           |                                                                                  | $0.7 \times V_{\text{CC}}$  | —    | $V_{\text{CC}}$             | V             |
| 3.3                                                                                                                                                                                                                                                                                                                                        | Input hysteresis voltage                                                                     |                                                                                  | —                           | —    | 120                         | mV            |
| 3.4                                                                                                                                                                                                                                                                                                                                        | Input current                                                                                | Pins: BAND, MODE, DATA = 1                                                       | —                           | —    | 100                         | nA            |
| 3.5                                                                                                                                                                                                                                                                                                                                        | ENABLE pulldown resistor                                                                     |                                                                                  | —                           | 180  | —                           | k $\Omega$    |
| 3.6                                                                                                                                                                                                                                                                                                                                        | DATACLK output low voltage                                                                   | $C_{\text{load}} = 2 \text{ pF}$                                                 | 0                           | —    | $0.25 \times V_{\text{CC}}$ | V             |
| 3.7                                                                                                                                                                                                                                                                                                                                        | DATACLK output high voltage                                                                  |                                                                                  | $0.75 \times V_{\text{CC}}$ | —    | $V_{\text{CC}}$             | V             |
| 3.8                                                                                                                                                                                                                                                                                                                                        | DATACLK rising time                                                                          | $C_{\text{load}} = 2 \text{ pF}$ , measured from 20% to 80% of the voltage swing | —                           | 250  | 500                         | ns            |
| 3.9                                                                                                                                                                                                                                                                                                                                        | DATACLK falling time                                                                         |                                                                                  | —                           | 150  | 400                         | ns            |
| 3.10                                                                                                                                                                                                                                                                                                                                       | DATACLK settling time, $t_{\text{DATACLK\_settling}}$                                        | $45\% < \text{duty cycle } f_{\text{DATACLK}} < 55\%$                            | —                           | 800  | 2000                        | $\mu\text{s}$ |

## 10 RF Output Spectrum

The following figures represent spectrums of the transmitter carrier, measured in conduction mode. Three different spans have been used. The 5 MHz span spectrum (Figure 5) shows phase noise response close to the RF carrier and the noise suppression within the PLL-loop bandwidth. The 50 MHz span spectrum (Figure 6) shows phase noise and reference spurious. Finally, the 1.5 GHz span spectrum (Figure 7) shows the second and third harmonics of carrier. All spectrums are measured in OOK modulation at DATA=1.

Figure 8 shows the spectrum in case of FSK modulation with 45 kHz deviation at 4 kbit/s data rate.

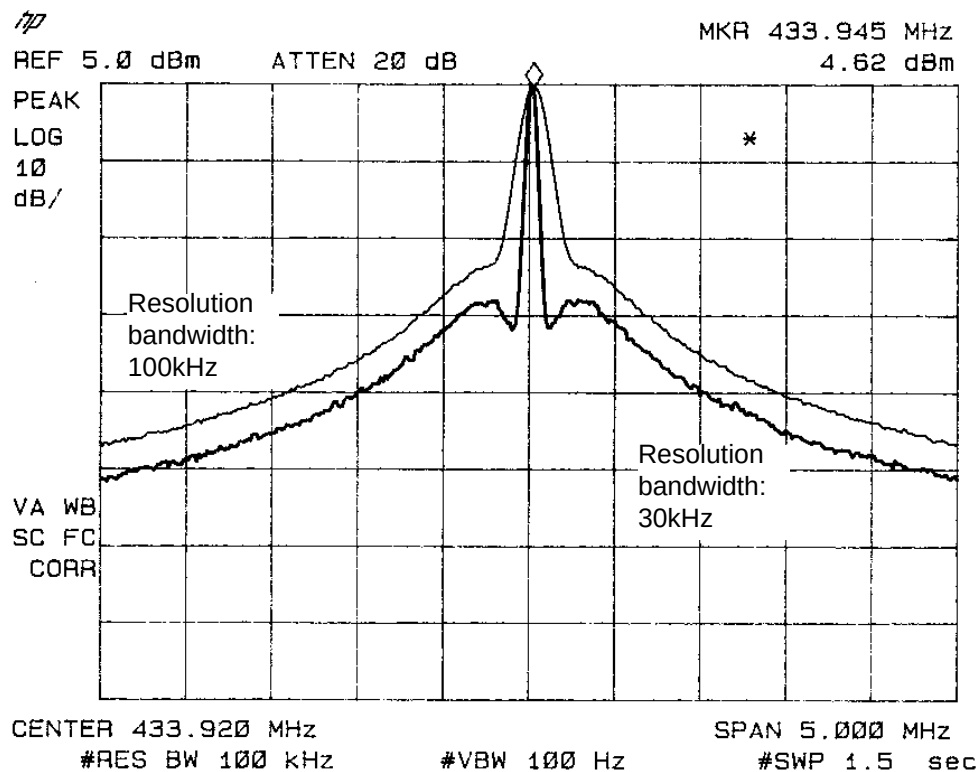


Figure 5. RF Spectrum at 434 MHz Frequency Band Displayed with a 5 MHz Span

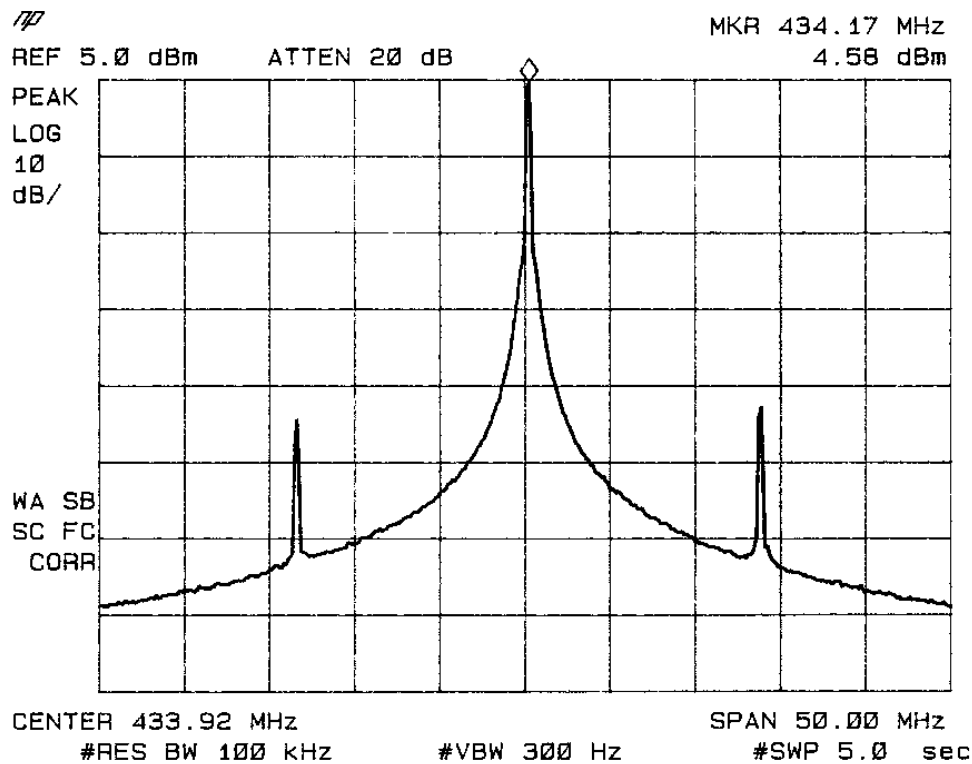


Figure 6. RF Spectrum at 434 MHz Frequency Band Displayed with a 50 MHz Span

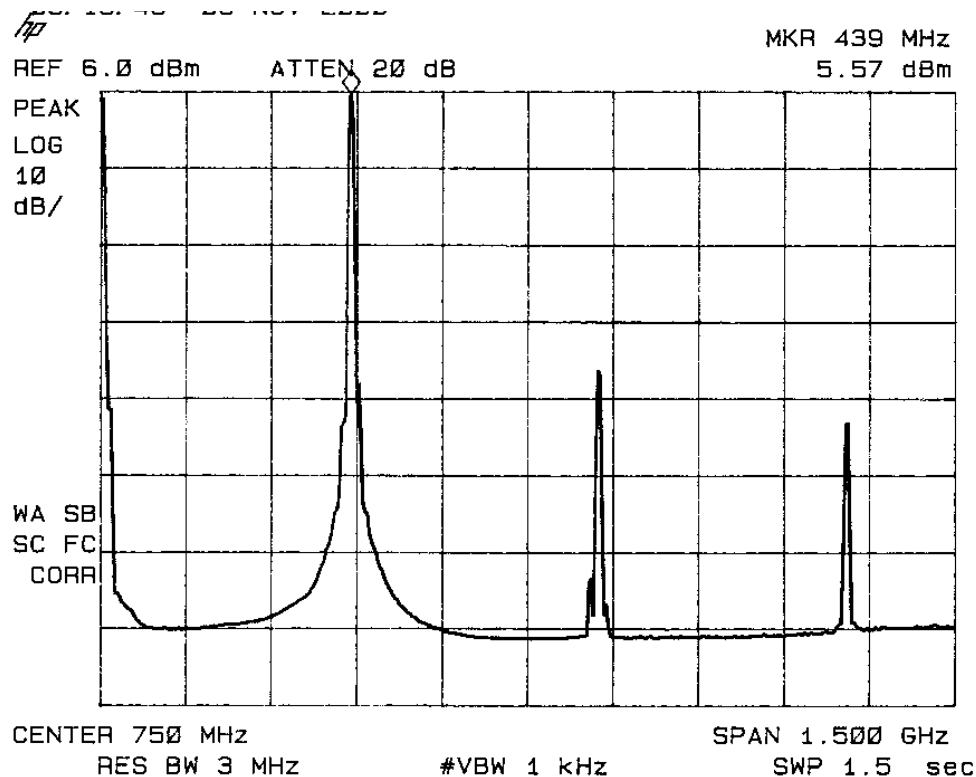


Figure 7. RF Spectrum at 434 MHz Frequency Band Displayed with a 1.5 GHz Span

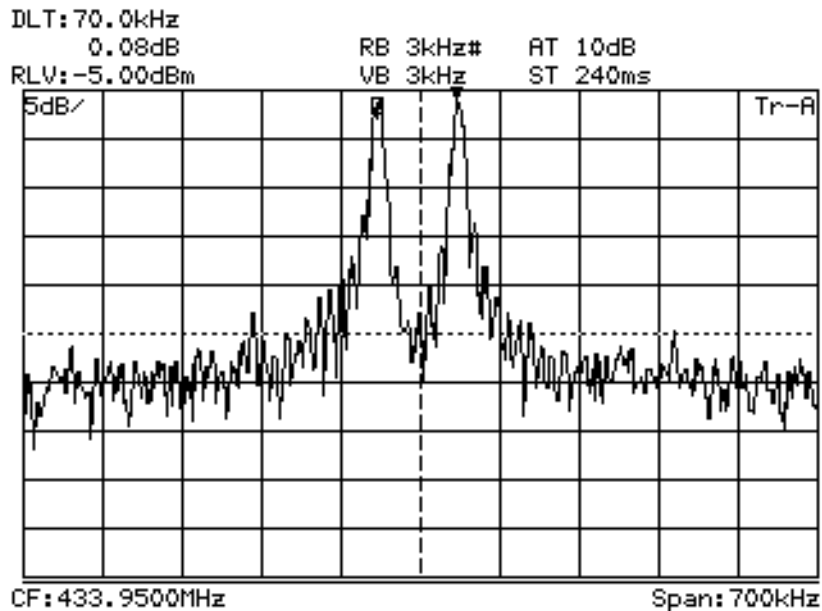


Figure 8. RF Spectrum at 434 MHz Band for a 70 kHz FSK Deviation at 4.8 kbit/s

# 11 Output Power Measurement

The RF output levels given in [Section 9, “Electrical Characteristics,”](#) are measured with a  $50\ \Omega$  load directly connected to the RFOUT pin, as shown below in [Figure 9](#). This wideband coupling method gives results independent of the application.

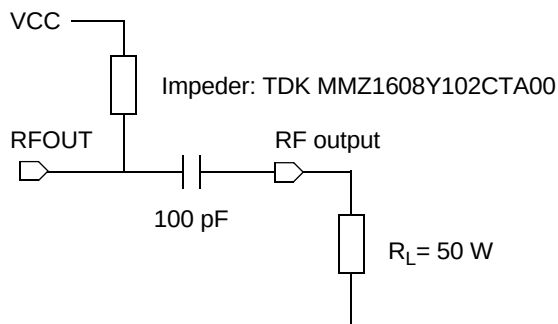


**Figure 9. Output Power Measurement Configurations**

The configuration shown in [Figure 10\(a\)](#) provides better efficiency in terms of output power and harmonics rejection. The schematic on [Figure 10\(b\)](#) gives the equivalent circuit of the RFOUT pin and the DC bias impeder as well as matching network components for 434 MHz frequency band.

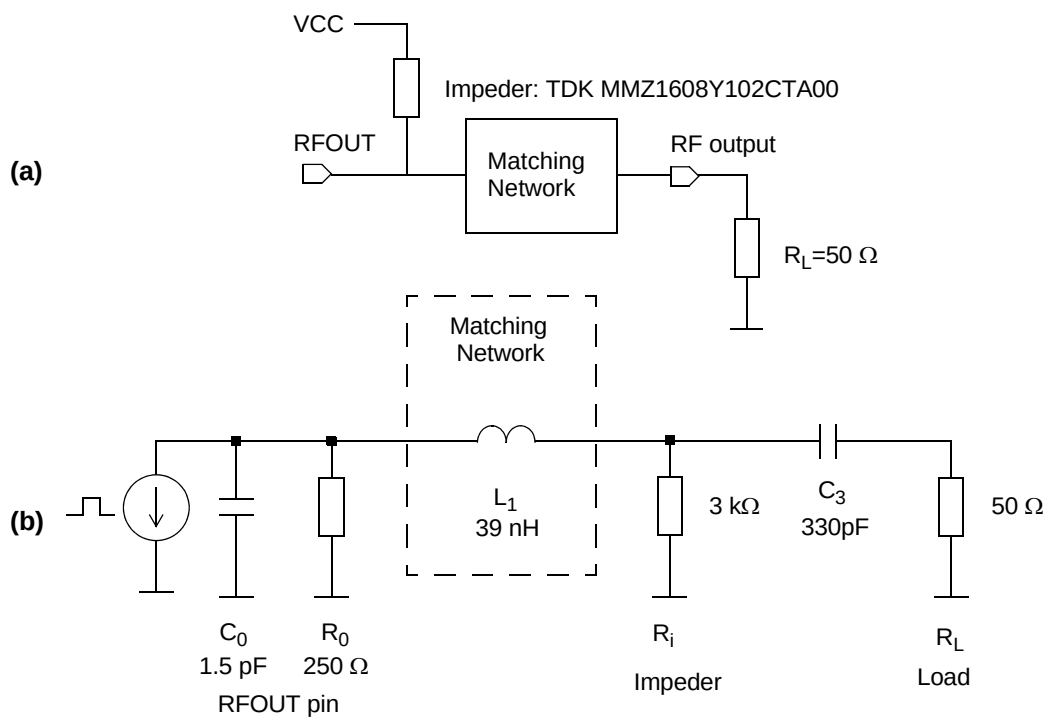


**Figure 10. Output Model and Matching Network for 434 MHz Band**

Figure 11 shows the output power versus the  $R_{ext}$  resistor value with 50  $\Omega$  load and with matching network.

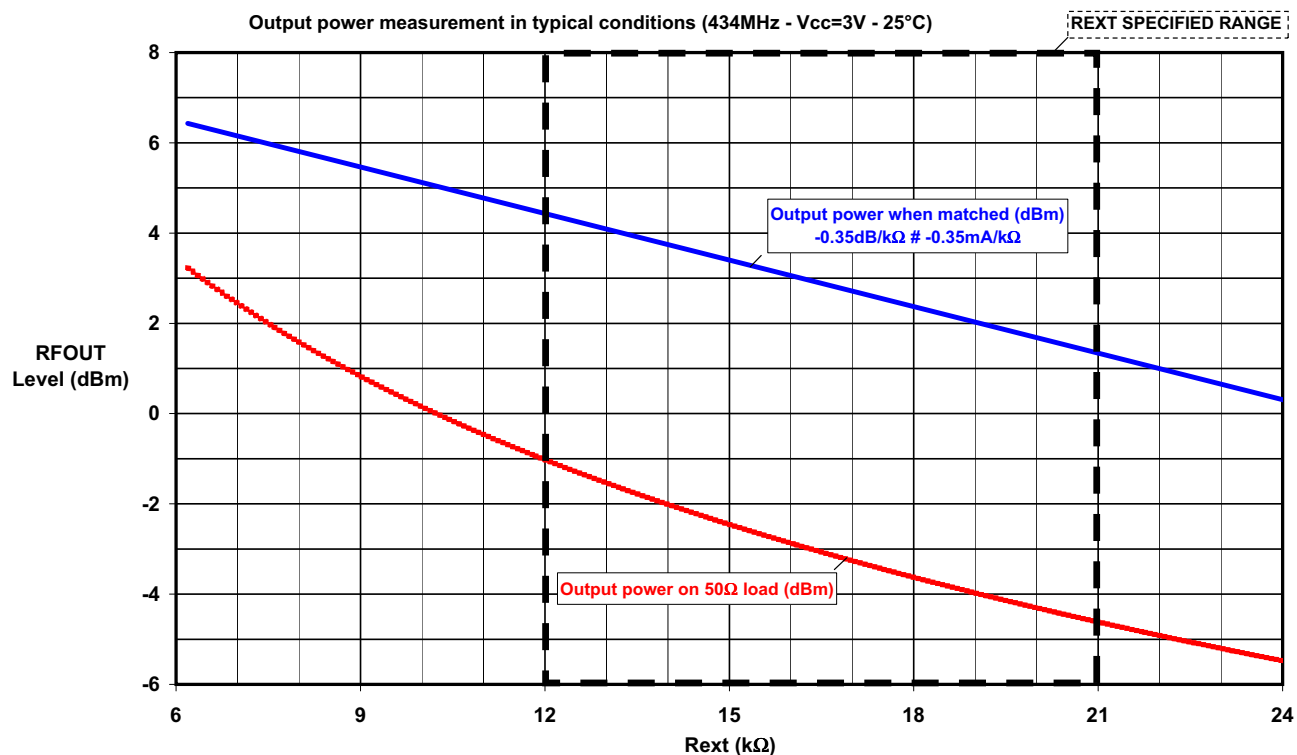


Figure 11. Output Power at 434 MHz Band vs  $R_{ext}$  Value

The 50  $\Omega$  matching network used for the 868 MHz band is similar to the 434 MHz, excepting components values: L1 is changed to 8.2 nH and C3 to 470 pF in Figure 11. The typical gain of this 868 MHz matching network is 4 dB compared to unmatched configuration.

## 12 Complete Application Schematic and PCB for OOK Modulation

Figure 12 shows a complete application schematic using a MC68HC908RK2 microcontroller. OOK modulation is selected,  $f_{carrier} = 433.92$  MHz. The  $C_2$  to  $C_5$  capacitors can be removed if switch debounce is done by software.

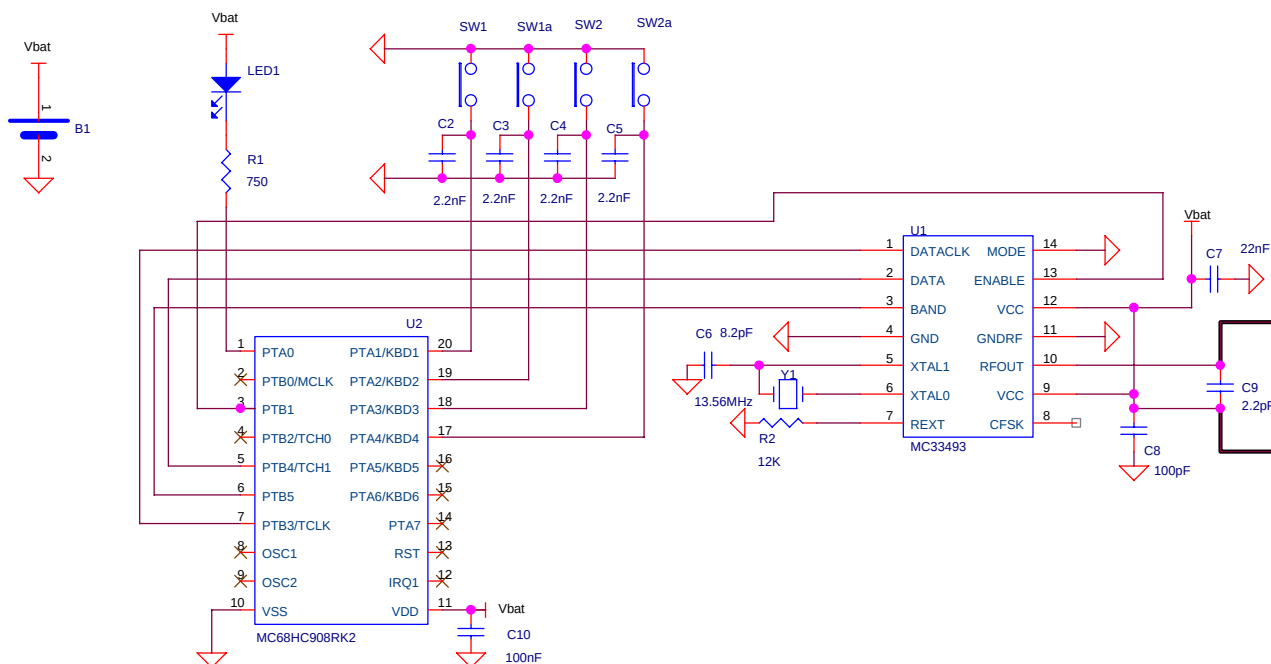


**Figure 12. Application Schematic for OOK Modulation, 434 MHz Frequency Band**

For 868 MHz band application, the input pin BAND must be wired to ground. See component description on [Table 6](#) and [Table 7](#).

Table 6. External Components Description for OOK

| Component | Function                                                | Value               | Unit |
|-----------|---------------------------------------------------------|---------------------|------|
| Y1        | Crystal,<br>see <a href="#">Table 7</a>                 | 315 MHz band: 9.84  | MHz  |
|           |                                                         | 434 MHz band: 13.56 | MHz  |
|           |                                                         | 868 MHz band: 13.56 | MHz  |
| R2        | RF output level setting<br>resistor (R <sub>ext</sub> ) | 12                  | kΩ   |
| C6        | Crystal load capacitor                                  | 8.2 <sup>1</sup>    | pF   |
| C7        | Power supply decoupling<br>capacitors                   | 22                  | nF   |
| C8        |                                                         | 100                 | pF   |

<sup>1</sup> C6 value equals recommended crystal load capacitance reduced by the PCB stray capacitances.

Examples of crystal reference are given below (see characteristics in [Table 7](#)) for different application bands:

- at 315 MHz band ( $f_{\text{reference}} = 9.84375 \text{ MHz}$ ,  $-40^\circ\text{C} < T_A < 85^\circ\text{C}$ ): NDK LN-G102-950,
- at 434/868 MHz bands ( $f_{\text{reference}} = 13.56 \text{ MHz}$ ,  $-40^\circ\text{C} < T_A < 125^\circ\text{C}$ ): NDK NX8045GB/CSJ S1-40125-8050-12 and NDK NX1255GA.

Table 7. Typical Crystal Characteristics (SMD Package)

| Parameter            | NDK LN-G102-950<br>(for 315 MHz) | NDK NX8045GB/CSJ<br>S1-40125-8050-12<br>(for 434 MHz and 868 MHz) | NDK NX1255GA<br>(for 434 MHz and 868 MHz) | Unit     |
|----------------------|----------------------------------|-------------------------------------------------------------------|-------------------------------------------|----------|
| Load capacitance     | 12                               | 12                                                                | 12                                        | pF       |
| Motional capacitance | 3.33                             | 4.4                                                               | 10.5                                      | fF       |
| Static capacitance   | 1.05                             | 1.5                                                               | 2.46                                      | pF       |
| Loss resistance      | 28                               | 18.5                                                              | 10                                        | $\Omega$ |

Figure 13 shows a two-button keyfob board. Size is 30 × 45 millimeters.

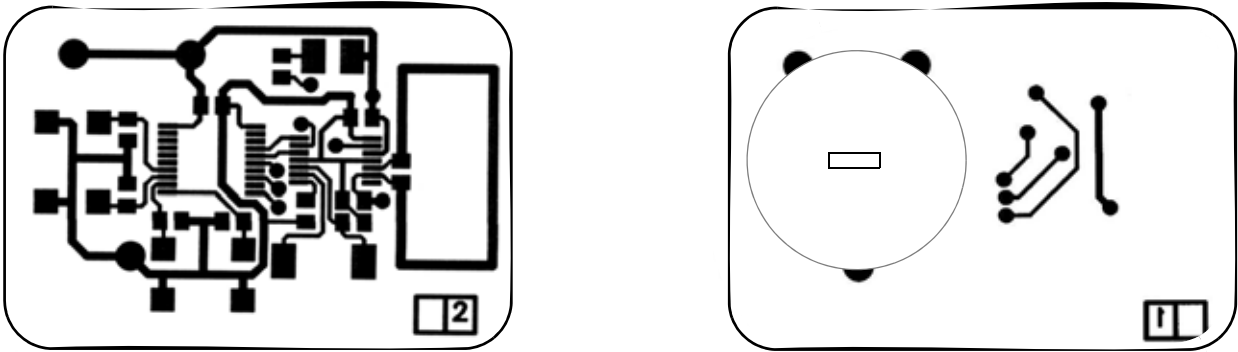


Figure 13. Two-Button Keyfob Board Layout

# 13 Complete Application Schematic and PCB for FSK Modulation

Figure 14 shows a complete application schematic using a MC68HC908RK2 microcontroller. FSK modulation is selected,  $f_{\text{carrier}} = 433.92 \text{ MHz}$ .  $C_1$  capacitor can be removed if switch debounce is done by software.

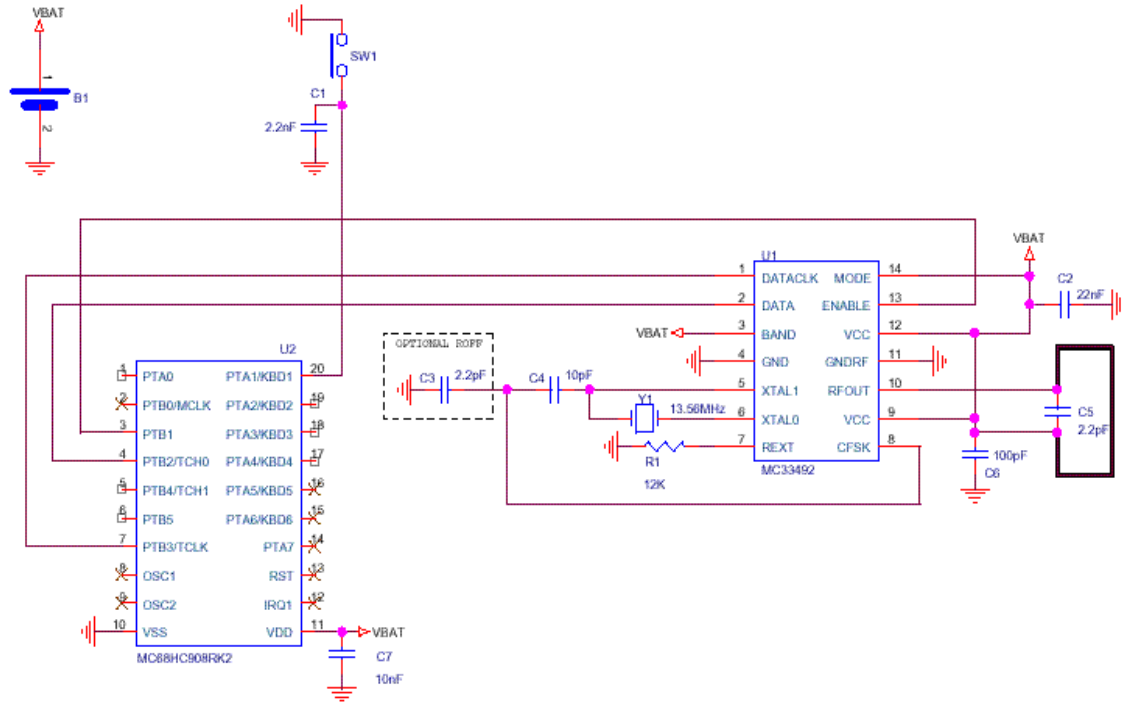


**Figure 14. Application Schematic for FSK Modulation, Serial Configuration, 434 MHz Frequency Band**

For 868 MHz band application, the input pin BAND must be wired to ground. See component description in [Table 8](#).

**Table 8. External Components Description for FSK**

| Component | Function                                          | Value                                               | Unit       |
|-----------|---------------------------------------------------|-----------------------------------------------------|------------|
| Y1        | Crystal                                           | 315 MHz band: 9.84,<br>See <a href="#">Table 7</a>  | MHz        |
|           |                                                   | 434 MHz band: 13.56,<br>see <a href="#">Table 7</a> | MHz        |
|           |                                                   | 868 MHz band: 13.56,<br>see <a href="#">Table 7</a> | MHz        |
| R1        | RF output level setting<br>resistor ( $R_{ext}$ ) | 12                                                  | k $\Omega$ |
| C3        | Crystal load capacitor                            | See <a href="#">Table 9</a>                         | pF         |
| C4        |                                                   |                                                     | pF         |
| C2        | Power supply decoupling capacitor                 | 22                                                  | nF         |
| C6        |                                                   | 100                                                 | pF         |

[Figure 15](#) shows the corresponding PCB layout.

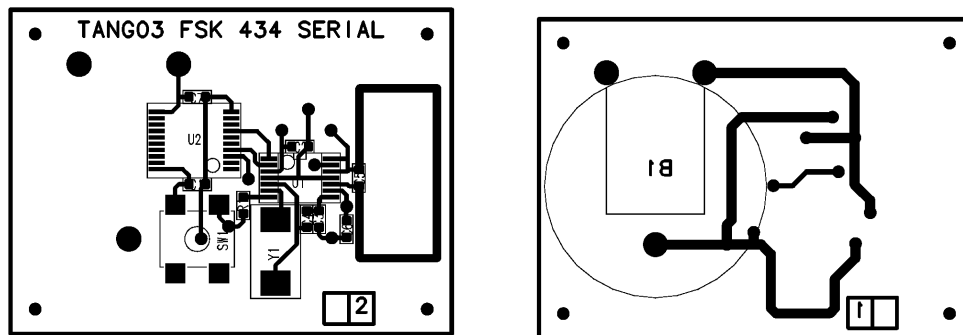


**Figure 15. Application PCB Layout for FSK Modulation, Serial Configuration, 434 MHz Frequency Band**

Table 9 gives the measured FSK deviations respective to C3 and C4 capacitor values for three deviations. Crystal reference is NDK NX8045GB/CSJ S1-40125-8050-12.

**Table 9. Crystal Pulling Capacitor Values vs Carrier Frequency Total Deviation -1-**

| Carrier frequency (MHz) | Carrier frequency total deviation (kHz) | C3 capacitor (pF) | C4 capacitor (pF) | Recommended R_off value (k $\Omega$ ) |
|-------------------------|-----------------------------------------|-------------------|-------------------|---------------------------------------|
| 434                     | 45                                      | 4.7               | 6.8               | 10                                    |
|                         | 70                                      | 2.2               | 10                | —                                     |
|                         | 100                                     | 1                 | 15                | 22                                    |
| 868                     | 90                                      | 4.7               | 6.8               | 10                                    |
|                         | 140                                     | 2.2               | 10                | —                                     |
|                         | 200                                     | 1                 | 15                | 22                                    |

Another crystal reference, NDK NX1255GA (see Table 7), is enabled to reach higher deviation as mentioned on Table 10. These results are due to the higher crystal motional capacitor.

**Table 10. Crystal Pulling Capacitor Values vs Carrier Frequency Total Deviation -2-**

| Carrier frequency (MHz) | Carrier frequency total deviation (kHz) | C3 capacitor value (pF) | C4 capacitor value (pF) | Recommended R_off value (k $\Omega$ ) |
|-------------------------|-----------------------------------------|-------------------------|-------------------------|---------------------------------------|
| 434                     | 150                                     | 1                       | 27                      | —                                     |
| 868                     | 300                                     | 1                       | 27                      | —                                     |

## 14 Recommendations for FSK Modulation

FSK deviation is function of total load capacitance presented to the crystal. This load capacitance is constituted by various contributors:

- the crystal characteristic, especially its static capacitance
- the external load capacitors (C3, C4 as defined in Figure 14 and Table 9)
- the device internal capacitance of pins XTAL0, XTAL1, CFSK
- the PCB track capacitance

The schematic given in Figure 16 shows a typical FSK application using serial capacitor configuration, where device pads and PCB track capacitances are mentioned.

Device pad capacitance is defined by the package capacitance and by the internal circuitry. Typical capacitance values for these pads are given in [Table 11](#).

Some realistic assumptions and measurements have been made concerning track parasitic capacitances for a 0.8 mm FR4 double side application PCB. They are given in [Table 11](#) and the corresponding PCB layout is shown in [Figure 17](#).

To achieve large deviations, this total load capacitance must be lowered. For a given crystal, the PCB must be carefully laid out to reduce the capacitance of the tracks wired to XTAL0, XTAL1, and CFSK pins.

**Recommendation:** a R<sub>off</sub> resistor can be added in parallel with the FSK switch to optimize the transient response of demodulated signal. [Table 11](#) gives the optimized R<sub>off</sub> values for two deviations. There is no footprint for R<sub>off</sub> resistor on the layout in [Figure 16](#). When used, this component can be soldered on top of C3.

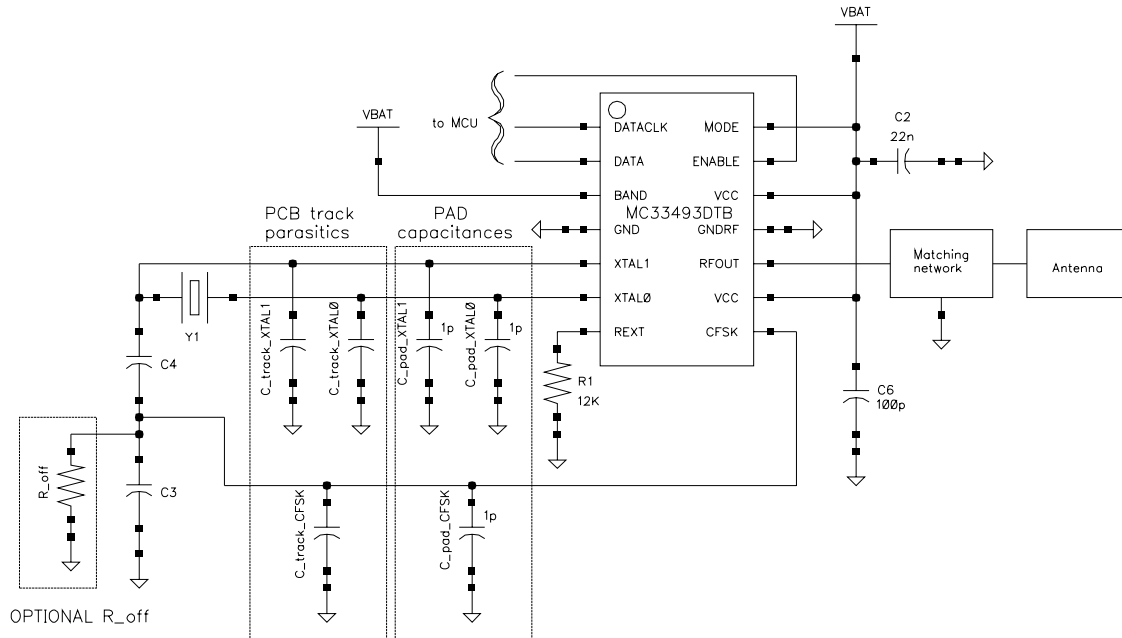
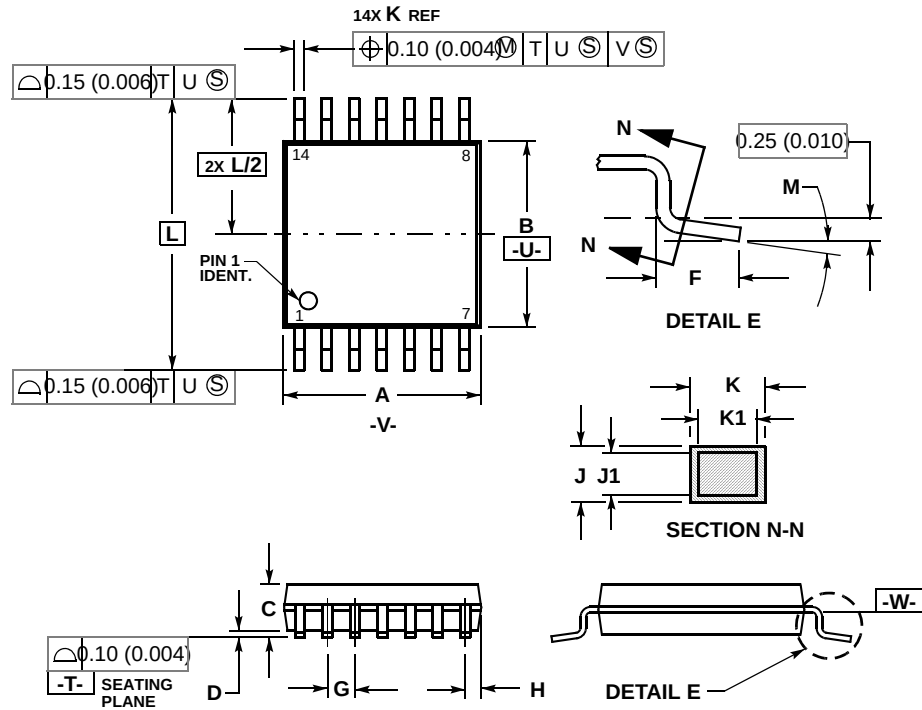


**Figure 16. Crystal Load Capacitance Contributors Schematic**

**Table 11. Pads and Tracks Parasitic Values**

| Capacitance              | Value | Unit |
|--------------------------|-------|------|
| C <sub>pad_XTAL0</sub>   | 1     | pF   |
| C <sub>pad_XTAL1</sub>   | 1     | pF   |
| C <sub>pad_CFSK</sub>    | 1     | pF   |
| C <sub>track_XTAL0</sub> | 1.5   | pF   |
| C <sub>track_XTAL1</sub> | 1.5   | pF   |
| C <sub>track_CFSK</sub>  | 1.5   | pF   |

# 15 Case Outline Dimensions



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.50        | 0.60 | 0.020     | 0.024 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

CASE 948G-01  
ISSUE O

Figure 17. Case Outline Dimensions

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