



BiCMOS LOW-POWER CURRENT-MODE PWM CONTROLLER

FEATURES

- **Enhanced Replacement for UC3842A Family With Pin-to-Pin Compatibility**
- **1-MHz Operation**
- **50- μ A Standby Current, 100- μ A Maximum**
- **Low Operating Current of 2.3 mA at 52 kHz**
- **Fast 35-ns Cycle-by-Cycle Overcurrent Limiting**
- **± 1 -A Peak Output Current**
- **Rail-to-Rail Output Swings with 25-ns Rise and 20-ns Fall Times**
- **$\pm 1\%$ Initial Trimmed 2.5-V Error Amplifier Reference**
- **Trimmed Oscillator Discharge Current**
- **New Under Voltage Lockout Versions**
- **MSOP-8 Package Minimizes Board Space**

APPLICATIONS

- **Switch-Mode Power Supplies**
- **dc-to-dc Converters**
- **Board Mount Power Modules**

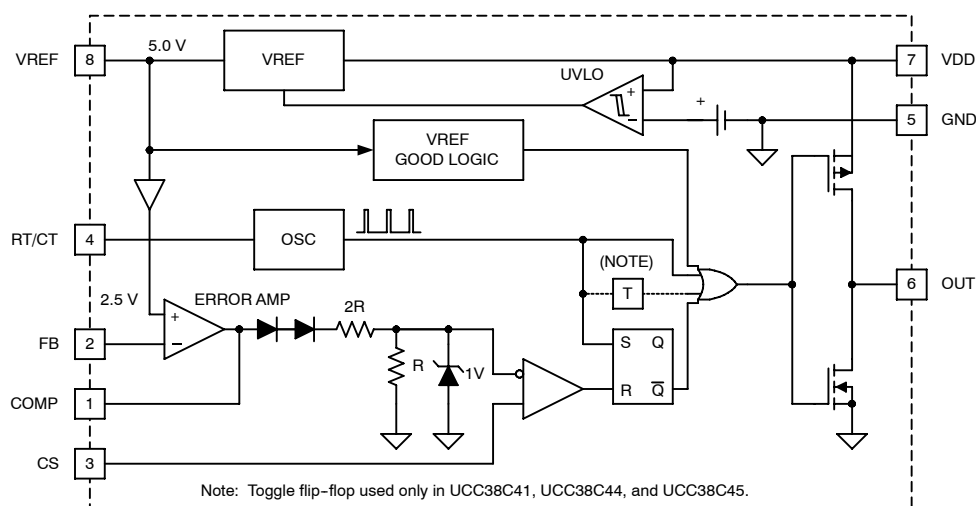
DESCRIPTION

UCC38C4x family is a high-performance current-mode PWM controller. It is an enhanced BiCMOS version with pin-for-pin compatibility to the industry standard UC384xA family and UC384x family of PWM controllers. In addition, lower startup voltage versions of 7 V are offered as UCC38C40 and UCC38C41.

Providing necessary features to control fixed frequency, peak current-mode power supplies, this family offers the following performance advantages. The device offers high-frequency operation up to 1 MHz with low start-up and operating currents, thus minimizing start-up loss and low operating power consumption for improved efficiency. The device also features a very fast current-sense-to-output delay time of 35 ns and a ± 1 A peak output current capability with improved rise and fall times for driving large external MOSFETs directly.

The UCC38C4x family is offered in 8-pin packages, MSOP (DGK), SOIC (D) and PDIP (P).

FUNCTIONAL BLOCK DIAGRAM



UDG-99139



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

UCC28C40, UCC28C41, UCC28C42, UCC28C43, UCC28C44, UCC28C45 UCC38C40, UCC38C41, UCC38C42, UCC38C43, UCC38C44, UCC38C45

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recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_{DD}		18	V
Output voltage range, V_{OUT}		18	V
Average output current, $I_{OUT}^{\dagger}$		200	mA
Reference output current, $I_{OUT(ref)}^{\dagger}$		-20	mA
Operating junction temperature, $T_J^{\dagger}$	-40	105	°C

[†] It is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)^{‡§}

Supply voltage (V_{DD})	20 V
(MAX ICC)	30 mA
Output current, I_{OUT} peak	±1 A
Output energy, capacitive load	5 µJ
Voltage rating (COMP, CS, FB)	-0.3 V to 6.3 V
(OUT)	-0.3 V to 20 V
(RT/CT)	-0.3 V to 6.3 V
(VREF)	7 V
Error amplifier output sink current	10 mA
Total Power Dissipation at $T_A = 25^{\circ}\text{C}$: D package	50 °C/W
DGK package	120°C/W
P package	65°C/W
Operating junction temperature range, T_J	-55°C to 150°C
Storage temperature range T_{stg}	-65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

[‡] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[§] All voltages are with respect to ground. Currents are positive into and negative out of the specified terminals. Consult the Packaging Section of the Databook for thermal limitations and considerations of the package.

AVAILABLE OPTIONS

$T_A = T_J$	MAXIMUM DUTY CYCLE	UVLO ON/OFF	SOIC-8 SMALL OUTLINE (D) [†]	PDIP-8 PLASTIC DIP (P)	MSOP-8 SMALL OUTLINE (DGK) [†]
-40°C to 105°C	100%	14.5V / 9.0V	UCC28C42D	UCC28C42P	UCC28C42DGK
		8.4V / 7.6V	UCC28C43D	UCC28C43P	UCC28C43DGK
		7.0V / 6.6V	UCC28C40D	UCC28C40P	UCC28C40DGK
	50%	14.5V / 9.0V	UCC28C44D	UCC28C44P	UCC28C44DGK
		8.4V / 7.6V	UCC28C45D	UCC28C45P	UCC28C45DGK
		7.0V / 6.6V	UCC28C41D	UCC28C41P	UCC28C41DGK
0°C to 70°C	100%	14.5V / 9.0V	UCC38C42D	UCC38C42P	UCC38C42DGK
		8.4V / 7.6V	UCC38C43D	UCC38C43P	UCC38C43DGK
		7.0V / 6.6V	UCC38C40D	UCC38C40P	UCC38C40DGK
	50%	14.5V / 9.0V	UCC38C44D	UCC38C44P	UCC38C44DGK
		8.4V / 7.6V	UCC38C45D	UCC38C45P	UCC38C45DGK
		7.0V / 6.6V	UCC38C41D	UCC38C41P	UCC38C41DGK

[†] D (SOIC-8) and DGK (MSOP-8) packages are available taped and reeled. Add R suffix to device type (e.g. UCC28C42DR) to order quantities of 2500 devices per reel. Tube quantities are 75 for D packages (SOIC-8) and 80 for DGK package (MSOP-8), and 50 for P package (PDIP-8).

UCC28C40, UCC28C41, UCC28C42, UCC28C43, UCC28C44, UCC28C45 UCC38C40, UCC38C41, UCC38C42, UCC38C43, UCC38C44, UCC38C45

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electrical characteristics $V_{DD} = 15\text{ V}$ (See Note 1), $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, $C_{VDD} = 0.1\mu\text{F}$ and no load on the outputs, $T_A = -40^\circ\text{C}$ to 105°C for the UCC28C4x and $T_A = 0^\circ\text{C}$ to 70°C for the UCC38C4x, $T_A = T_J$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output voltage, initial accuracy	$T_A = 25^\circ\text{C}$ $I_{OUT} = 1\text{ mA}$	4.9	5.0	5.1	V
Line regulation	$V_{DD} = 12\text{ V}$ to 18 V		0.2	20	mV
Load regulation	1 mA to 20 mA		3	25	mV
Temperature stability	See Note 2		0.2	0.4	mV/ $^\circ\text{C}$
Total output variation	See Note 2	4.82		5.18	V
Output noise voltage	10 Hz to 10 kHz, $T_A = 25^\circ\text{C}$, See Note 2		50		μV
Long term stability	1000 hours, $T_A = 125^\circ\text{C}$, See Note 2		5	25	mV
Output short circuit		-30	-45	-55	mA
Oscillator Section					
Initial accuracy	$T_A = 25^\circ\text{C}$, See Note 3	50.5	53	55	kHz
Voltage stability	$V_{DD} = 12\text{ V}$ to 18 V		0.2%	1.0%	
Temperature stability	T_{MIN} to T_{MAX} , See Note 2		1%	2.5%	
Amplitude	RT/CT Pin peak-to-peak		1.9		V
Discharge current	$T_A = 25^\circ\text{C}$, RT/CT = 2 V, See Note 4	7.7	8.4	9.0	mA
	RT/CT = 2 V, See Note 4	7.2	8.4	9.5	mA
Error Amplifier Section					
Feedback input voltage, initial accuracy	$V_{COMP} = 2.5\text{ V}$, $T_A = 25^\circ\text{C}$	2.475	2.500	2.525	V
Feedback input voltage, total variation	$V_{COMP} = 2.5\text{ V}$,	2.45	2.50	2.55	V
Input bias current	$V_{FB} = 5.0\text{ V}$		-0.1	-2.0	μA
Open-loop voltage gain (A_{VOL})	$V_{OUT} = 2\text{ V}$ to 4 V	65	90		dB
Unity gain bandwidth	See Note 2	1.0	1.5		MHz
Power supply rejection ratio (PSRR)	$V_{DD} = 12\text{ V}$ to 18 V	60			dB
Output sink current	$V_{FB} = 2.7\text{ V}$, $V_{COMP} = 1.1\text{ V}$	2	14		mA
Output source current	$V_{FB} = 2.3\text{ V}$, $V_{COMP} = 5\text{ V}$	-0.5	-1.0		mA
High-level output voltage (VOH)	$V_{FB} = 2.7\text{ V}$, $R_{LOAD} = 15\text{ k}$ to GND	5	6.8		V
Low-level output voltage (VOL)	$V_{FB} = 2.7\text{ V}$, $R_{LOAD} = 15\text{ k}$ to VREF		0.1	1.1	V
Current Sense Section					
Gain	See Note 5, 6	2.85	3.00	3.15	V/V
Maximum input signal	$V_{FB} < 2.4\text{ V}$	0.9	1.0	1.1	V
Power supply rejection ratio (PSRR)	$V_{DD} = 12\text{ V}$ to 18 V , See Note 2, 5		70		dB
Input bias current			-0.1	-2.0	μA
CS to output delay			35	70	ns
COMP to CS offset	$V_{CS} = 0\text{ V}$		1.15		V

NOTE: 1. Adjust V_{DD} above the start threshold before setting at 15 V.

NOTE: 2. Ensured by design. Not production tested.

NOTE: 3. Output frequencies of the UCC38C41, UCC38C44 and the UCC38C45 are half the oscillator frequency.

NOTE: 4. Oscillator discharge current is measured with $R_T = 10\text{ k}\Omega$ to V_{REF} .

NOTE: 5. Parameter measured at trip point of latch with $V_{FB} = 0\text{ V}$.

NOTE: 6. Gain is defined as $ACS = \frac{\Delta V_{COM}}{\Delta V_{CS}}$, $0\text{ V} \leq V_{CS} \leq 900\text{ mV}$

UCC28C40, UCC28C41, UCC28C42, UCC28C43, UCC28C44, UCC28C45 UCC38C40, UCC38C41, UCC38C42, UCC38C43, UCC38C44, UCC38C45

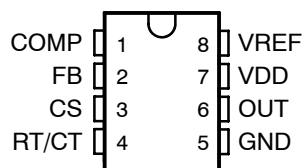
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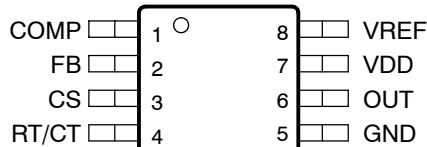
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section					
V _{OUT} low (R _{DS(on)} pull-down)	I _{SINK} = 200 mA		5.5	15	Ω
V _{OUT} high (R _{DS(on)} pull-up)	I _{SOURCE} = 200 mA		10	25	
Rise t _{lme}	T _A = 25°C, C _{LOAD} = 1 nF		25	50	ns
Fall time	T _A = 25°C, C _{LOAD} = 1 nF		20	40	
Undervoltage Lockout Section					
Start threshold	UCC38C42, UCC38C44	13.5	14.5	15.5	V
	UCC38C43, UCC38C45	7.8	8.4	9.0	
	UCC38C40, UCC38C41	6.5	7.0	7.5	
Minimum operating voltage	UCC38C42, UCC38C44	8	9	10	
	UCC38C43, UCC38C45	7.0	7.6	8.2	
	UCC38C40, UCC38C41	6.1	6.6	7.1	
PWM Section					
Maximum duty cycle	UCC38C42, UCC38C43, UCC38C40, V _{FB} < 2.4 V	94%	96%		
	UCC38C44, UCC38C45, UCC38C41, V _{FB} < 2.4 V	47%	48%		
Minimum duty cycle	V _{FB} > 2.6 V			0%	
Current Supply Section					
Start-up current (I _{START-UP})	V _{DD} = Undervoltage lockout start threshold (–0.5 V)		50	100	μA
Operating supply current (I _{DD})	V _{FB} = V _{CS} = 0 V		2.3	3.0	mA

NOTE 1: Adjust V_{DD} above the start threshold before setting at 15 V.

PDIP (P) or SOIC (D) PACKAGE
(TOP VIEW)



MSOP (DGK) PACKAGE
(TOP VIEW)



pin assignments

COMP: This pin provides the output of the error amplifier for compensation. In addition, the COMP pin is frequently used as a control port by utilizing a secondary-side error amplifier to send an error signal across the secondary-primary isolation boundary through an opto-isolator.

CS: The current sense pin is the non-inverting input to the PWM comparator. This is compared to a signal proportional to the error amplifier output voltage. A voltage ramp can be applied to this pin to run the device with a voltage mode control configuration.

FB: This pin is the inverting input to the error amplifier. The non-inverting input to the error amplifier is internally trimmed to 2.5 V $\pm$ 1%.

GND: Ground return pin for the output driver stage and the logic level controller section.

OUT: The output of the on-chip drive stage. OUT is intended to directly drive a MOSFET. The OUT pin in the UCC38C40, UCC38C42 and UCC38C43 is the same frequency as the oscillator, and can operate near 100% duty cycle. In the UCC38C41, UCC38C44 and the UCC38C45, the frequency of OUT is one-half that of the oscillator due to an internal T flipflop. This limits the maximum duty cycle to < 50%.

RT/CT: Timing resistor and timing capacitor. The timing capacitor should be connected to the device ground using minimal trace length.

VDD: Power supply pin for the device. This pin should be bypassed with a 0.1- μ F capacitor with minimal trace lengths. Additional capacitance may be needed to provide hold up power to the device during startup.

VREF: 5-V reference. For stability, the reference should be bypassed with a 0.1- μ F capacitor to ground using the minimal trace length possible.

APPLICATION INFORMATION

This device is a pin-for-pin replacement of the bipolar UC3842 family of controllers, the industry standard PWM controller for single-ended converters. Familiarity with this controller family is assumed.

The UCC28C4x/UCC38C4x series is an enhanced replacement with pin-to-pin compatibility to the bipolar UC284x/UC384x and UC284xA/UC384xA families. The new series offers improved performance when compared to older bipolar devices and other competitive BiCMOS devices with similar functionality. Note that these improvements discussed below generally consist of tighter specification limits that are a subset of the older product ratings, maintaining drop-in capability. In new designs these improvements can be utilized to reduce the component count or enhance circuit performance when compared to the previously available devices.

advantages

This device increases the total circuit efficiency whether operating off-line or in dc input circuits. In off-line applications the low start-up current of this device reduces steady state power dissipation in the startup resistor, and the low operating current maximizes efficiency while running. The low running current also provides an efficiency boost in battery operated supplies.

low voltage operation

Two members of the UCC38C4x family are intended for applications that require a lower start-up voltage than the original family members. The UCC38C40 and UCC38C41 have a turn-on voltage of 7.0 V typical and exhibit hysteresis of 0.4 V for a turn-off voltage of 6.6 V. This reduced start-up voltage enables use in systems with lower voltages, such as 12-V battery systems which are nearly discharged.

high speed operation

The BiCMOS design allows operation at high frequencies that were not feasible in the predecessor bipolar devices. First, the output stage has been redesigned to drive the external power switch in approximately half the time of the earlier devices. Second, the internal oscillator is more robust with less variation as frequency increases. In addition, the current sense to output delay has been reduced by a factor of three, to 45ns typical. These features combine to provide a device capable of reliable high frequency operation.

The UCC38C4x family oscillator is true to the curves of the original bipolar devices at lower frequencies yet extends the frequency programmability range to at least 1MHz. This allows the device to offer pin to pin capability where required yet capable of extending the operational range to the higher frequencies typical of latest applications. When the original UC3842 was released in 1984 most switching supplies operated between 20kHz and 100kHz. Today, the UCC38C4x can be used in designs cover a span roughly ten times higher than those numbers.

start/run current improvements

The start-up current is only 60 μ A typical, a significant reduction from the bipolar device's ratings of 300 μ A (UC384xA). For operation over the temperature range of -40 to 85°C the UCC28C4x devices offer a maximum startup current of 100 μ A, an improvement over competitive BiCMOS devices. This allows the power supply designer to further optimize the selection of the startup resistor value to provide a more efficient design. In applications where low component cost overrides maximum efficiency the low run current of 2.3 mA, typical, may allow the control device to run directly through the single resistor to (+) rail, rather than needing a bootstrap winding on the power transformer, along with a rectifier. The start/run resistor for this case must also pass enough current to allow driving the primary switching MOSFET, which may be a few milliamps in small devices.

APPLICATION INFORMATION

± 1% initial reference voltage

The BiCMOS internal reference of 2.5 V has an enhanced design and utilizes production trim to allow initial accuracy of $\pm 1\%$ at room temperature and $\pm 2\%$ over the full temperature range. This can be used to eliminate an external reference in applications that do not require the extreme accuracy afforded by the additional device. This is very useful for nonisolated dc-to-dc applications where the control device is referenced to the same common as the output. It is also applicable in offline designs that regulate on the primary side of the isolation boundary by looking at a primary bias winding, or perhaps from a winding on the output inductor of a buck-derived circuit.

reduced discharge current variation

The original UC3842 oscillator did not have trimmed discharged current, and the parameter was not specified on the datasheet. Since many customers attempted to use the discharge current to set a crude deadtime limit the UC3842A family was released with a trimmed discharge current specified at 25°C. The UCC28C4x/UCC38C4x series now offers even tighter control of this parameter, with approximately $\pm 3\%$ accuracy at 25°C, and less than 10% variation over temperature using the UCC28C4x devices. This level of accuracy can enable a meaningful limit to be programmed, a feature not currently seen in competitive BiCMOS devices. The improved oscillator and reference also contribute to decreased variation in the peak to peak variation in the oscillator waveform, which is often used as the basis for slope compensation for the complete power system.

soft-start

The following diagram provides a typical soft-start circuit for use with the UCC38C42. The values of R and C should be selected to bring the COMP pin up at a controlled rate, limiting the peak current supplied by the power stage. After the soft-start interval is complete the capacitor continues to charge to V_{REF} , effectively removing the PNP transistor from circuit considerations.

The optional diode in parallel with the resistor forces a soft-start each time the PWM goes through UVLO and the reference (V_{REF}) goes low. Without the diode, the capacitor otherwise remains charged during a brief loss of supply or brown-out, and no soft-start is enabled upon reapplication of V_{IN} .

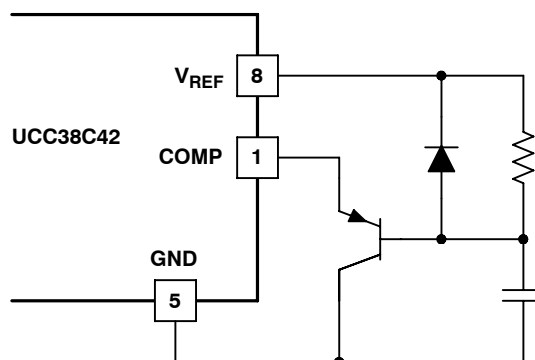


Figure 1

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oscillator synchronization

The diagram shows the synchronization input circuit for the UCC38C42 PWM controller. A square wave pulse, labeled "SYNCHRONIZATION CIRCUIT INPUT", is applied to the input of a capacitor C_T . The other end of C_T is connected to a node that also branches to a resistor R_T and the pin 4 of the UCC38C42. Pin 4 is labeled R_T / C_T . The other end of R_T is connected to pin 8, which is labeled V_{REF} . The bottom terminals of both C_T and R_T are connected to a common ground, which is also the ground of the UCC38C42. A $24\ \Omega$ resistor is connected between the input pulse source and the junction of C_T and the ground.

UDG-01069

The diagram illustrates the timing relationship for the CTCT module. It shows three main signals over time:

- CLOCK INPUT:** A periodic signal alternating between LOW and HIGH states. The transitions are marked by horizontal arrows labeled "UPPER THRESHOLD" and "LOWER THRESHOLD".
- PWM OUT:** A pulse-width modulated signal that is "ON" during the HIGH phase of the clock input and "OFF" during the LOW phase. The output is labeled "OUTPUT A".
- CTCT Input Signals:**
 - V_{CT} (ANALOG): A sawtooth waveform that ramps up linearly and then resets.
 - V_{SYNC} (DIGITAL): A square wave that is high during the "ON" phase of the PWM OUT and low during the "OFF" phase.
 - COMBINED:** The resulting signal after combining the analog and digital inputs. It shows the sawtooth ramp being reset at the rising edge of the digital sync signal, which occurs at the upper threshold of the clock input.

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Figure 3. Synchronization to an External Clock

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APPLICATION INFORMATION

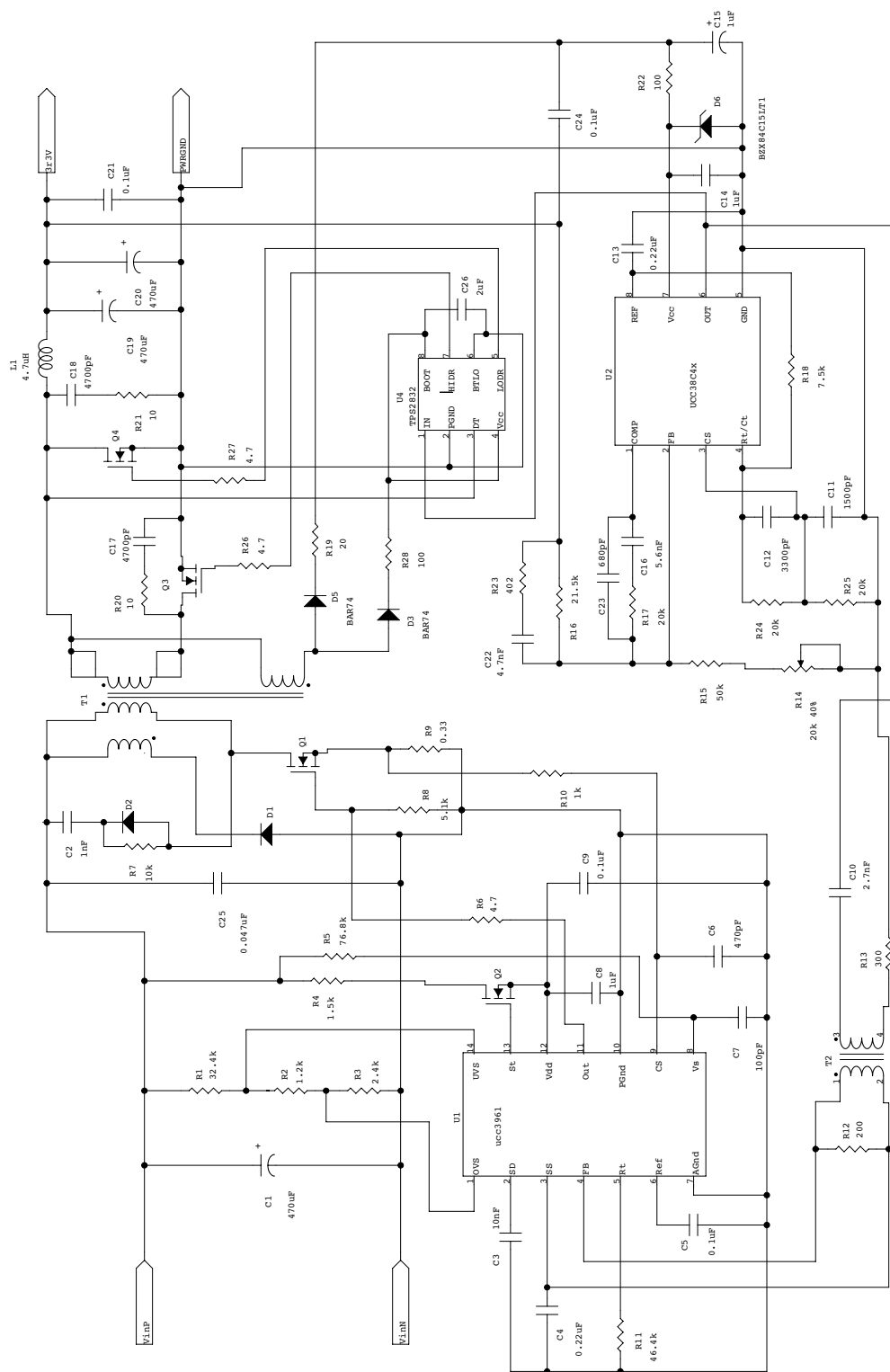


Figure 5. Forward Converter with Synchronous Rectification Using the UCC38C42 as the Secondary-Side Controller

TYPICAL CHARACTERISTICS

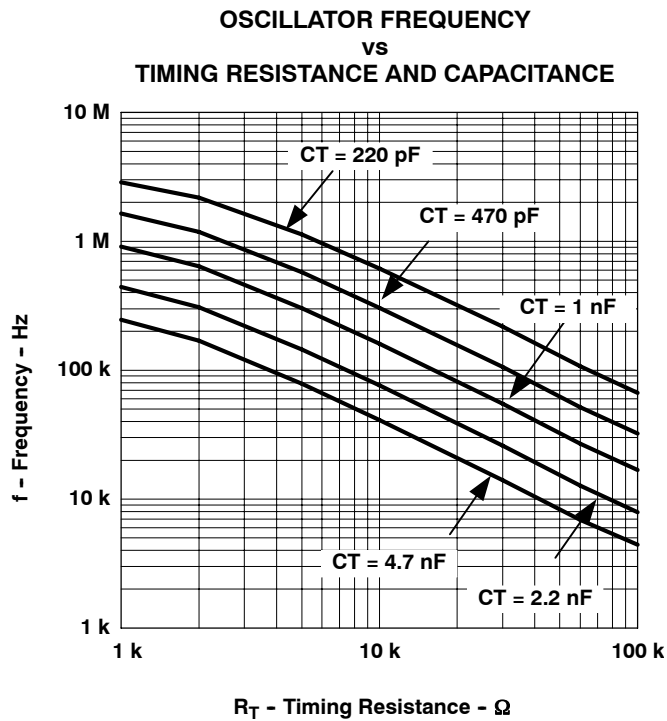


Figure 6

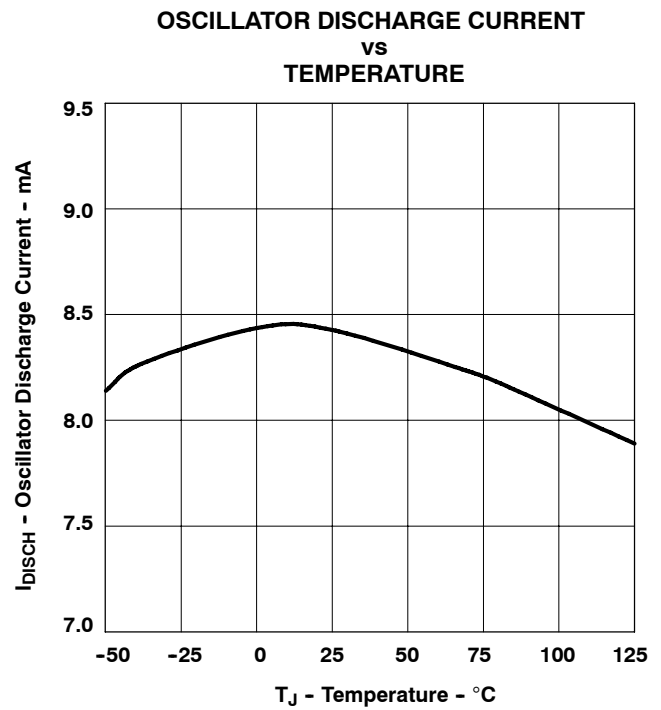


Figure 7

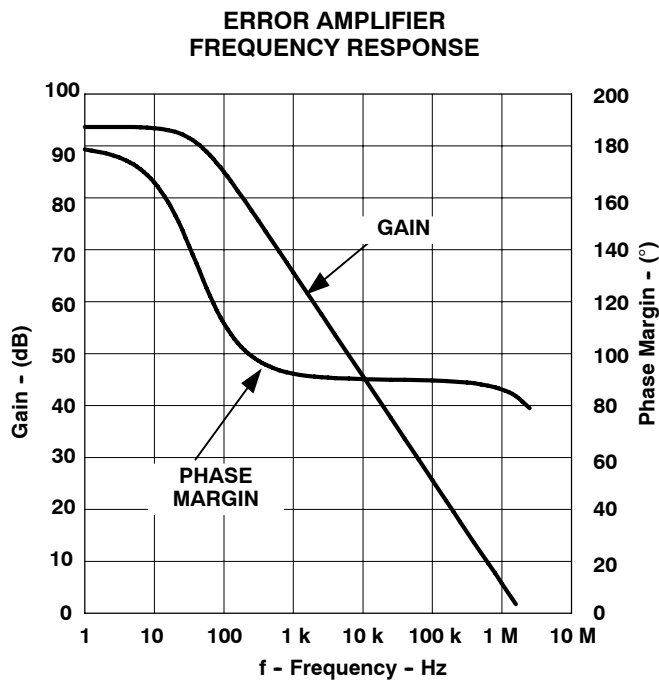


Figure 8

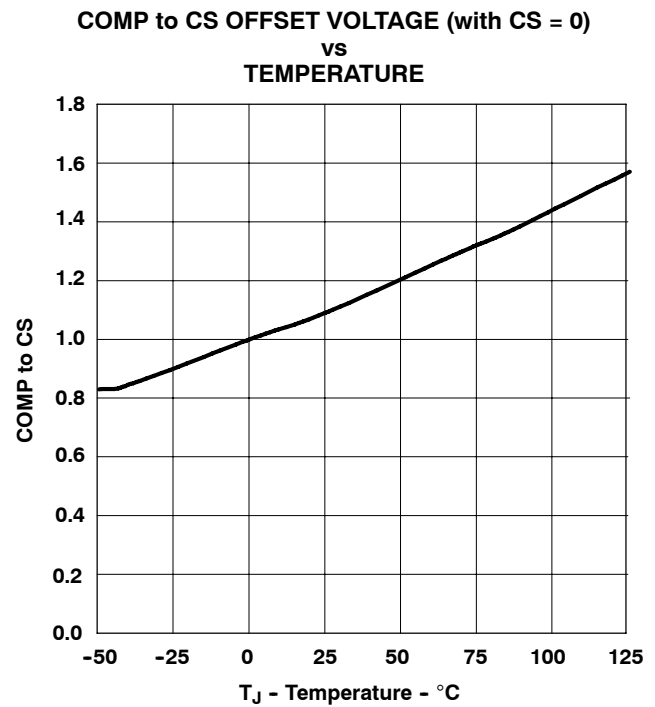


Figure 9

TYPICAL CHARACTERISTICS

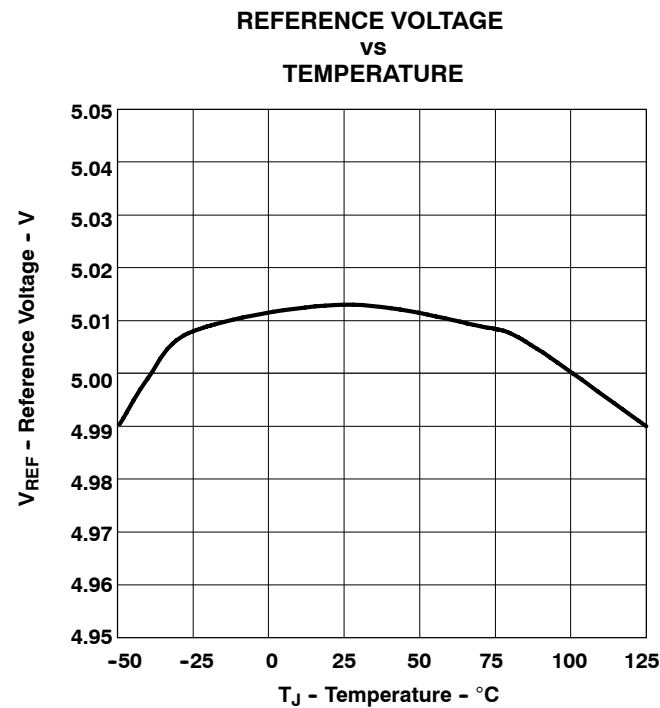


Figure 10

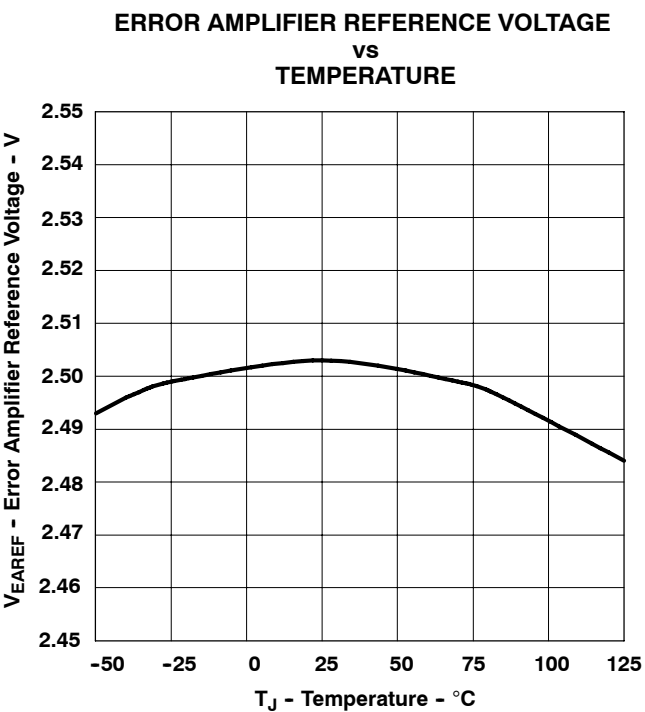


Figure 11

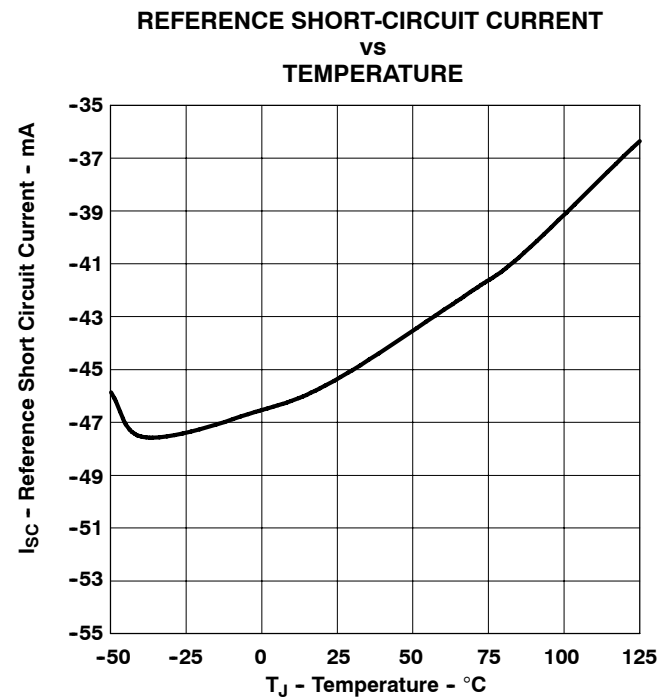


Figure 12

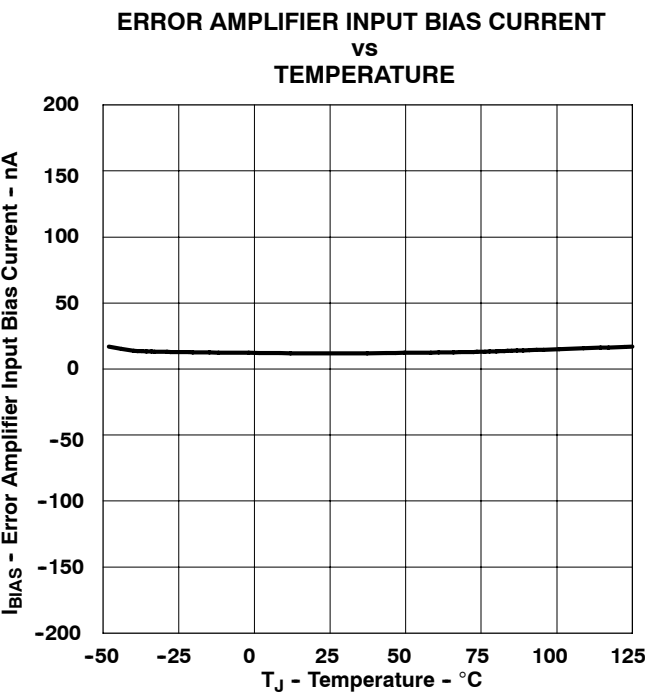


Figure 13

TYPICAL CHARACTERISTICS

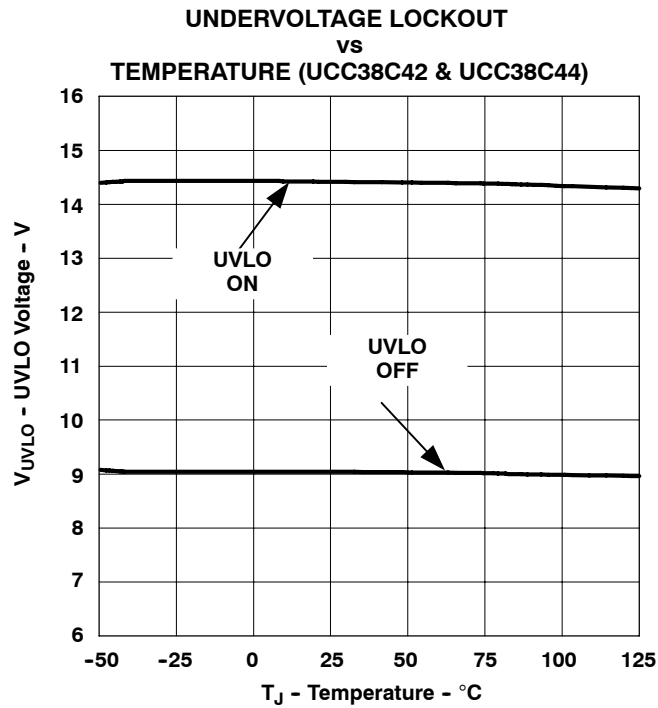


Figure 14

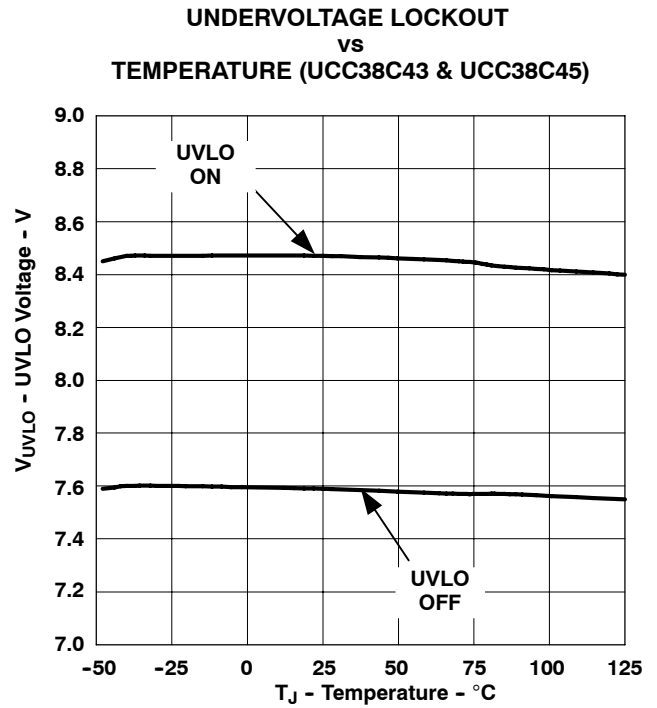


Figure 15

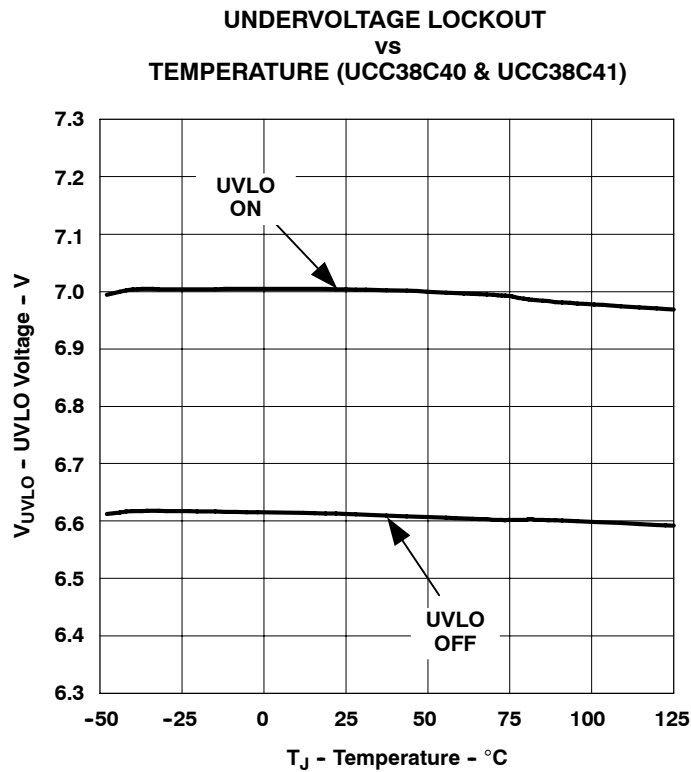


Figure 16

TYPICAL CHARACTERISTICS

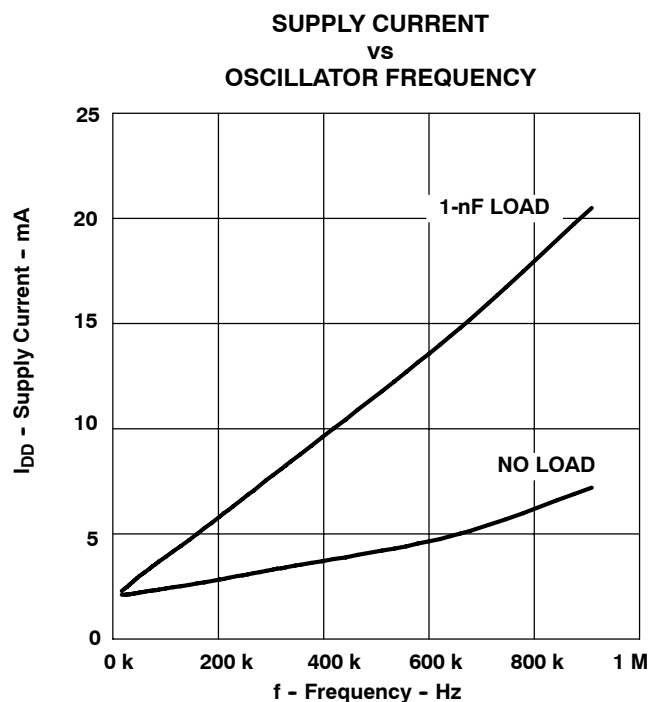


Figure 17

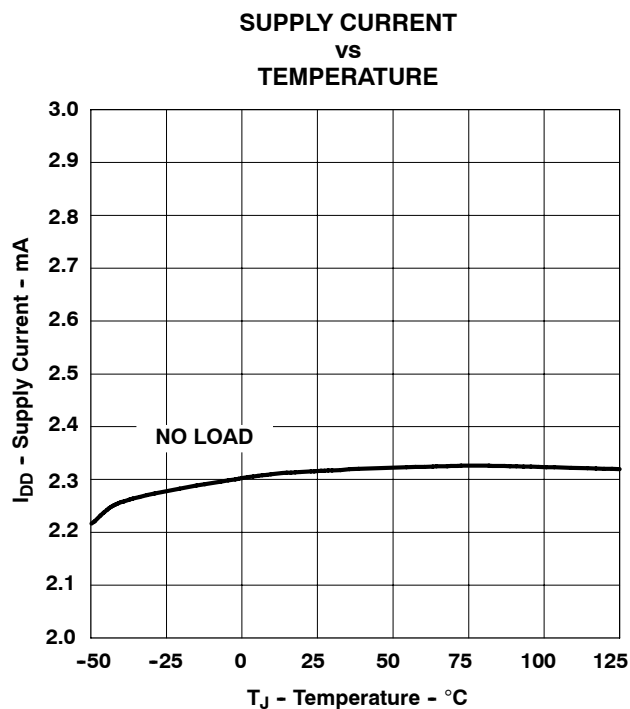


Figure 18

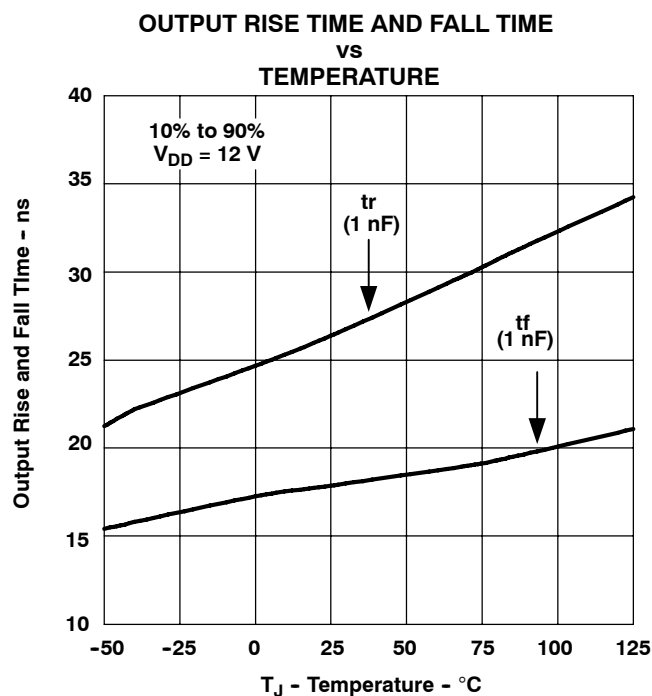


Figure 19

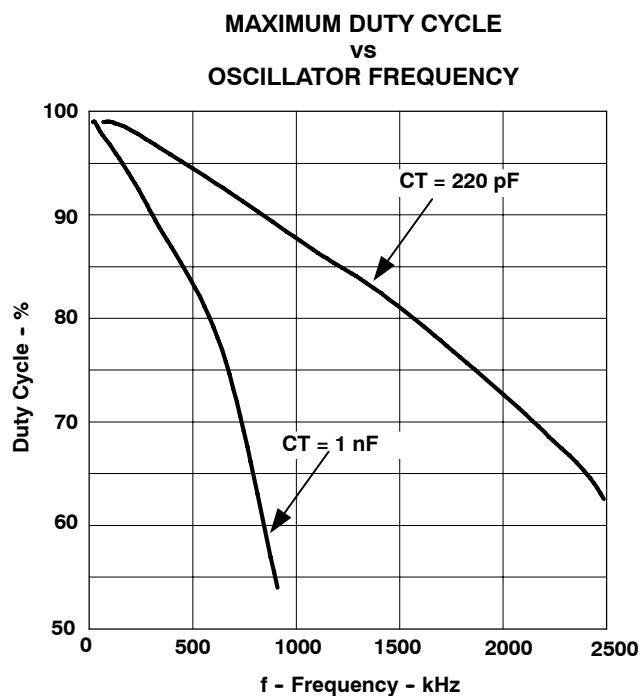


Figure 20

TYPICAL CHARACTERISTICS

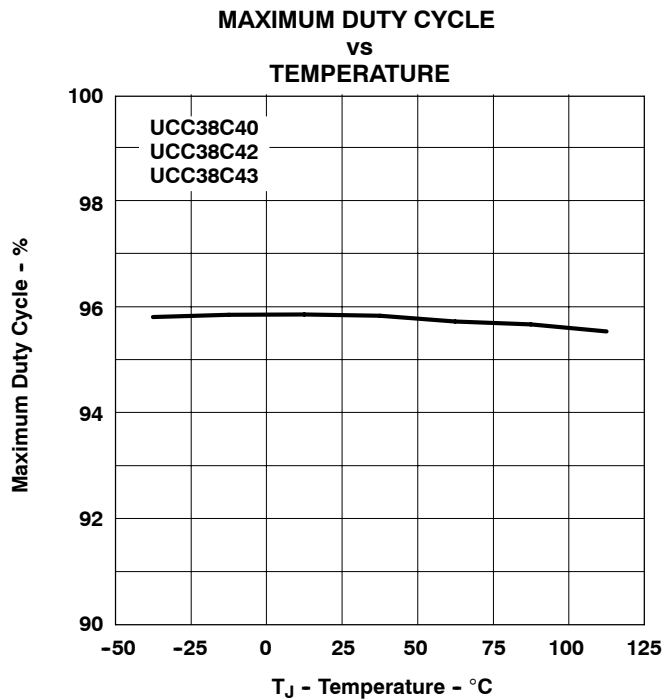


Figure 21

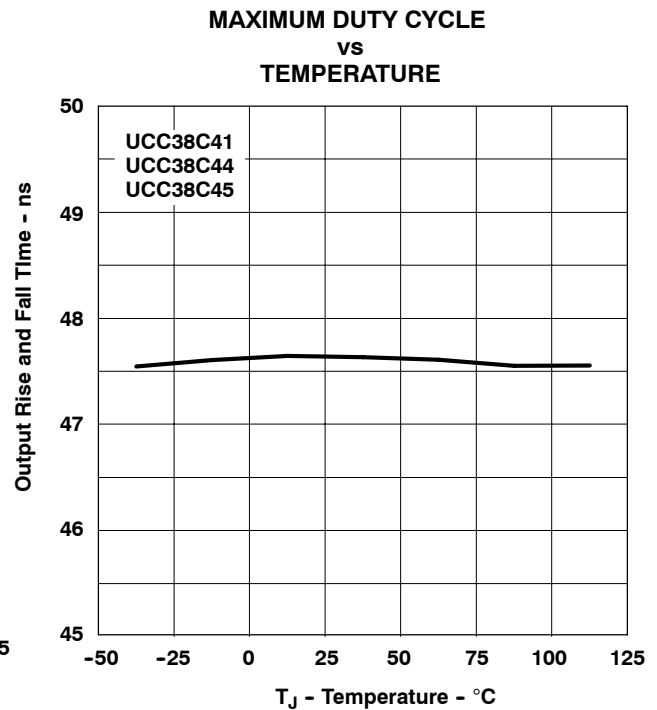


Figure 22

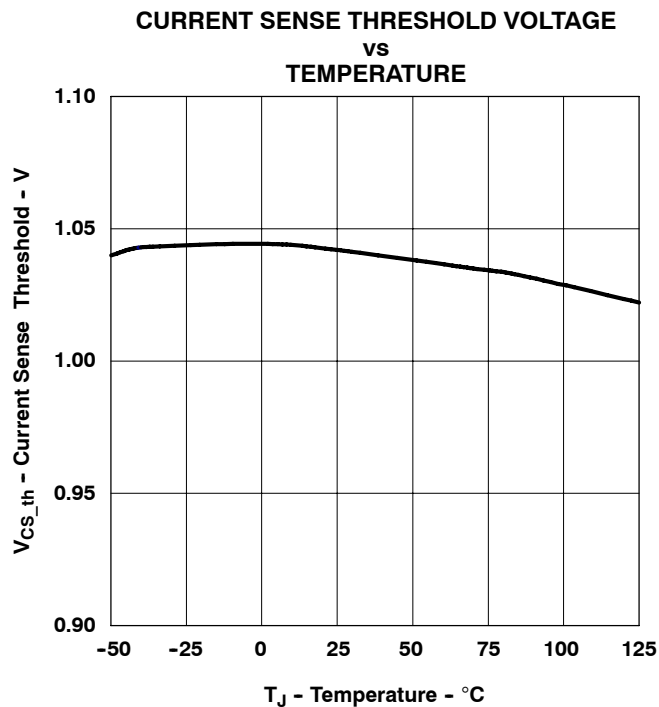


Figure 23

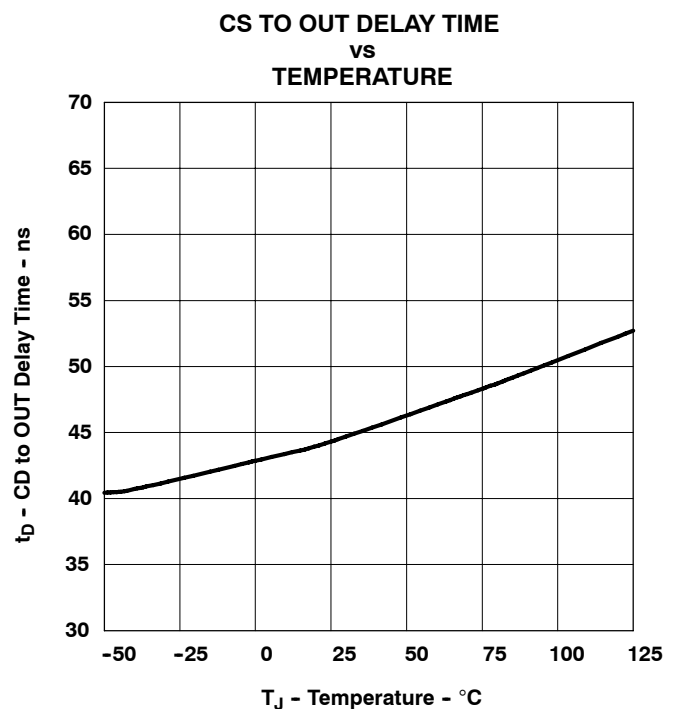


Figure 24

Revision History

Revision SLUS458D to SLUS458E, 10/2010

- 1) Updated Operating Junction Temperature in the Recommended Operating Conditions Table, from -55 to 150 to -40 to 105.
- 2) Updated Available Options Table heading from T_A to $T_A = T_J$.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
UCC28C40D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C40DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C40DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C40DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C40DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C40DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C40DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C40DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C40P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC28C40PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC28C41D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C41DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C41DGK	ACTIVE	VSSOP	DGK	8	100	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C41DGKG4	ACTIVE	VSSOP	DGK	8	100	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C41DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C41DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C41DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
UCC28C41DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C42D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C42DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C42DGK	ACTIVE	VSSOP	DGK	8	100	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C42DGKG4	ACTIVE	VSSOP	DGK	8	100	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C42DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C42DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C42DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C42DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C42P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC28C42PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC28C43D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C43DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C43DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C43DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C43DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C43DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C43DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
UCC28C43DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C43P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC28C43PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC28C44D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C44DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C44DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C44DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C44DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C44DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C44DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C44DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C44P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC28C44PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC28C45D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C45DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C45DGK	ACTIVE	VSSOP	DGK	8	100	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C45DGKG4	ACTIVE	VSSOP	DGK	8	100	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC28C45DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
UCC28C45DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC28C45DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C45DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC28C45P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC28C45PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC38C40D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C40DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C40DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38C40DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38C40DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38C40DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38C40DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C40DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C40P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC38C40PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC38C41D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C41DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C41DGK	ACTIVE	VSSOP	DGK	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
UCC38C41DGKG4	ACTIVE	VSSOP	DGK	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38C41DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C41DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C41P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC38C41PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC38C42D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C42DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C42DGK	ACTIVE	VSSOP	DGK	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38C42DGKG4	ACTIVE	VSSOP	DGK	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38C42DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38C42DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38C42DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C42DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C42P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC38C42PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC38C43D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C43DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C43DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
UCC38C43DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38C43DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38C43DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38C43DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C43DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C43P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC38C43PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC38C44D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C44DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C44DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38C44DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38C44DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38C44DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UCC38C44DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C44DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C44P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC38C44PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC38C45D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
UCC38C45DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C45DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC38C45DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC38C45DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC38C45DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	
UCC38C45DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C45DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UCC38C45P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UCC38C45PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

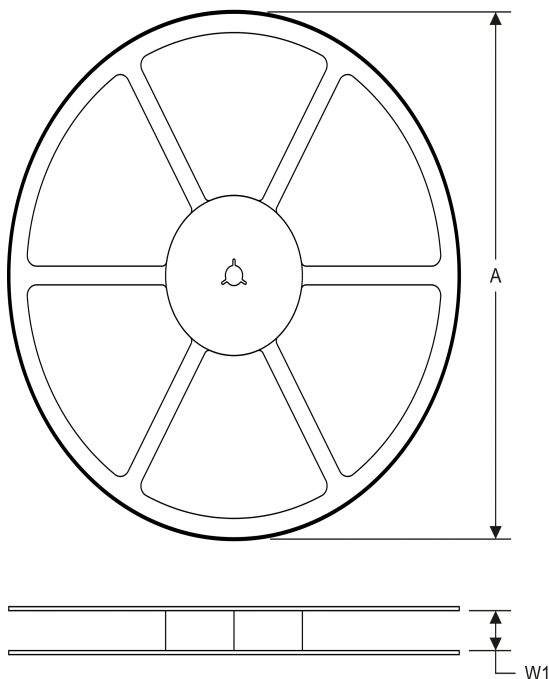
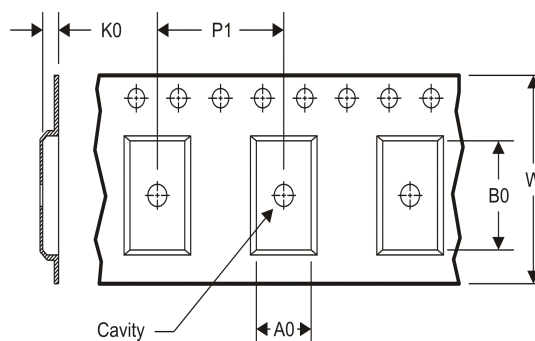
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC28C41, UCC28C43, UCC28C45 :

- Automotive: [UCC28C41-Q1](#)
- Enhanced Product: [UCC28C43-EP](#), [UCC28C45-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

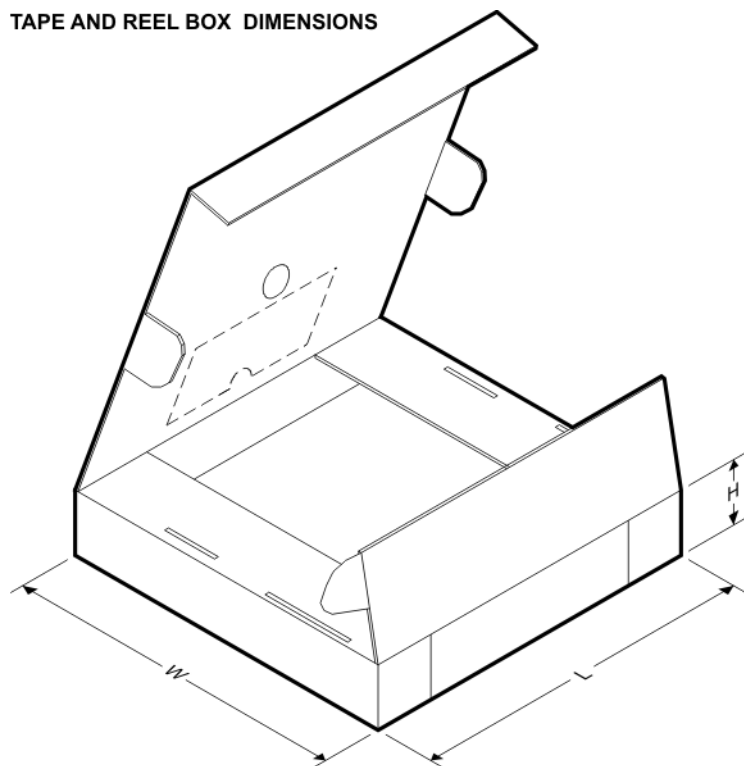
TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28C40DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C40DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C41DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C41DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C42DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C42DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C43DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C43DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C44DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C44DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC28C45DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC28C45DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC38C40DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC38C40DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC38C41DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC38C42DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC38C42DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC38C43DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC38C43DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC38C44DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC38C44DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC38C45DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC38C45DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28C40DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
UCC28C40DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC28C41DGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
UCC28C41DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC28C42DGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
UCC28C42DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC28C43DGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
UCC28C43DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC28C44DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
UCC28C44DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC28C45DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
UCC28C45DR	SOIC	D	8	2500	340.5	338.1	20.6

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC38C40DGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
UCC38C40DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC38C41DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC38C42DGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
UCC38C42DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC38C43DGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
UCC38C43DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC38C44DGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
UCC38C44DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC38C45DGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
UCC38C45DR	SOIC	D	8	2500	340.5	338.1	20.6

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

DGK (S-PDSO-G8)

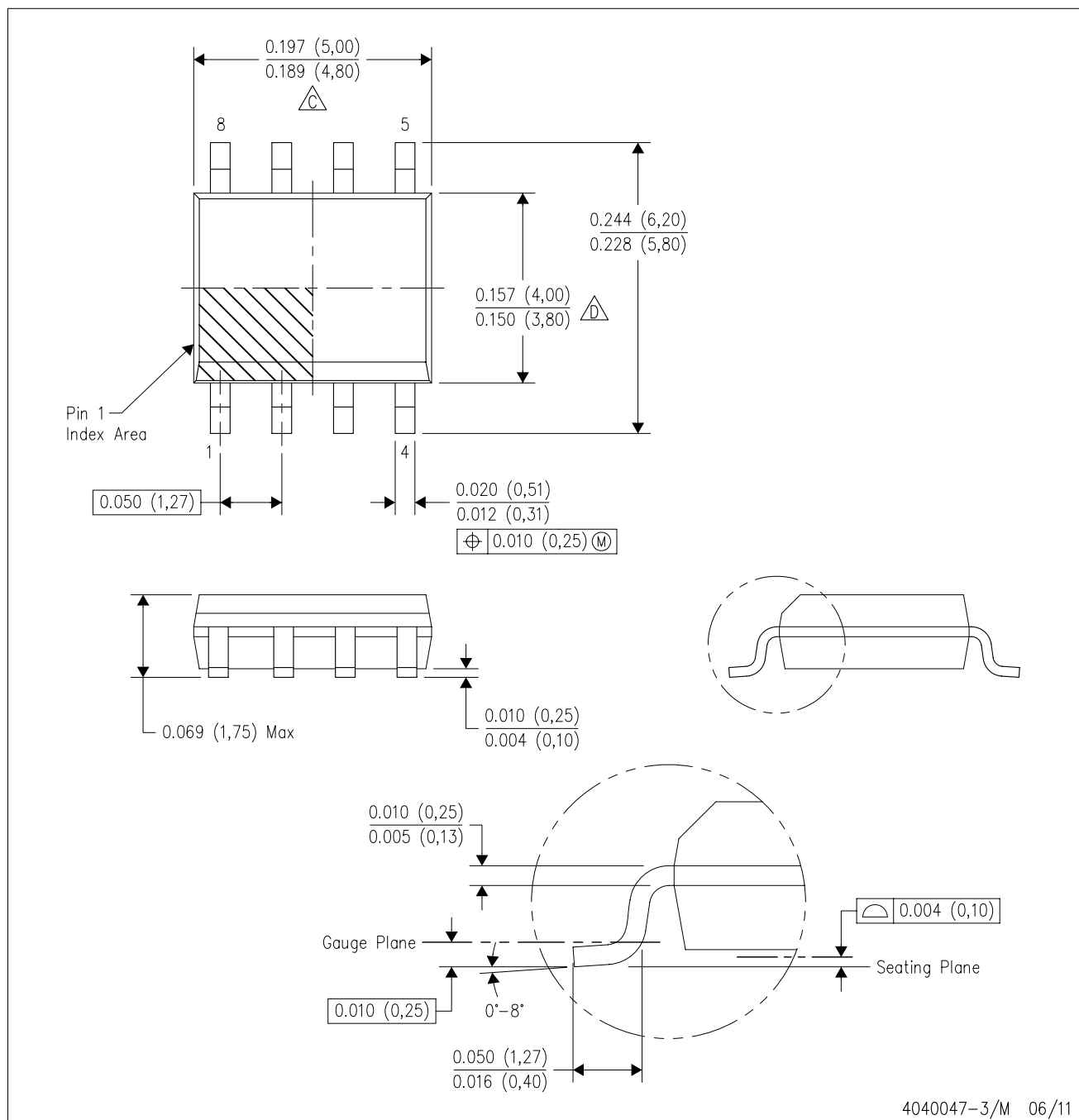
PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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