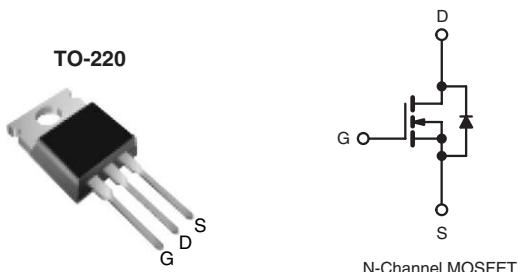


# Power MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	500
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10$ V    0.450
$Q_g$ (Max.) (nC)	81
$Q_{gs}$ (nC)	20
$Q_{gd}$ (nC)	36
Configuration	Single



## FEATURES

- Lower Gate Charge  $Q_g$  Results in Simpler Drive Requirements
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage
- Lead (Pb)-free Available


**RoHS\***  
COMPLIANT

## APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supplies
- High Speed Power Switching

## ORDERING INFORMATION

Package	TO-220
Lead (Pb)-free	IRFB13N50APbF SiHFB13N50A-E3
SnPb	IRFB13N50A SiHFB13N50A

## ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	500	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current	$I_D$	14	A
		9.1	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	56	
Linear Derating Factor		2.0	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	560	mJ
Avalanche Current <sup>a</sup>	$I_{AR}$	14	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	25	mJ
Maximum Power Dissipation	$P_D$	250	W
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	9.2	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting  $T_J = 25$  °C,  $L = 5.7$  mH,  $R_G = 25$  Ω,  $I_{AS} = 14$  A,  $dV/dt = 7.6$  V/ns (see fig. 12a).
- $I_{SD} \leq 14$  A,  $dI/dt \leq 250$  A/μs,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

**THERMAL RESISTANCE RATINGS**

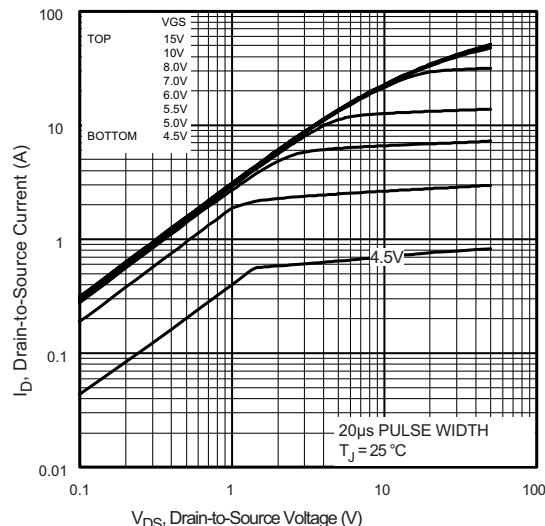
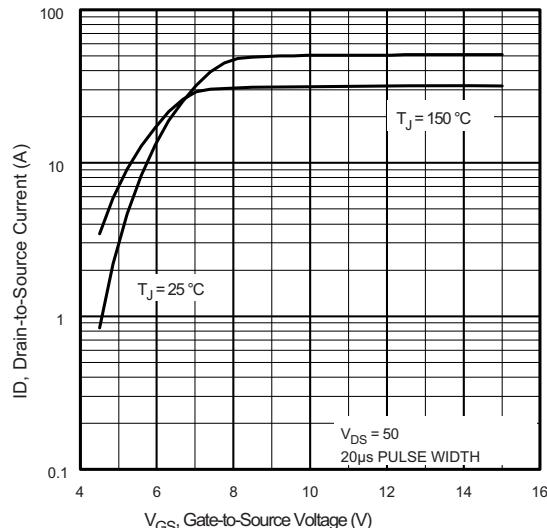
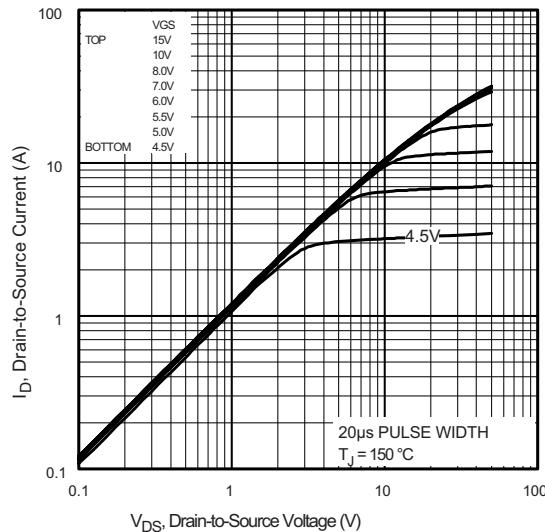
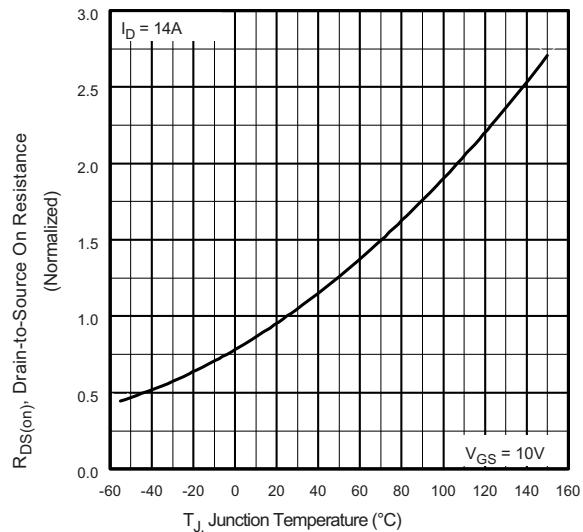
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	$^{\circ}\text{C}/\text{W}$
Case-to-Sink, Flat, Greasd Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.50	

**SPECIFICATIONS**  $T_J = 25 \text{ }^{\circ}\text{C}$ , unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$		500	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25 \text{ }^{\circ}\text{C}$ , $I_D = 1 \text{ mA}$		-	0.55	-	$\text{V}/\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30 \text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500 \text{ V}$ , $V_{GS} = 0 \text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 400 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_J = 125 \text{ }^{\circ}\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 8.4 \text{ A}^b$	-	-	0.450	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50 \text{ V}$ , $I_D = 8.4 \text{ A}$		8.1	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 25 \text{ V}$ , $f = 1.0 \text{ MHz}$ , see fig. 5		-	1910	-	pF
Output Capacitance	$C_{oss}$			-	290	-	
Reverse Transfer Capacitance	$C_{rss}$			-	11	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0 \text{ V}$	$V_{DS} = 1.0 \text{ V}$ , $f = 1.0 \text{ MHz}$	-	2730	-	pF
			$V_{DS} = 400 \text{ V}$ , $f = 1.0 \text{ MHz}$	-	82	-	
Effective Output Capacitance	$C_{oss eff.}$		$V_{DS} = 0 \text{ V}$ to $400 \text{ V}^c$	-	160	-	
Total Gate Charge	$Q_g$	$I_D = 14 \text{ A}$ , $V_{DS} = 400 \text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	81	nC	
Gate-Source Charge	$Q_{gs}$		-	-	20		
Gate-Drain Charge	$Q_{gd}$		-	-	36		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250 \text{ V}$ , $I_D = 14 \text{ A}$ , $R_G = 7.5 \Omega$ , see fig. 10 <sup>b</sup>	-	15	-	ns	
Rise Time	$t_r$		-	39	-		
Turn-Off Delay Time	$t_{d(off)}$		-	39	-		
Fall Time	$t_f$		-	31	-		
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	14	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	56	
Body Diode Voltage	$V_{SD}$	$T_J = 25 \text{ }^{\circ}\text{C}$ , $I_S = 14 \text{ A}$ , $V_{GS} = 0 \text{ V}^b$		-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25 \text{ }^{\circ}\text{C}$ , $I_F = 14 \text{ A}$ , $T_J = 125 \text{ }^{\circ}\text{C}$ , $dI/dt = 100 \text{ A}/\mu\text{s}^b$	-	370	550	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	4.4	6.5	$\mu\text{C}$	
Body Diode Reverse Recovery Current	$I_{RRM}$		-	21	31	A	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

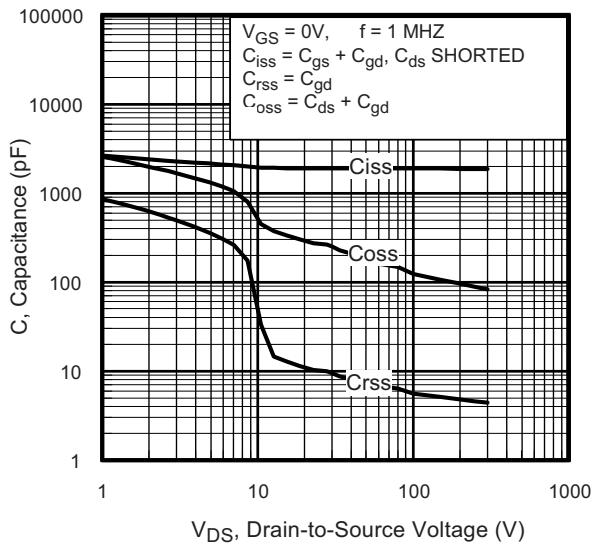
**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
b. Pulse width  $\leq 300 \mu\text{s}$ ; duty cycle  $\leq 2 \%$ .  
c.  $C_{oss eff.}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80 %  $V_{DS}$ .

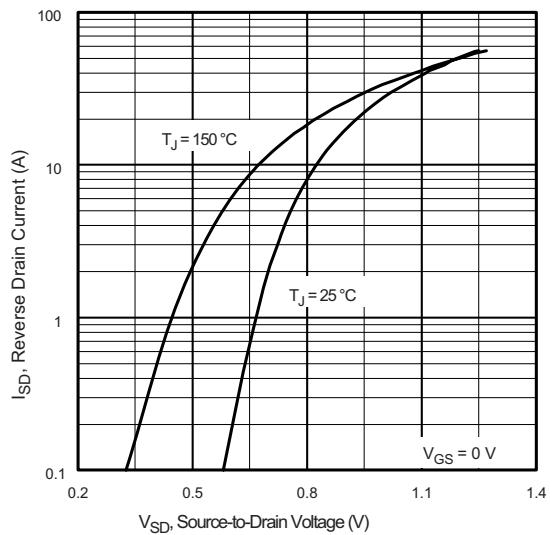
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Fig. 1 - Typical Output Characteristics**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 2 - Typical Output Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**

# IRFB13N50A, SiHFB13N50A

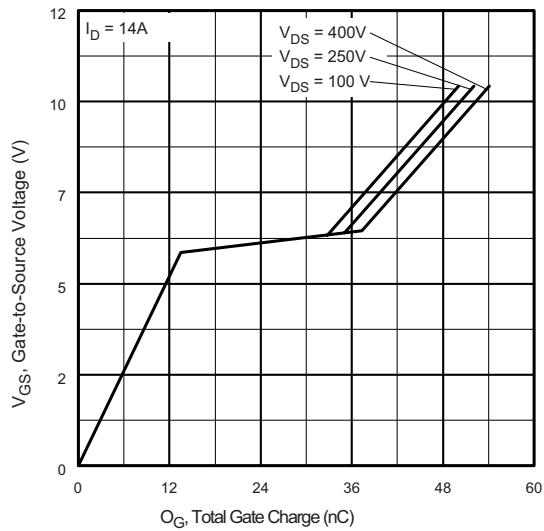
Vishay Siliconix



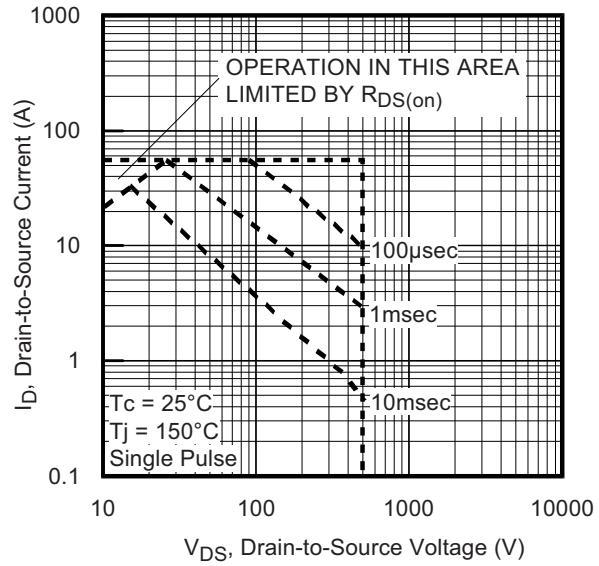
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 7 - Typical Source-Drain Diode Forward Voltage**



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**



**Fig. 8 - Maximum Safe Operating Area**

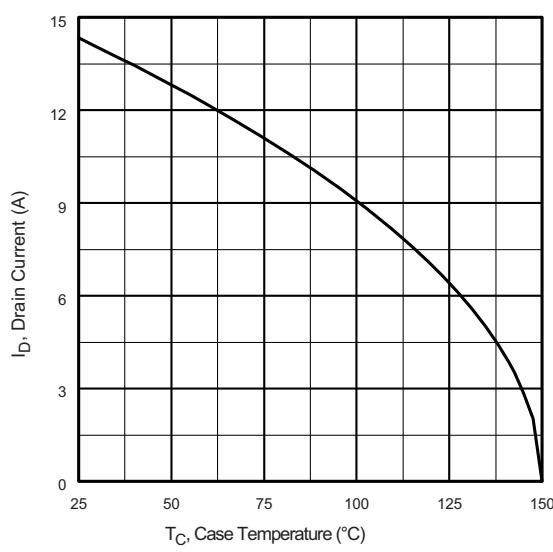


Fig. 9 - Maximum Drain Current vs. Case Temperature

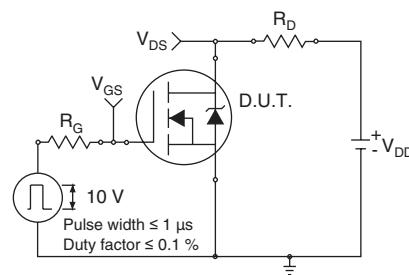


Fig. 10a - Switching Time Test Circuit

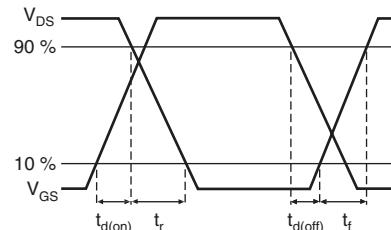


Fig. 10b - Switching Time Waveforms

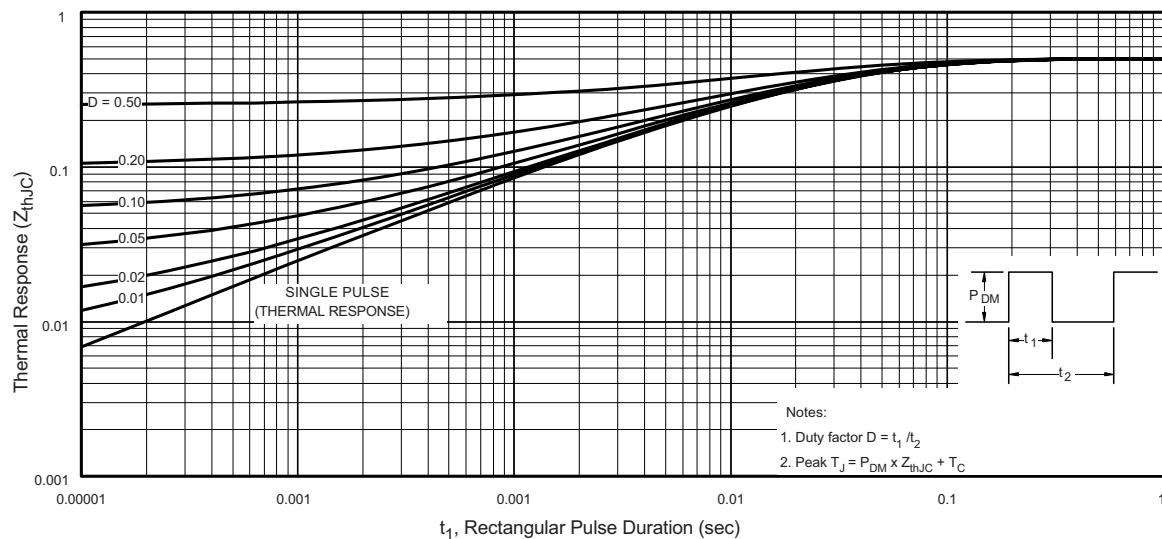


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

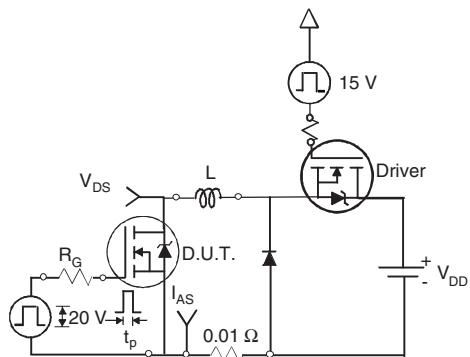


Fig. 12a - Unclamped Inductive Test Circuit

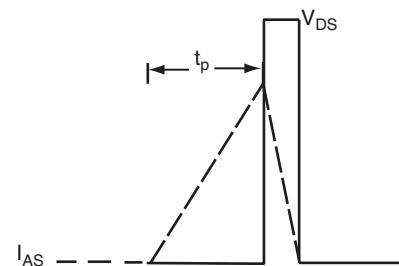
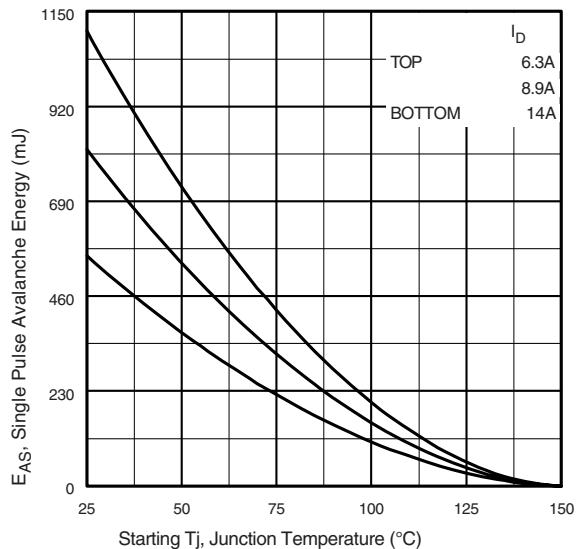
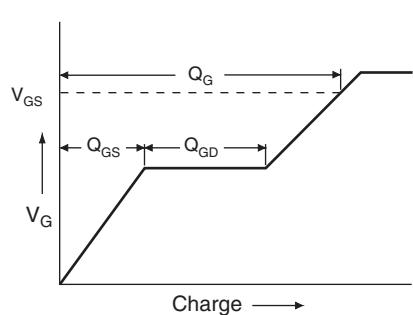


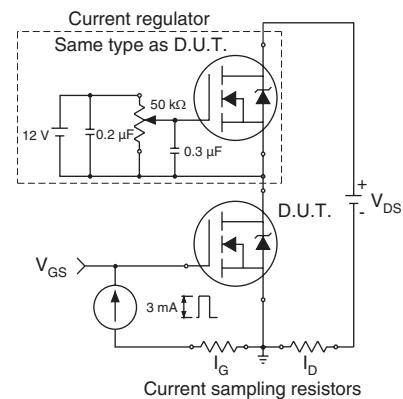
Fig. 12b - Unclamped Inductive Waveforms



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

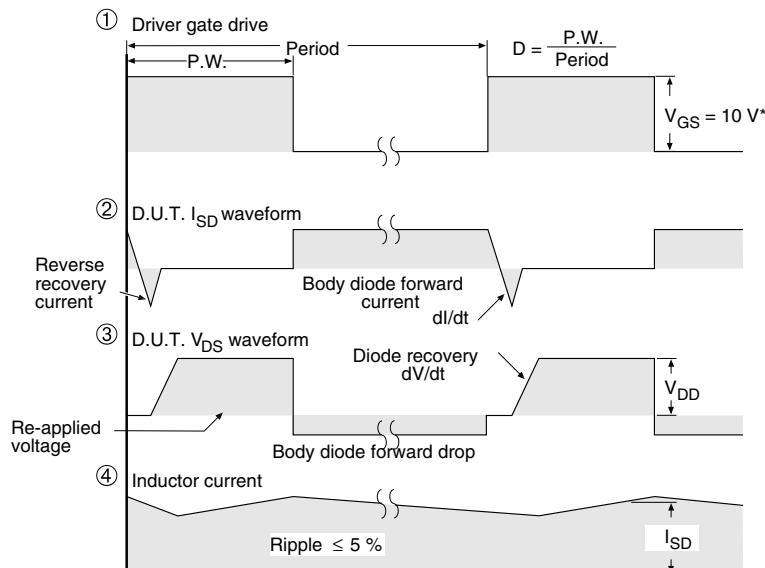
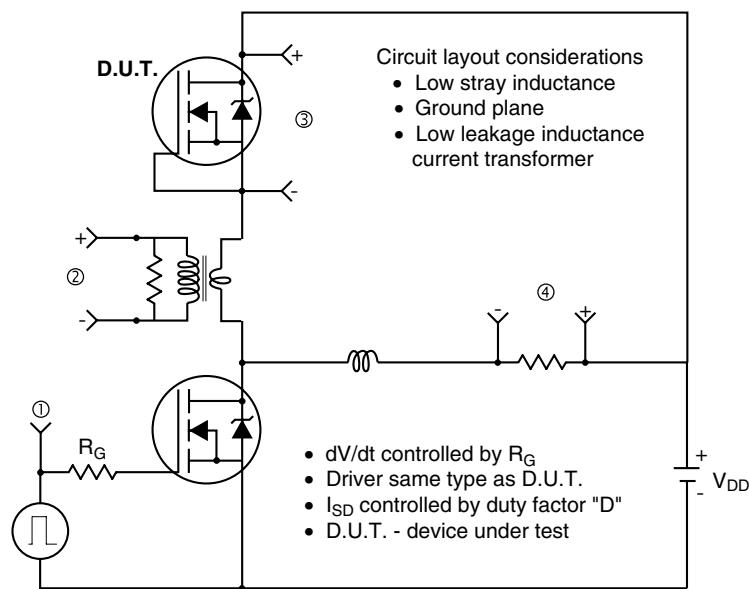


**Fig. 13a - Basic Gate Charge Waveform**



**Fig. 13b - Gate Charge Test Circuit**

### Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS} = 5 \text{ V}$  for logic level devices

Fig. 14 - For N-Channel

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