3.3 V Dual LVTTL/LVCMOS to Differential LVPECL Buffer

FEATURES

- **Dual 3.3V LVTTL to LVPECL Buffer**
- **Operating Range**
  - **LVPECL V_{CC} = 3.0 V to 3.6 V With GND = 0 V**
- **Support for Clock Frequencies to 2.0 GHz (typ)**
- **420 ps Typical Propagation Delay**
- **Deterministic HIGH Output Value for Open Input Conditions**
- **Built-in Temperature Compensation**
- **Drop in Compatible to MC100ELT23**
- **PNP Single Ended Inputs for Minimal Loading**

APPLICATIONS

- **Data and Clock Transmission Over Backplane**
- **Signaling Level Conversion**

DESCRIPTION

The SN65EPT22 is a low power dual LVTTL to LVPECL translator device. The device includes circuitry to maintain known logic HIGH level when inputs are in open condition. The SN65EPT22 is housed in an industry standard SOIC-8 package and is also available in TSSOP-8 package option.

PINOUT ASSIGNMENT

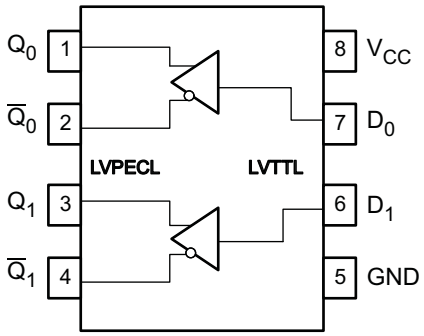


Table 1. Pin Description

PIN	FUNCTION
D_0, D_1	LVTTL data inputs
Q_0, $\overline{Q}_0$, Q_1, $\overline{Q}_1$	LVPECL outputs
V_{CC}	Positive supply
GND	Ground

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65EPT22D	SN65EPT22	SOIC	NiPdAu
SN65EPT22DGK	SN65EPT22	SOIC-TSSOP	NiPdAu

(1) Leaded device options not initially available. Contact sales representative for further details.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER	CONDITION	VALUE	UNIT
Absolute supply voltage, V_{CC}		6	V
Absolute input voltage, VI	GND = 0 and VI ≤ V_{CC}	0 to 6	V
Supply voltage LVPEL		3.3	V
Output current	Continuous	50	mA
	Surge	100	
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	POWER RATING T_A < 25°C (mW)	THERMAL RESISTANCE, JUNCTION TO AMBIENT NO AIRFLOW	DERATING FACTOR T_A > 25°C (mW/°C)	POWER RATING T_A = 85°C (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
SOIC-TSSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

THERMAL CHARACTERISTICS

PARAMETER		PACKAGE	VALUE	UNIT
θ_{JB}	Junction-to Board Thermal Resistance	SOIC	79	°C/W
		SOIC-TSSOP	120	
θ_{JC}	Junction-to Case Thermal Resistance	SOIC	98	°C/W
		SOIC-TSSOP	74	

KEY ATTRIBUTES

CHARACTERISTICS	VALUE
Moisture sensitivity level	Lead free package
SOIC-8	Level 1
TSSOP-8	Level 3
Flammability rating (Oxygen Index: 28 to 34)	UL 94 V-0 at 0.125 in
ESD-HBM	4 kV
ESD-machine model	200 V
ESD-charge device model	2 kV
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test	

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TTL INPUT DC CHARACTERISTICS[1] (V_{CC} = 3.3 V, GND = 0, T_A = –40°C to 85°C)

CHARACTERISTIC		CONDITION	MIN	TYP	MAX	UNIT
I_{IH}	Input HIGH current	V_{IN} = 2.7 V			20	µA
I_{IHH}	Input HIGH current max	V_{IN} = V_{CC}			100	µA
I_{IL}	Input LOW current	V_{IN} = 0.5 V			–0.6	mA
V_{IK}	Input clamp voltage	I_{IN} = –18 mA			–1	V
V_{IH}	Input high voltage		2.0			V
V_{IL}	Input low voltage				0.8	V

(1) Device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

PECL OUTPUT DC CHARACTERISTICS[1] (V_{CC} = 3.3 V; GND = 0.0V) [2]

CHARACTERISTIC		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Power supply current		39	45		42	47		45	50	mA
V_{OH}	Output HIGH voltage [3]	2155	2224	2405	2155	2224	2405	2155	2224	2405	mV
V_{OL}	Output LOW voltage[3]	1355	1441	1605	1355	1438	1605	1355	1435	1605	mV

(1) Device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Output parameters vary 1:1 with V_{CC}
(3) All loading with 50Ω to V_{CC} –2.0V

AC CHARACTERISTICS [1](V_{CC} = 3.0 V to 3.6 V; GND = 0 V)[2]

CHARACTERISTIC		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Max switching frequency[3], see Figure 5		2.1			2.0			2.0		GHz
t_{PLH} / t_{PHL}	Propagation delay to differential output	230		550	230		550	230		550	ps
t_{SKEW}	Within device skew[4]		25	50		25	50		25	50	ps
	Device to device skew[5]		100	200		100	200		100	200	ps
t_{JITTER}	Random clock jitter (RMS)		0.2	0.8		0.2	0.8		0.2	0.8	ps
t_r / t_f	Output rise/fall times (20%–80%)	150		300	150		300	150		300	ps

(1) Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Measured using a 2.4 V source, 50% duty cycle clock source. All loading with 50 Ω to VCC – 2.0 V.
(3) Maximum switching frequency mearured at output amplitude of 300 mV_{pp}.
(4) Skew is measured between outputs under identical transitions and conditions on any one device.
(5) Device−to−Device Skew for identical transitions at identical VCC levels.

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Typical Termination for Output Driver

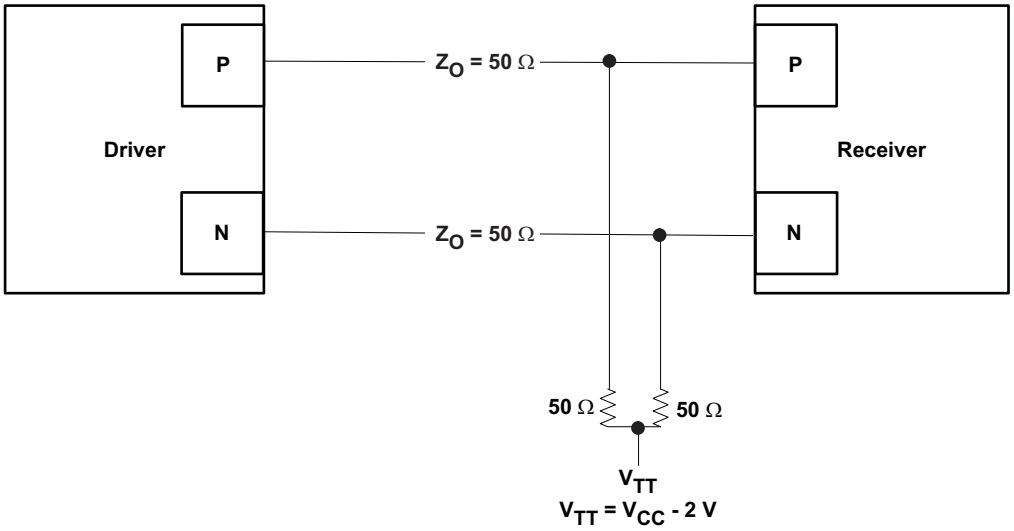


Figure 1. Termination for Output Driver

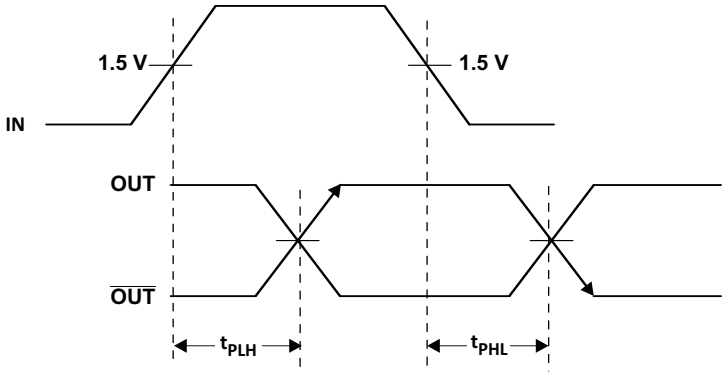


Figure 2. Output Propagation Delay

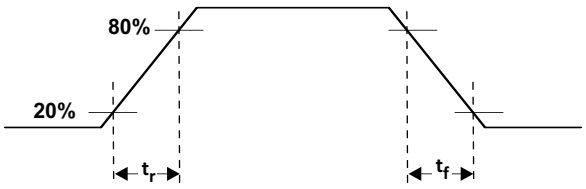


Figure 3. Output Rise and Fall Times

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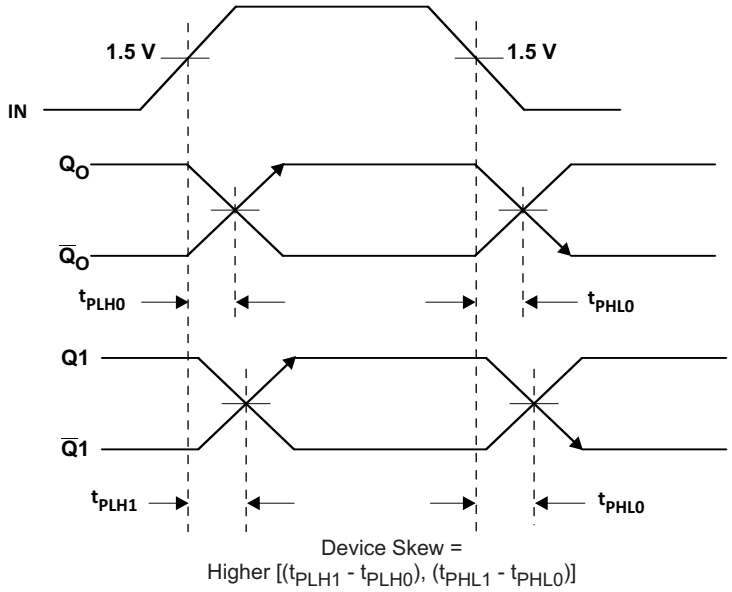


Figure 4. Device Skew

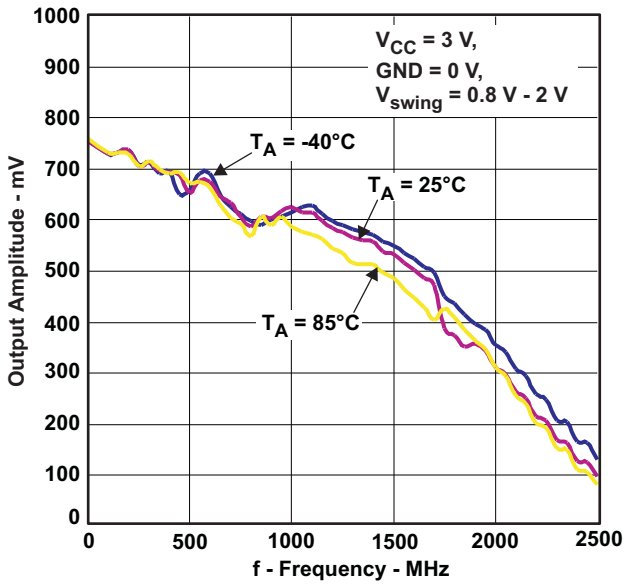
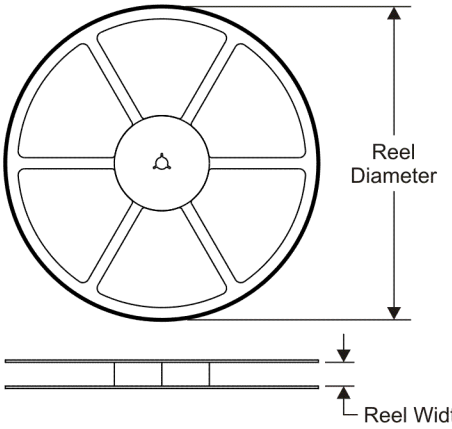


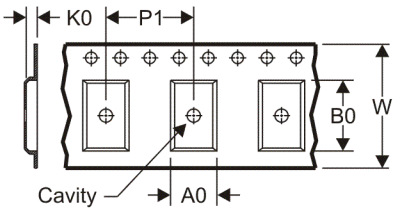
Figure 5. Output Amplitude versus Frequency

TAPE AND REEL INFORMATION

REEL DIMENSIONS

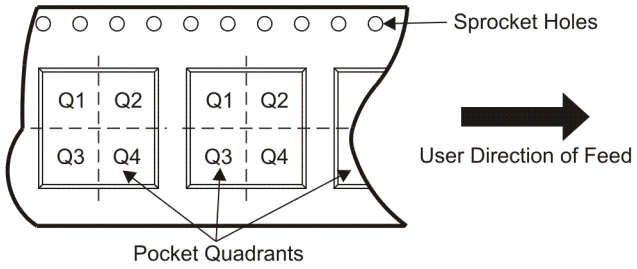


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

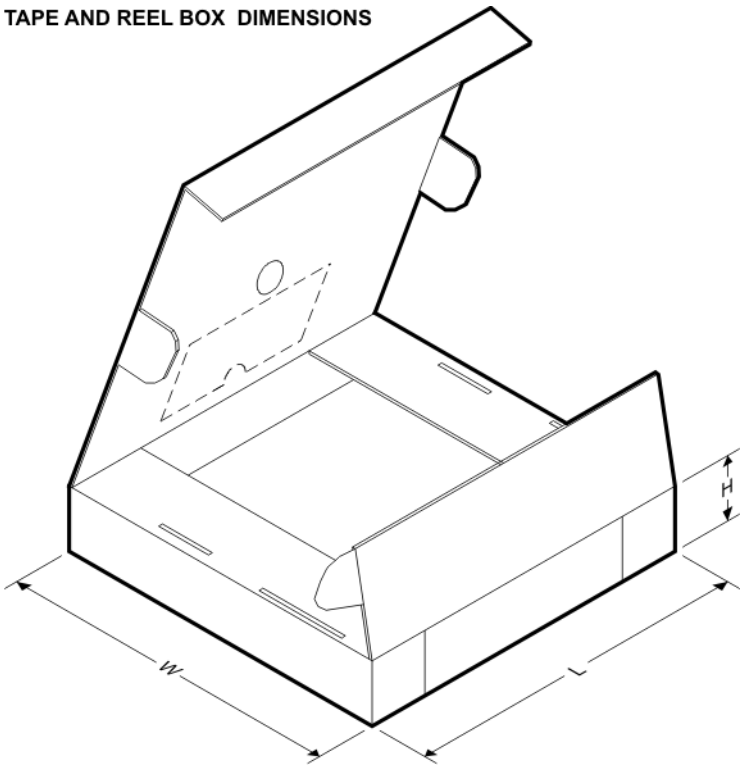
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65EPT22DGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65EPT22DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

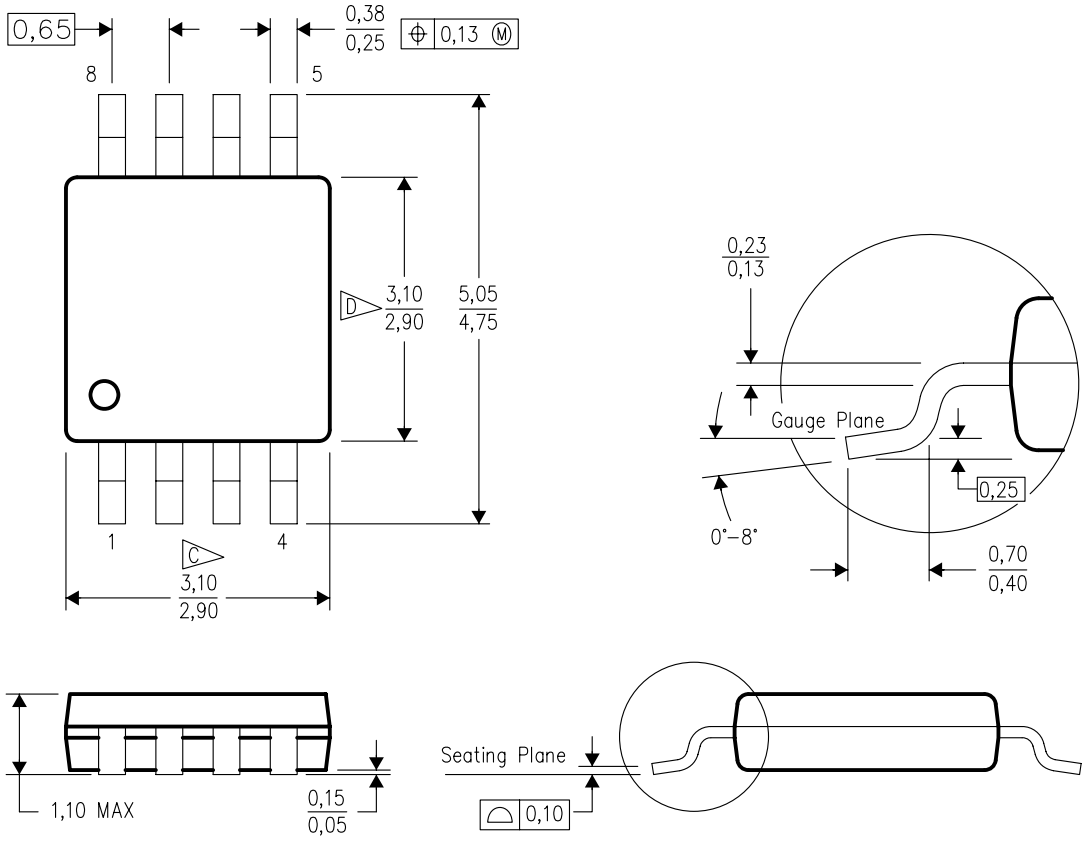
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65EPT22DGKR	MSOP	DGK	8	2500	346.0	346.0	29.0
SN65EPT22DR	SOIC	D	8	2500	346.0	346.0	29.0

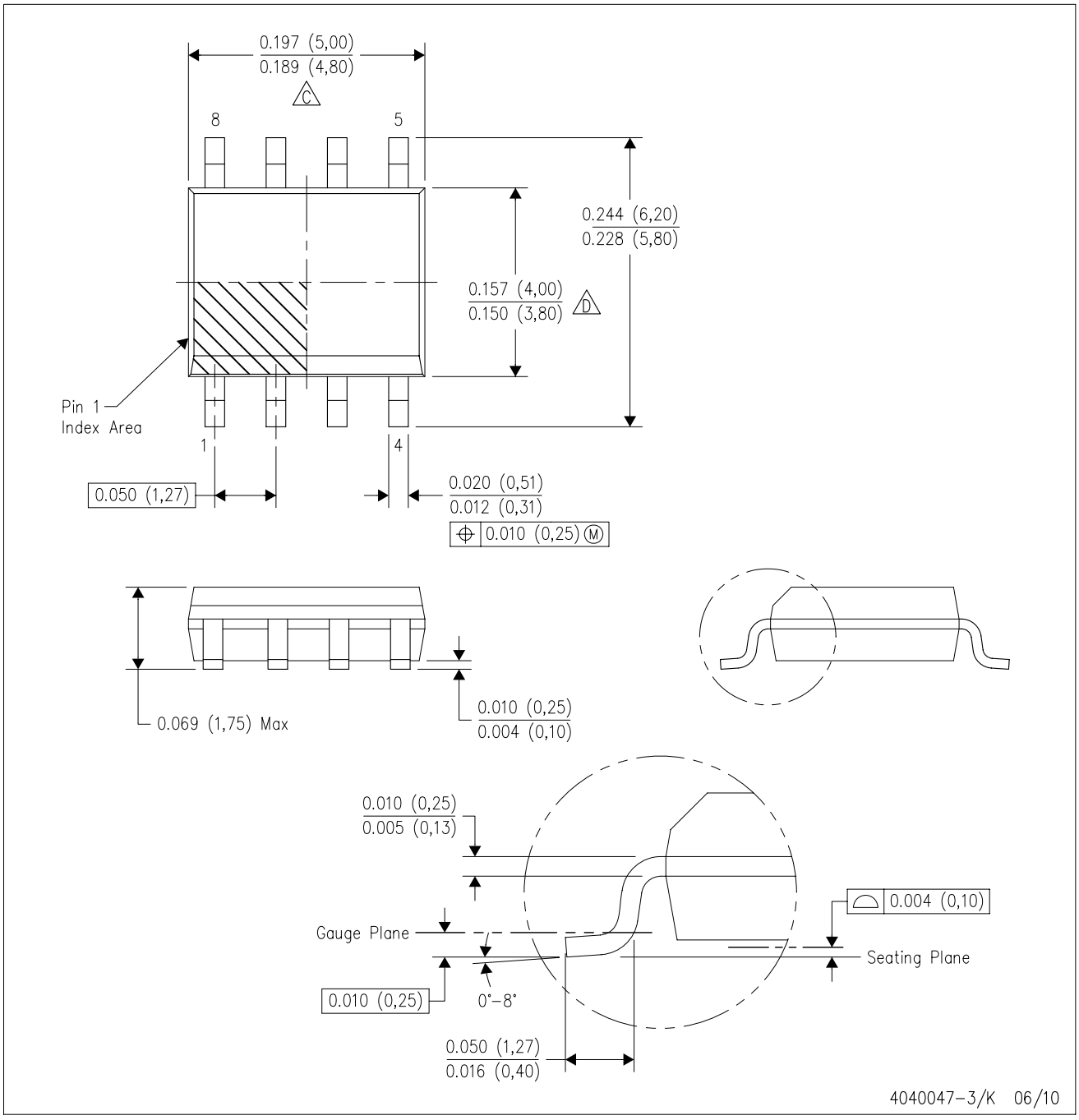
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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