NIKO-SEM

P-Channel Logic Level Enhancement Mode Field Effect Transistor

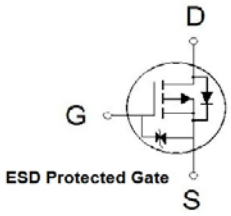
PZ0703EK

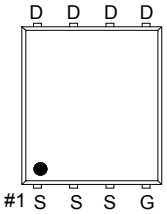
PDFN 5x6P

Halogen-Free & Lead-Free

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D[3]
-30V	7mΩ	-70A





1. GATE
2. DRAIN
3. SOURCE

RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current[3]	T_C = 25 °C	I_D	-70	A
	T_C = 100 °C		-56	
Pulsed Drain Current[1]		I_{DM}	-150	
Continuous Drain Current	T_A = 25 °C	I_D	-13	
	T_A = 70 °C		-10	
Avalanche Current		I_{AS}	-71	
Avalanche Energy	L = 0.1mH	E_{AS}	252	mJ
Power Dissipation	T_C = 25 °C	P_D	50	W
	T_C = 100 °C		32	
Power Dissipation	T_A = 25 °C	P_D	2.5	W
	T_A = 70 °C		1.6	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C
ESD Class	HBM		>3KV	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient	$R_{\theta JA}$		50	°C / W
Junction-to-Case	$R_{\theta JC}$		2.5	

[1]Pulse width limited by maximum junction temperature.
[2]The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.
[3]Package limitation current is -51A

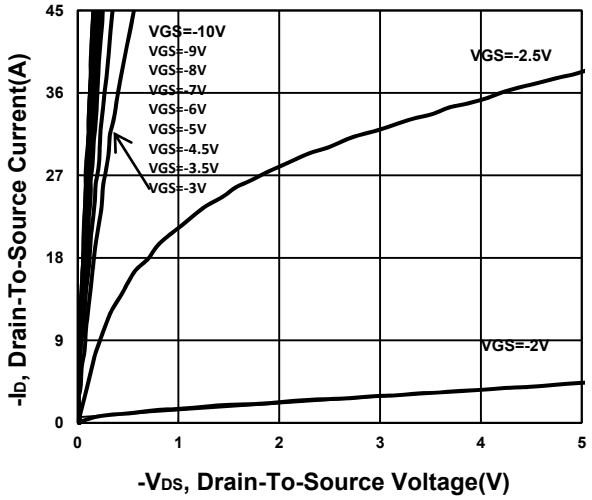
ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1	-1.4	-3	

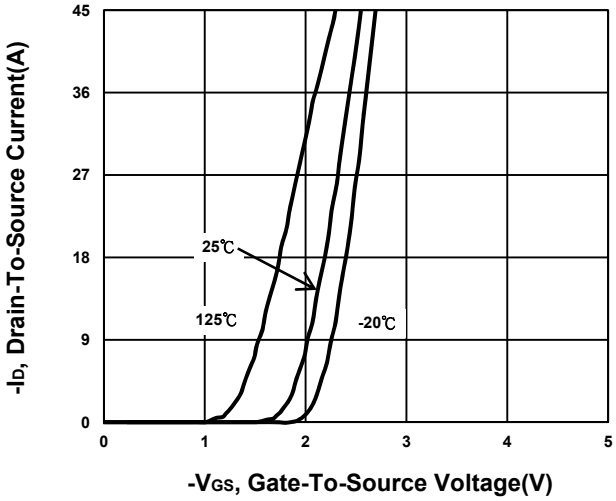
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±16V			±30	uA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V			-1	μA
		V_{DS} = -20V, V_{GS} = 0V, T_J = 125 °C			-10	
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -4.5V, I_D = -20A		5.7	10	mΩ
		V_{GS} = -10V, I_D = -20A		3.8	7	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -20A		65		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz		5210		pF
Output Capacitance	C_{oss}			960		
Reverse Transfer Capacitance	C_{rss}			890		
Total Gate Charge[2]	Q_g V_{GS}=10V	V_{DS} = -15V , V_{GS} = -10V, I_D = -20A		121		nC
	Q_g V_{GS}=4.5V			64		
Gate-Source Charge[2]	Q_{gs}			12		
Gate-Drain Charge[2]	Q_{gd}			27		
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DS} = -15V, $I_D \cong$ -20A, V_{GS} = -10V, R_{GS} = 6Ω		33		nS
Rise Time[2]	t_r			25		
Turn-Off Delay Time[2]	$t_{d(off)}$			100		
Fall Time[2]	t_f			45		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)						
Continuous Current[3]	I_S				-70	A
Forward Voltage[1]	V_{SD}	I_F = -20A, V_{GS} = 0V			-1.3	V
Reverse Recovery Time	t_{rr}	I_F = -20A, dI_F/dt = 100A / μS		26.5		nS
Reverse Recovery Charge	Q_{rr}			16		nC

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Package limitation current is -51A

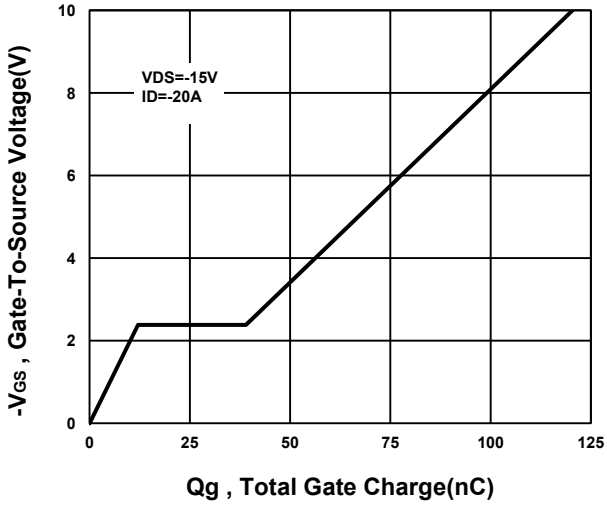
Output Characteristics



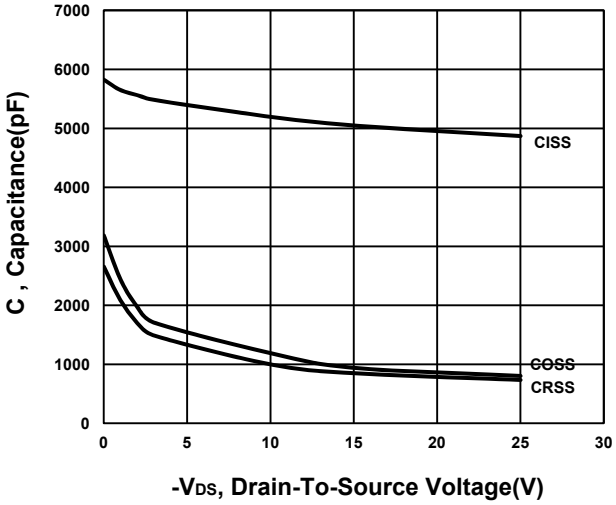
Transfer Characteristics



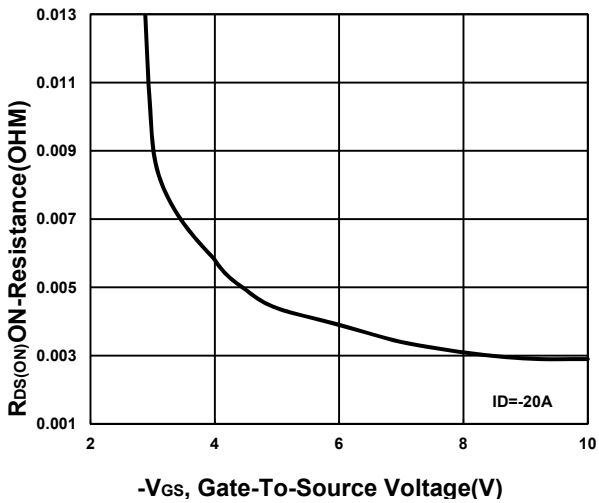
Gate charge Characteristics



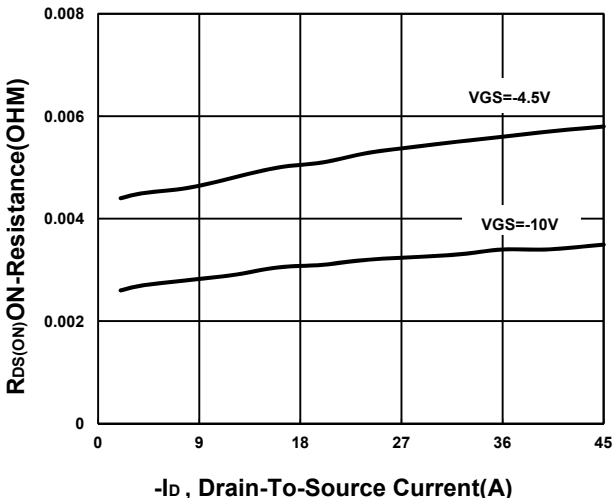
Capacitance Characteristic



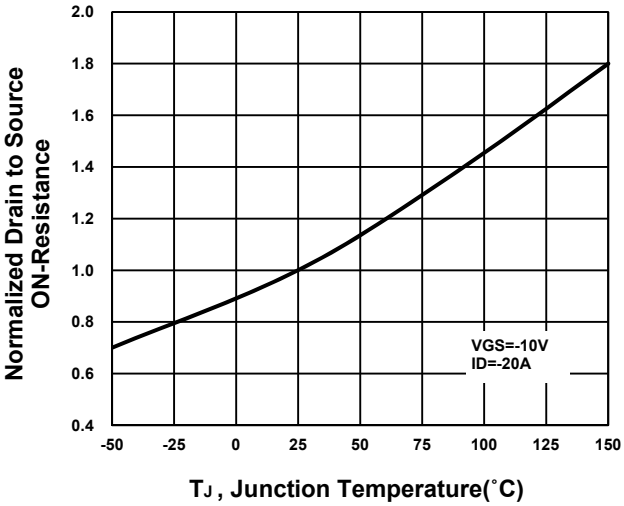
On-Resistance VS Gate-To-Source



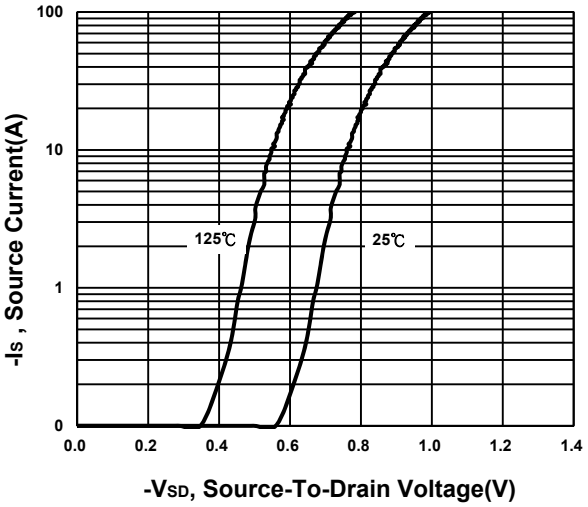
On-Resistance VS Drain Current



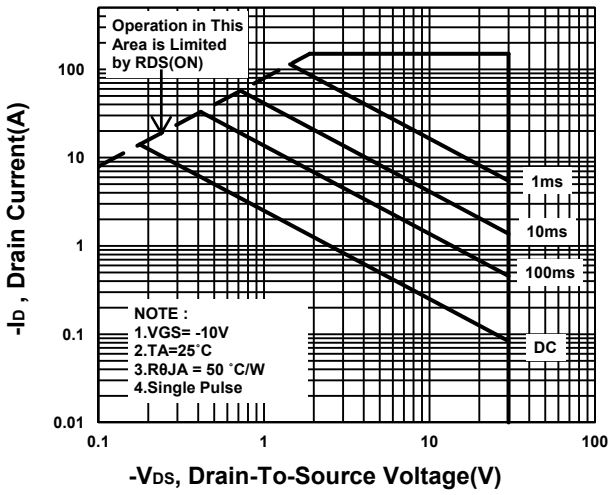
On-Resistance VS Temperature



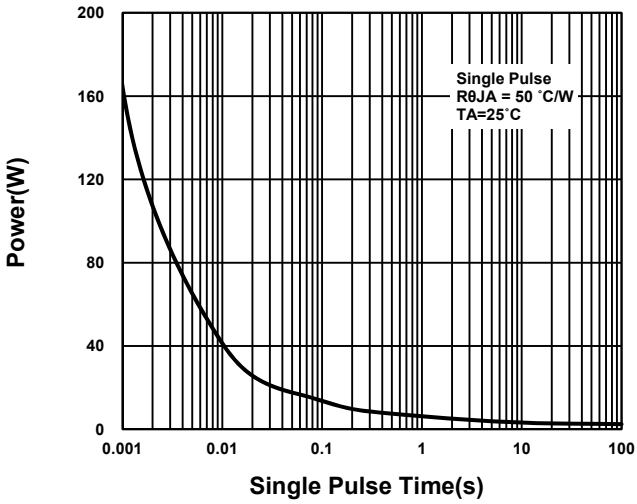
Source-Drain Diode Forward Voltage



Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve

