LM25066 Evaluation Board

National Semiconductor
Application Note 2100
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February 8, 2011

Introduction

The LM25066EVM evaluation board provides the design engineer with a fully functional intelligent monitoring and protection controller board designed for positive voltage systems. This application note describes the various functions of the board, how to test and evaluate it, and how to use the GUI design tool to change the components for a specific application. Use of the advanced telemetry and monitoring capabilities of this device requires the installation of the Intelligent Power Manager graphical user interface, however the LM25066 is capable of acting as a hot-swap and protection circuit without any software installation. Please check the LM25066 webpage for the latest software and datasheet information.

PCB Features

- Input voltage range: +2.9V to 16V (limited by input clamp)
- Programmable Current limit: 50 Amps or 90 Amps (±10%)
- Q1 Power limit: 80W (typical), 100W (worst case)
- UVLO Thresholds: 2.9V and 3.1V
- PGD Thresholds: 10.8V and 10.25V
- Insertion delay: 147 ms (typical)
- Fault time-out period: 8.9 ms
- Restart time: 1.1 seconds
- PCB Size: 3.5” x 3.5”
- Solution Size: 0.75” x 0.75”

Simplified Schematic

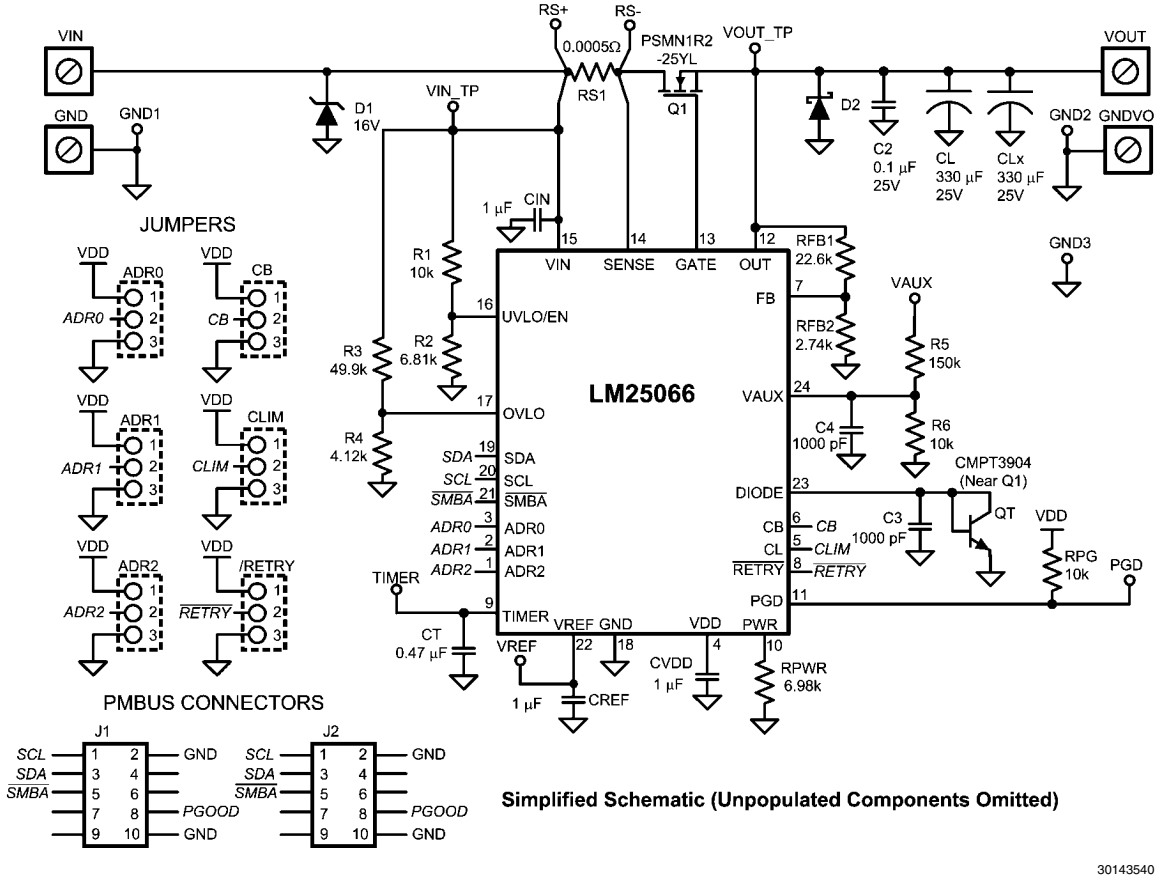

FIGURE 1. Simplified Evaluation Board Schematic

The simplified schematic for the LM25066 evaluation board is shown in *Figure 1*. Connections to the PMBus interface is provided by J1. Panduit terminal lugs bolt down to the PCB to provide input and output connection. Jumpers ADR0, ADR1, and ADR2 set the PMBus™ address of the device to one of 27 unique addresses. Jumpers also exist to set the device retry, circuit breaker, and current limit behavior. Test points are provided to connect to the input voltage, output voltage, VAUX, PGD, VREF and the TIMER pin.

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Getting Started

The LM25066 evaluation kit hardware is shown in *Figure 2*. The board offers two connections for the system input voltage and load. For evaluation at currents below 15A, the system voltage and load can be plugged directly into the female banana receptacles. For higher currents it is recommended to use the copper Panduit lugs with low gauge wire to minimize the cable power dissipation and voltage drops. Capacitors CL and CLx represent capacitance which is typically present on the input of the load circuit, and are present on this evaluation board so the turn-on characteristics of the LM25066 may be tested starting into a capacitive load. Footprints for components RSx and Q1x are not populated and are provided to accommodate evaluation of hot-swap designs greater than 50A.

The LM25066EVB is supplied with the PMBus address set to 16 Hex as dictated by the jumper configuration of the ADR0, ADR1, and ADR2 jumper connections.

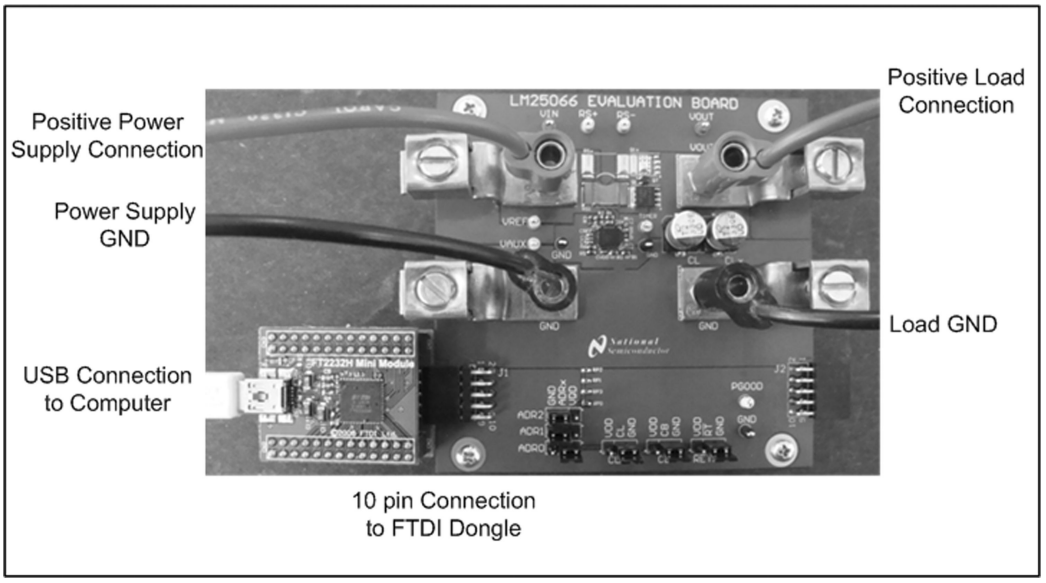

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FIGURE 2. Connection Illustration

The first step to evaluate the telemetry features of LM25066 demonstration is to install the GUI software. The software is included on a CD in the evaluation kit and is titled PMBManager-x.x.x-xxxxxxxx.exe, where the x characters indicate the software version and build date. This file should be executed on a PC running Windows XP or later to install the software. Once the GUI software is installed the hardware should be configured as shown in *Figure 2*

Hardware Setup Steps

1. Connect the input supply to either the VIN and GND banana plugs (IOUT<15A) or to the input terminal lugs (IOUT>15A).
2. Connect the load to the VOUT and GND banana plugs or terminal lugs.
3. Connect the FTDI Dongle to the 10 pin connector on the left side of the board.
4. Connect the supplied mini USB cable from the FTDI dongle to an USB port on a PC.

When the FTDI dongle is connected for the first time the user will be prompted to install the device drivers. For the most current driver installation procedure refer to the README.TXT file in the installation directory.

For a hot swap circuit to function reliably, a low inductance connection to the input supply is recommended. Its purpose is to minimize voltage transients which occur when the load current changes or is shut off. If not careful, wiring inductance in the supply lines will generate a voltage transient at shutoff which can exceed the absolute maximum rating of the LM25066, resulting in its destruction. To protect against such voltage transients D1 is provided to clamp the voltage at the input to within safe operating limits. Likewise D2 is provided on the output to clamp the output from going too negative during short circuit events.

Device Evaluation

After configuring the hardware connections, apply an input voltage of 12V to the device. The current hardware configuration allows the LM25066 device to work with 3.3V, 5.0V, and 12V system rails; however, this getting started guide will assume an input voltage of 12V. Double click on the GUI executable in the installation folder from the previous installation step. The device should be detected on the PMBus and the initial load screen should appear as shown in *Figure 3*.

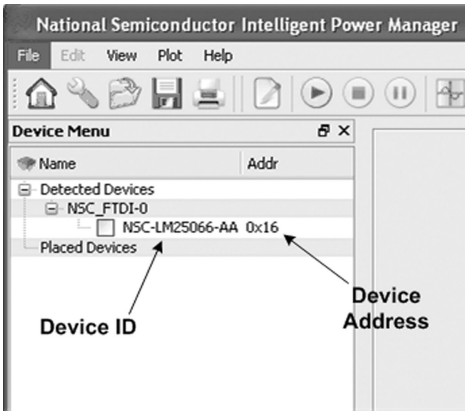

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FIGURE 3. Initial GUI Screen

If no device is detected you will have the option to rescan, ignore, or exit the GUI. If you intend to have the hardware connected check the USB connection to the PCB, FTDI connection to the evaluation module and verify that the power is present on the evaluation PCB by measuring the voltage between the GND and VIN testpoints. Ignoring the detection message allows use of the integrated design tool without the hardware connected.

Double click on the detected device ID (NSC-LM25066-AA) to display a block level representation of the device as shown in *Figure 4*. The block level view of the device provides a display of all the telemetry data, as well as most of the faults and warnings supported by the device. The faults and warnings supported by the device are generally associated with an invalid input or output condition.

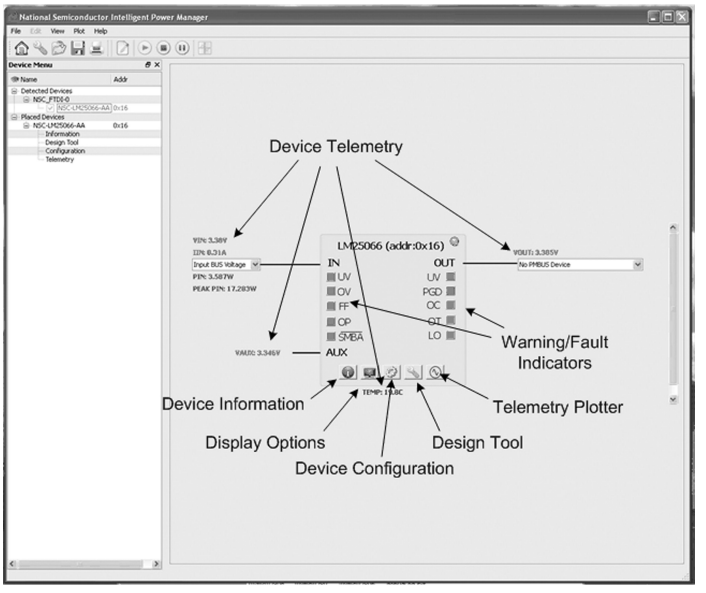

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FIGURE 4. LM25066 Block Level Representation

The faults shown on the left side of the block representation are generally associated with the input. These include input under voltage (UV), input over voltage (OV), Fet Fail (FF), input over power (OP). The SMBus alert status (SMBA) is also shown on the left side and will turn red during any warning or fault event. To facilitate the evaluation of the device, SMBus alerts are automatically cleared by the GUI.

The faults shown on the right side of the block representation are associated with the output. These include output over voltage (OV), power good status (PGD), output over current (OC), and over temperature (OT). There is also an indicator if the output is in the latched off state (LO). The device will latch the output off after the number of user programmable retries are exceeded. To clear the latched off condition the output can be toggled off and on by the red power button icon located in the top right of the LM25066 block representation.

To show a repetitive update of the device telemetry and status click on the play icon at the top of the screen. The play button starts an active telemetry log of the gathered data. Clicking the stop icon stops the telemetry collection and allows for the

log file to be viewed and saved. The pause button pauses both the displaying and logging of telemetry information.

To disable displaying undesired telemetry click the display icon on the block representation. This will open the window shown in *Figure 5* that will allow the user to disable the undesired telemetry, fault, and warning information from appearing on the block level device representation.

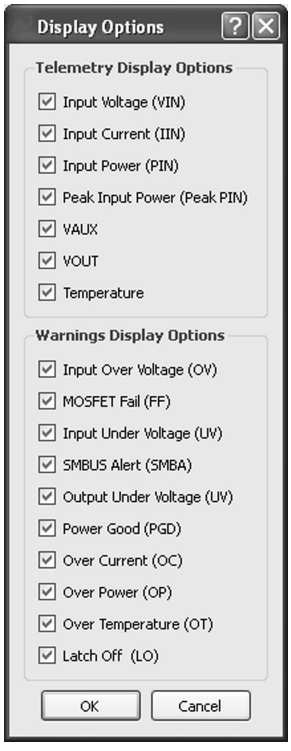

FIGURE 5. LM25066 Telemetry Display Options

Note that turning off the various warning options does not mask the faults from issuing an SMBus alert, it just does not display them if they occur. The device is capable of masking various faults, and this functionality can be setup in the device configuration panel.

GUI Event Log

A GUI event log is provided to keep track of GUI configuration changes and device fault events. To display the event log select View from the main menu bar and then View Event Log. The event log will appear in the bottom right of the main GUI window. The event log can be detached and expanded if desired by left clicking on the event log window and dragging window with the mouse to the desired location.

Plotting Telemetry Data

To enable telemetry data plots click on the sine wave icon located on the LM25066 block representation. After enabling the telemetry, a prompt will appear requesting entry of the GUI sample rate, plot rate, and plot depth. For most cases the default rates and depths will be acceptable. The plotting tool allows the user to select the desired data to be plotted. Up to 2 different parameters may be plotted at the same time as shown in *Figure 6*.

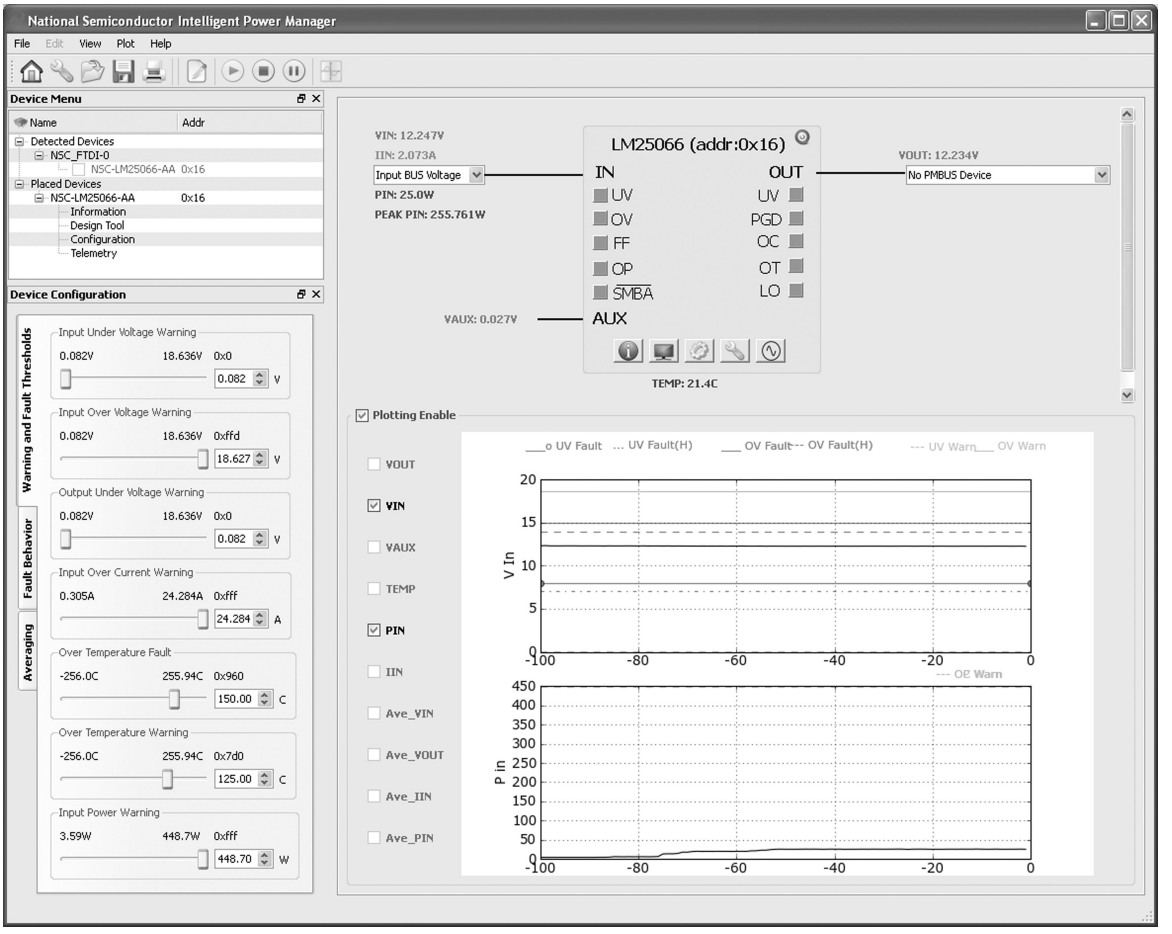

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FIGURE 6. LM25066 GUI with Telemetry Plotting Tool Enabled

Device telemetry data is plotted as a black line that continually updates as the device is queried. In addition to the device data the relevant warning and fault threshold are also plotted. Warning thresholds are shown as orange lines while fault threshold are shown in red.

By going to the plot menu option the user can disable the plotting grid, as well as the warning and fault lines.

Configuring the LM25066 Device

Warning Thresholds, Temperature Fault Threshold, Protection Ranges, Fault Masking, and Averaging can be configured in the Device Configuration panel. This panel, shown in *Figure 7*, is enabled by clicking the gear icon shown on the LM25066 block representation.

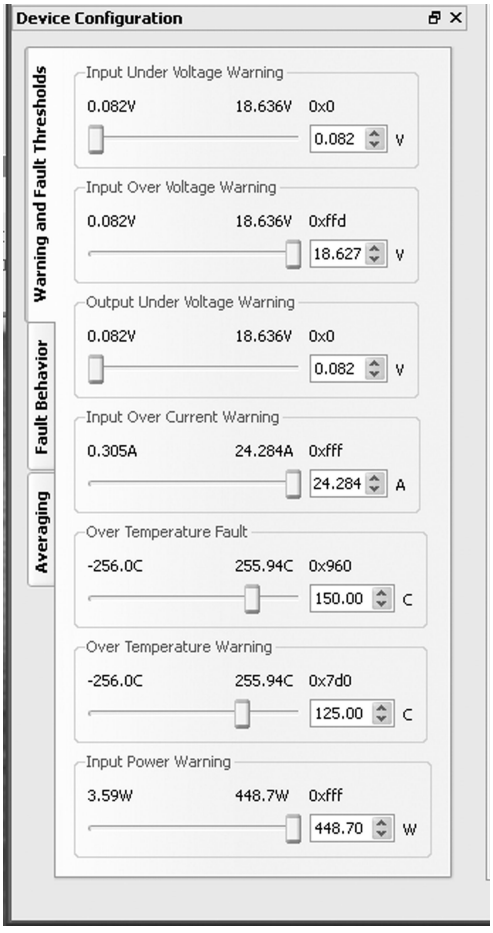

FIGURE 7. Device Configuration Panel

The Warning and Fault Threshold tab allows configuration of the input under voltage, input over voltage, output under voltage, input over current, input power, and over temperature warnings. This tab also allows adjustment of the over temperature fault threshold. Fault threshold for the input over and under voltage, current limit, power limit, and power good are set by the hardware design. Decimal values for the thresholds are shown in the text box located to the right of the slider bar. Above the decimal values setting is the value of the setting in hexadecimal; which can be useful when developing software for this device.

The fault behavior tab allows the user to set the device fault configuration and fault masking. The fault configuration section allows the user to set the number of retries, as well as the circuit breaker and current limit thresholds. The number of retries can be set by the /Retry pin to be infinite or latched off. Through software the number of retries can be set to 0 (latch-off), 1, 2, 4, 8, 16 or infinite. The software settings are independent of the hardware settings; however, if the power is cycled the device will default to values dictated by the hardware. Circuit breaker and current limit power-up values are also set by the hardware. The values for current limit can be set to either 25 mV (CL = GND) or 46 mV(CL = VDD). The circuit breaker threshold can also be set to either 1.8 x (CB = GND) or 3.6 x (CB = VDD) the current limit value. Fault masking is possible for many of the device fault conditions. Fault conditions allow masking of both the MOSFET response and the SMBus alert signal. Note that if a fault occurs repeatedly while the MOSFET is masked, damage to the MOSFET may result. This feature is allowed primarily for debug purposes. Faults that only issue a SMBus alert allow masking of the alert. Note the power up default setting for the Power Good signal is to mask the SMBus alert.

For convenience, the Device Configuration Panel can be undocked by holding down the left mouse button while the cursor is at the top of the panel, and dragging it to where you would like it to be placed.

Customizing the Design

The GUI assumes the hardware configuration is set to default evaluation board configuration. If any of the components are changed, the device hardware configuration needs to be updated in the design tool section. To open the design tool click the wrench icon located on the LM25066 block representation which will open the window displayed in *Figure 8*.

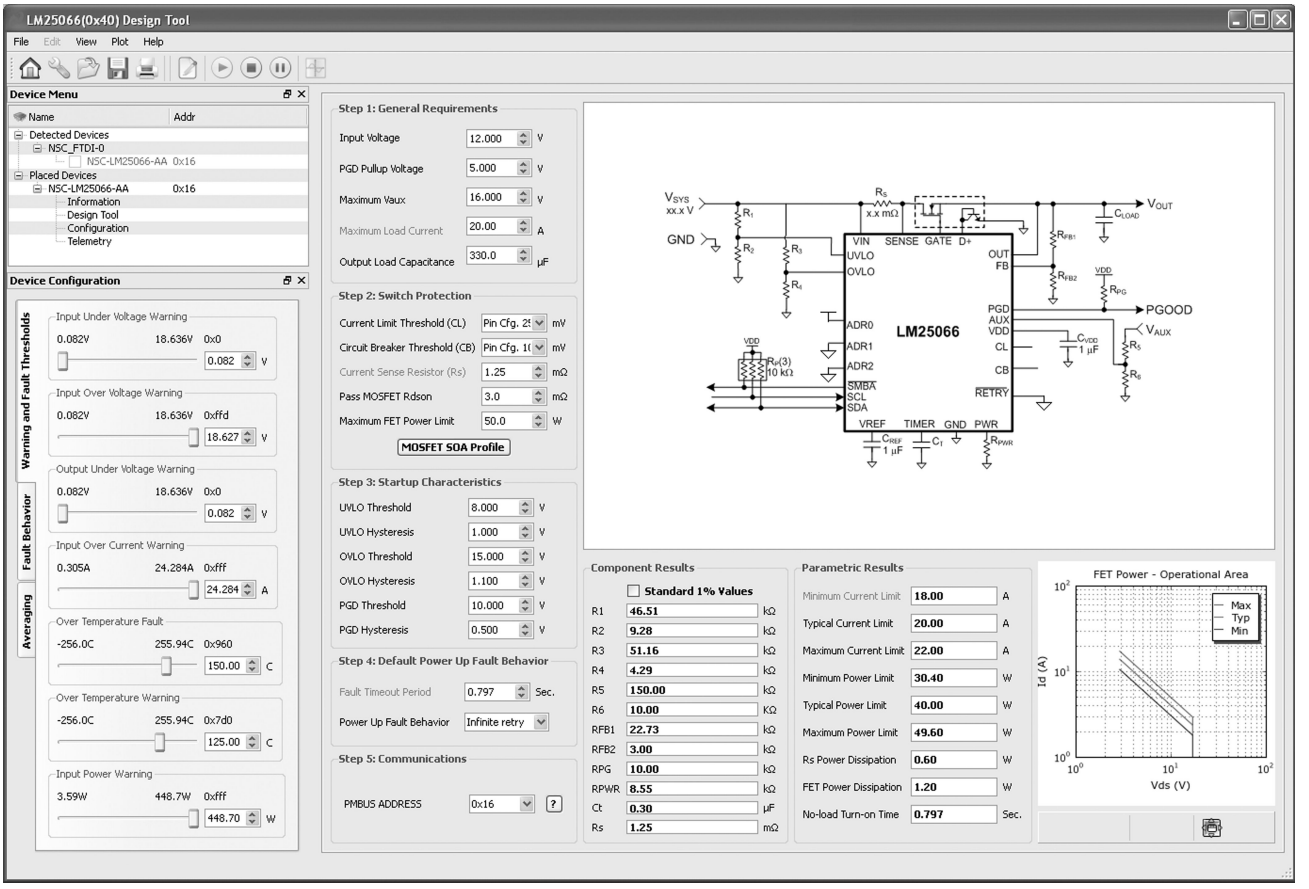

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FIGURE 8. LM25066 Design Tool

Design inputs are keyed in on the left side following steps 1 though 5. General operating conditions should be entered in step 1 of the design tool. These inputs help set bounds on the startup time and application voltage ranges.

Step 2 allows the user to tailor the MOSFET protection features to be specific to the target application. Both pin and software configurable ranges are available for the circuit breaker and current limit circuits. If a pin configuration is selected please make sure the CB and CL jumpers are set to match the GUI selection. By clicking on the MOSFET SOA Profile button the user can select SOA data from several popular MOSFETs or enter in the SOA data for the desired MOSFET.

Step 3 allows the user to select the under and over voltage lockout values (UVLO/OVLO), and power good (PGD) thresholds. Note that with the correct values for R1 - R4, and RFB1 and RFB2 installed, the device will indicate a fault condition when the input and/or output voltages are outside of their programmed range.

Step 4 allows the user to set the fault time-out period and the fault response. The fault time-out should be set to be below the MOSFET SOA data for a given time. For example, if a design is done to adhere to the 10 ms pulsed MOSFET SOA data, the desired fault time-out must be less than 10ms. The fault time-out time entered will set the value for CT. It also sets the insertion delay and fault retry delay. The initial power up retry behavior is also selected in this design step. Make sure to change the /Retry jumper to match the design tool schematic when changing the default retry setting.

In Step 5 the user enters the desired PMBus address. Note changing the PMBus address of the device in step 5 does not change the device address, but shows how the address pins of the device need to be configured to achieve a desired address. Once the ADR pin jumpers are configured for a particular address, power to the device needs to be cycled and the GUI restarted in order for the new address to take affect.

When invalid or incorrect inputs are given to the design tool, text associated with the faulty input will turn red. Positioning the mouse cursor over the red text will give additional information about any design conflict.

Component and parametric results are shown to the right, as well as the LM25066 protection SOA chart. The protection SOA chart shows the minimum, typical, and maximum SOA protection areas for a given design. For a robust design the SOA of the MOSFET used should be above the MAX protection SOA line for all operating areas. To help make this determination, step 2 allows the user to select the SOA curves

for several popular MOSFETs or to input in the SOA data for the desired MOSFET.

Once a design is complete the design should be saved by selecting the File menu, and then Save. Once the hardware is modified to match the design the GUI should be restarted and the hardware configuration file loaded right after the device is detected and placed. If the values in the design tool are different than the values on the board, erroneous telemetry and fault data will be reported by the GUI. To return to the block view of the device press the home icon located at the far left in the menu bar.

The design tool is also useful to calculate the PMBus coefficients. With the correct value for current sense resistor (RS1) the tool will calculate the correct coefficients to scale the raw telemetry data. The coefficients can be viewed by selecting View from the main menu bar, and then selecting the PMBus Coefficient Editor. When the PMBus Coefficient Editor is opened, press the Get All button to show the currently used coefficients.

If desired the equations used in the design tool can be calculated by hand using the equations provided in the datasheet. However, note the design tool calculates parameters factoring in worst case tolerances, while the equations in the datasheet based on typical thresholds.

Theory of Operation

The LM25066 provides intelligent control of the power supply connections of a load which is to be connected to a live power source. The three primary functions of the device is to limit in-rush current during turn-on, monitor the load current for faults during normal operation, and to provide system telemetry for the following parameters: Input Voltage (VIN), Input Current (IIN), Input Power (PIN), Output Voltage (VOUT), Auxilliary Voltage (VAUX), and Temperature. Additional functions include Under and Over-Voltage Lock-Outs (UVLO/OVLO) to ensure voltage is supplied to the load only when the system input voltage is within a specified range, power limiting of the series pass MOSFET (Q1) during turn-on, and a Power Good logic output (PGD) to indicate the output voltage status.

Upon applying the input voltage to the LM25066, Q1 is initially held off for the insertion delay (≅147 ms) to allow ringing and transients on the input to subside. At the end of the insertion delay, if the input voltage at VIN is above the UVLO threshold, Q1 is turned on in a controlled manner to limit the in-rush current. If the in-rush current were not limited during turn-on, the current would be high as the load capacitor (CL) charges up, limited only by the surge current capability of the voltage source, CIN's characteristics, and the wiring resistance (a few milliohms). That very high current could damage the edge connector, PC board traces, and possibly the load capacitors receiving the high current. Additionally, the dV/dt at the load's input is controlled to reduce possible EMI problems.

The LM25066 limits in-rush current to a safe level using a two step process. In the first portion of the turn-on cycle, when the voltage differential across Q1 is highest, Q1's power dissipation is limited to a peak value set by RPWR(80W) by monitoring its drain current (the voltage across RS1) and its drain-to-source voltage. Their product is maintained constant by controlling the drain current as the drain-to-source voltage decreases (as the output voltage increases). This is shown in the constant power portion of *Figure 9* where the drain current is increasing to I_{LIM}. When the drain current reaches the current limit threshold (50 Amps), it is then maintained constant as the output voltage continues to increase. When the output voltage reaches the input voltage (V_{DS} decreases to near zero), the drain current then reduces to a value determined by the load. Q1's gate-to-source voltage then increases to its final value. The circuit is now in normal operation mode.

Monitoring of the load current for faults during normal operation is accomplished using the current limit circuit described above. If the load current increases to 50 Amps (25 mV across RS1), Q1's gate is controlled to prevent the current from increasing further. When current limiting takes effect, the fault timer limits the duration of the fault. At the end of the fault timeout period Q1 is shut off, denying current to the load. The LM25066 then initiates a restart every 1.25 seconds. The restart consists of turning on Q1 and monitoring the load current to determine if the fault is still present. After the fault is removed, the circuit powers up to normal operation at the next restart.

In a sudden overload condition (e.g., the output is shorted to ground), it is possible the current could increase faster than the response time of the current limit circuit. In this case, the circuit breaker sensor shuts off Q1's gate rapidly when the voltage across RS reaches ≅90 mV. When the current reduces to the current limit threshold, the current limit circuitry then takes over.

The PGD logic level output is low during turn-on, and switches high when the output voltage at OUT is above 10.8V. PGD switches low when the voltage at OUT is below 10.25V. The high level voltage at PGD can be any appropriate voltage up to +17V, and can be higher or lower than the voltages at VIN and OUT.

The UVLO thresholds are set by resistors R1 and R2, the OVLO thresholds are set by R3 and R4, and the PGD thresholds are set by resistors RFB1 and RFB2. Internal current sources at the UVLO, OVLO, and FB pins provide hysteresis for the thresholds.

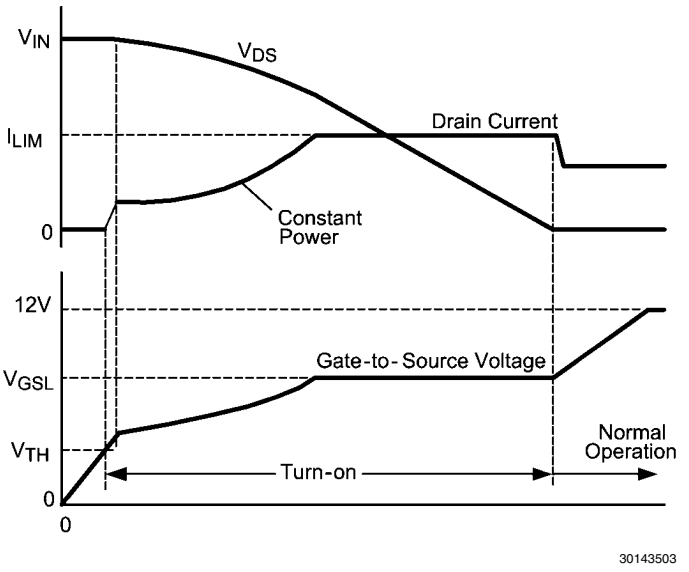


FIGURE 9. Power Up Using Power Limit and Current Limit

Fault Detection & Restart

If the load current increases to the fault level (the current limit threshold, 50A), an internal current source charges the timing capacitor at the TIMER pin. When the voltage at the TIMER pin reaches 1.7V, the fault time-out period is complete, and the LM25066 shuts off Q1. The restart sequence then begins, consisting of seven cycles at the TIMER pin between 1.7V and 1V, as shown in *Figure 10*. When the voltage at the TIMER pin reaches 0.3V during the eighth high-to-low ramp, Q1 is turned on. If the fault is still present, the fault time-out period and the restart sequence repeat.

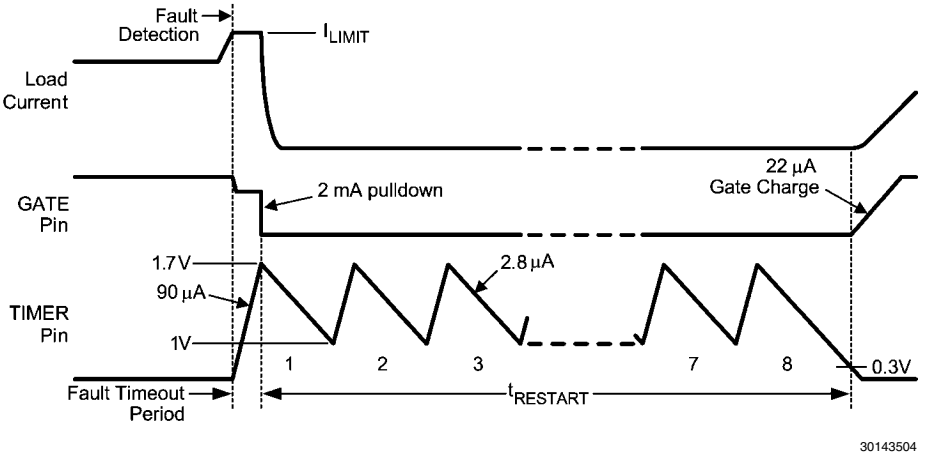


FIGURE 10. Fault Time-out and Restart Sequence

The waveform at the TIMER pin can be monitored at the TIMER test point. On this evaluation board the initial fault time-out period is 8.9 ms, and the restart time is 1.1 seconds. See Figure 18.

UVLO and OVLO Input Voltage Threshold

Programming the UVLO thresholds sets the minimum system voltage to enable the series pass device (Q1). If VIN is below the UVLO thresholds, Q1 is switched off, denying power to the load. Programmable hysteresis is adjustable by changing the value of R1.

The UVLO thresholds are set with two resistors (R1, R2) as shown in *Figure 11* .

The OVLO threshold sets the maximum voltage that can be present on the input before the device turns off the series pass device. The OVLO threshold is set with the two resistors (R3, R4). The hysterisis voltage is set by the internal 23uA current source and the value of R3.

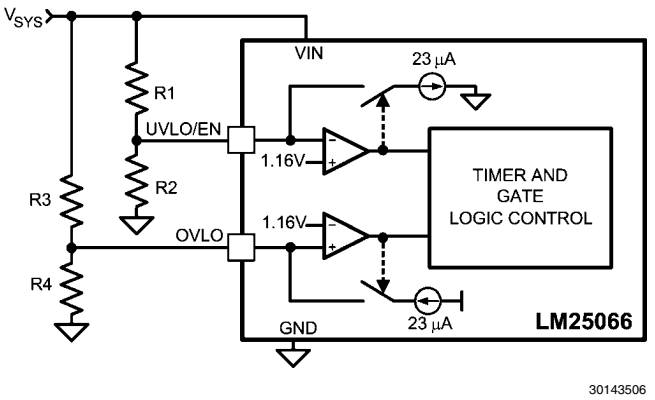


FIGURE 11. Programming the UVLO Threshold

POWER GOOD and FB Pins

During turn-on, the Power Good pin (PGD) will not be able to pull low until the voltage at VIN increases above ≅1.6V. Pulling the PGD pin up to VDD will keep the PGD pin low during this region because VDD does not turn on until VIN increases above ≅2.5V. When the voltage at the board's output pin increases above 10.8V(typ) PGD switches high. PGD switches low when the output voltage decreases below 10.25V(typ). Additionally, PGD switches low if the UVLO/EN pin is taken below its threshold regardless of the output voltage.

The output voltage threshold for the PGD pin is set with two resistors (RFB1, RFB2) at the FB pin.

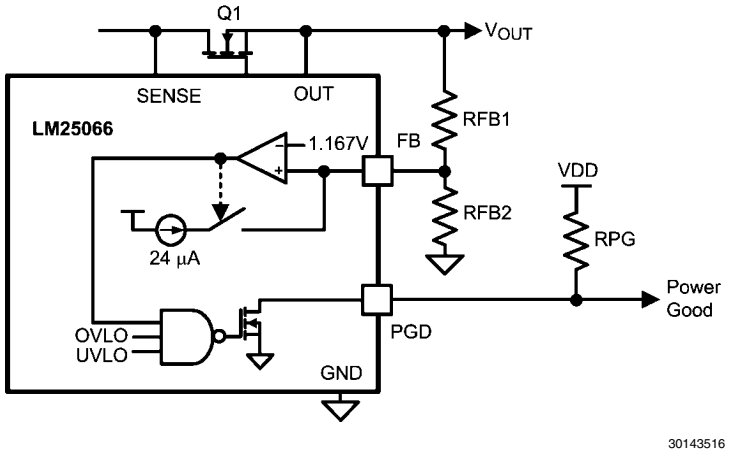


FIGURE 12. Programming the PGD Threshold

A pull-up voltage and pull-up resistor are required at PGD as shown in *Figure 12*. The pull-up voltage (VPGD) can be as high as 17V, with transient capability to 20V, and can be higher or lower than the voltages at VIN and OUT.

Shutdown

With the circuit in normal operation, the LM25066 can be shutdown by grounding the UVLO/EN pin or by clicking the ON/OFF button on the LM25066 block representation.

Board Layout and Probing Cautions

Refer to the product datasheet for detailed layout guidelines. For most applications the layout of this evaluation module as detailed in the PC Board Layout section of this document should be sufficient to provide a working solution with accurate telemetry. The following should be kept in mind when the board is powered:

1. Use CAUTION when probing the circuit to prevent injury, as well as possible damage to the circuit.
2. At maximum load current (50A), the wire size and length used to connect the power source and the load become very important. The wires connecting this evaluation board to the power source SHOULD BE TWISTED TOGETHER to minimize inductance in those leads. The same applies for the wires connecting this board to the load. This recommendation is made in order to minimize high voltage transients from occurring when the load current is shut off.

Performance Characteristics

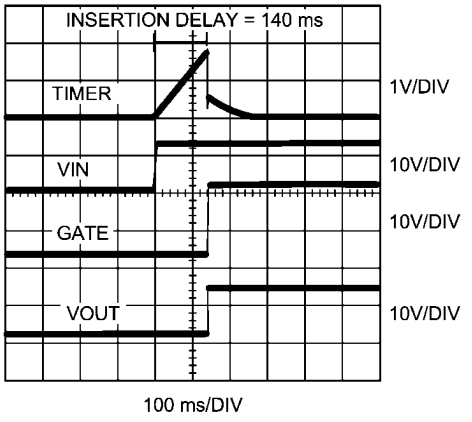


FIGURE 13. Insertion Time Delay

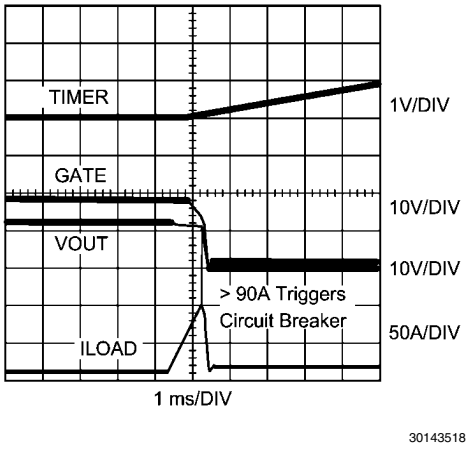


FIGURE 14. Circuit Breaker Response

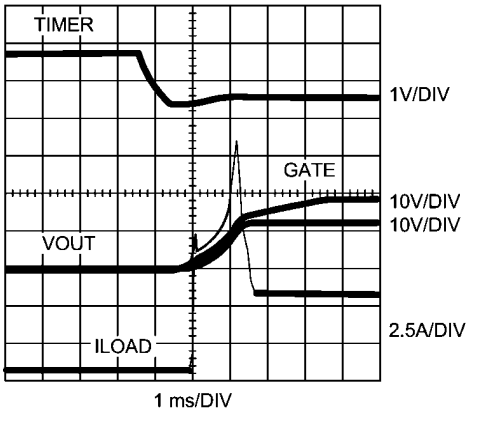


FIGURE 15. Turn-On Sequence into a 4Ω Load

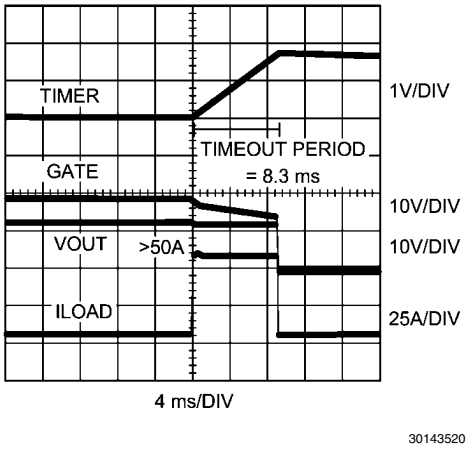


FIGURE 16. Initial Fault Timeout

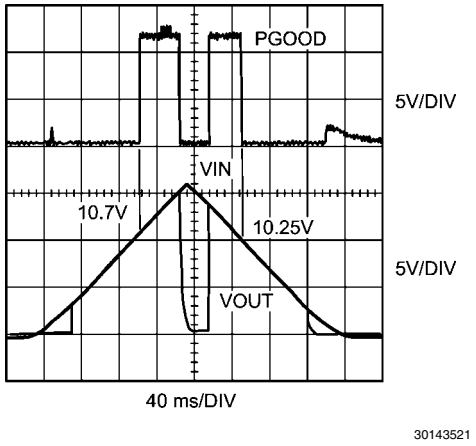


FIGURE 17. PGD Power up/Power down behavior

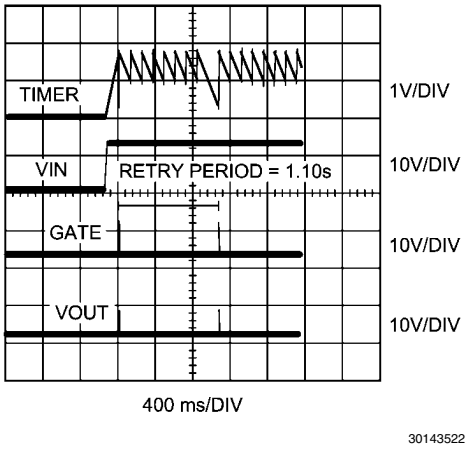


FIGURE 18. Restart Timing

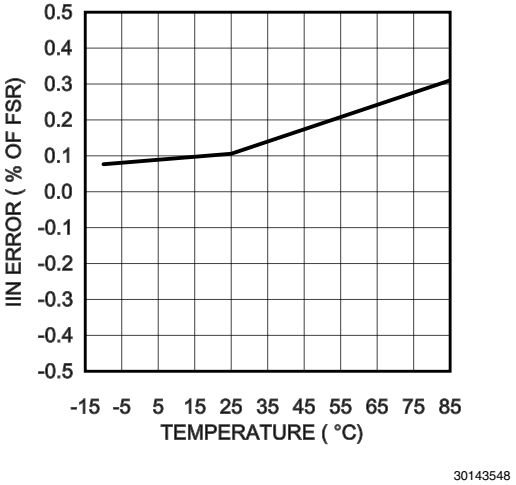


FIGURE 19. IIN Error vs Temperature

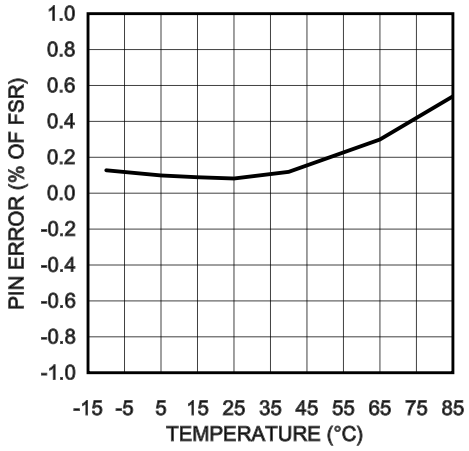


FIGURE 20. PIN Error vs Temperature

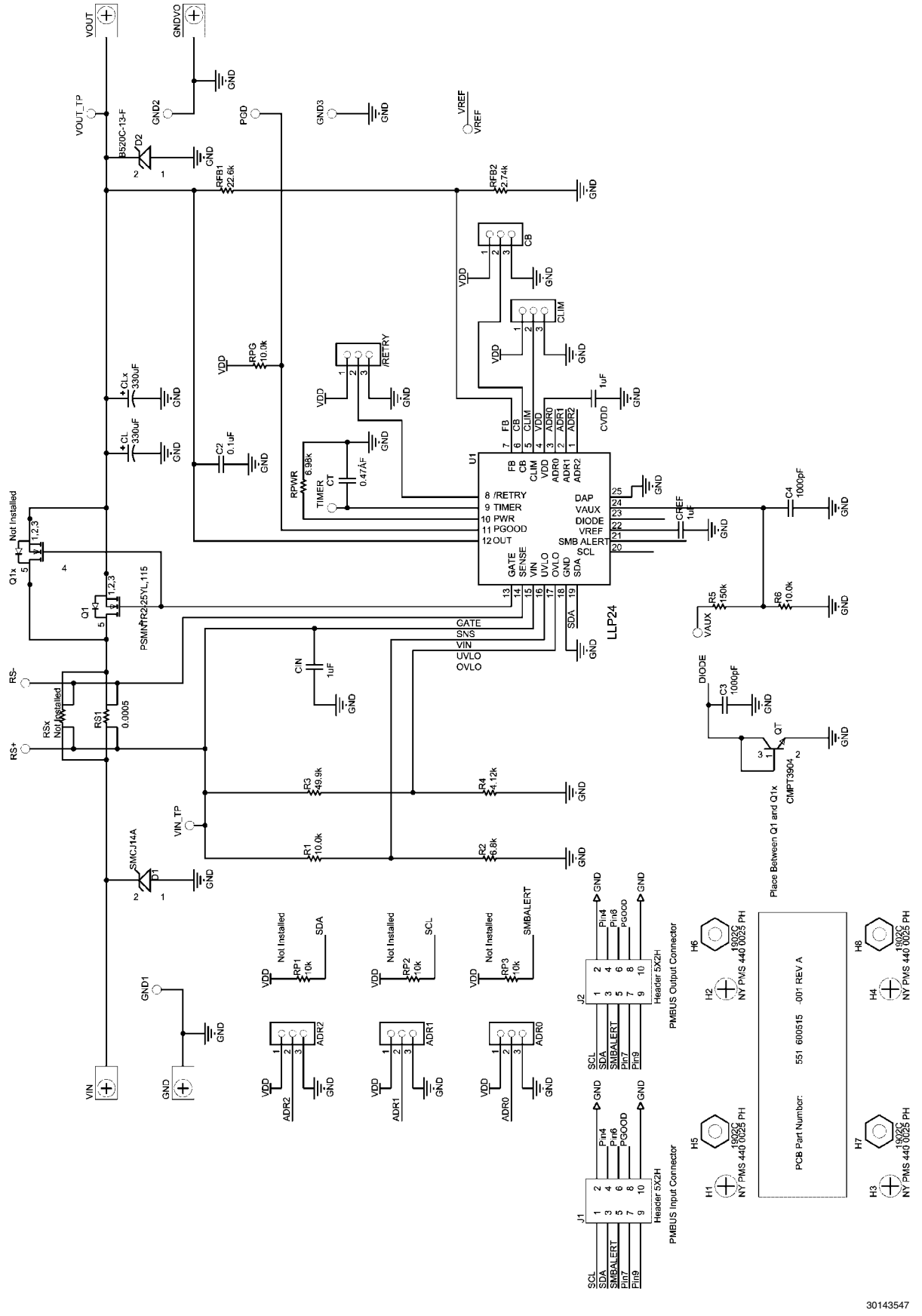
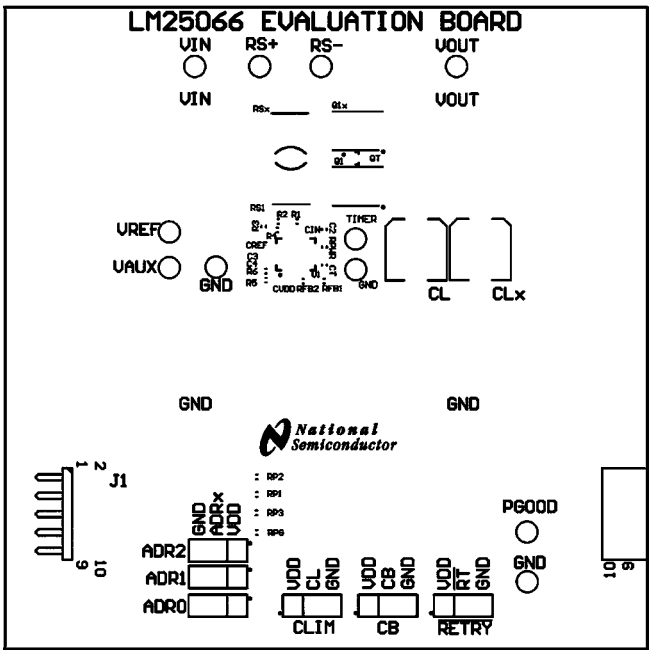


FIGURE 21. Evaluation Board Schematic

Bill of Materials

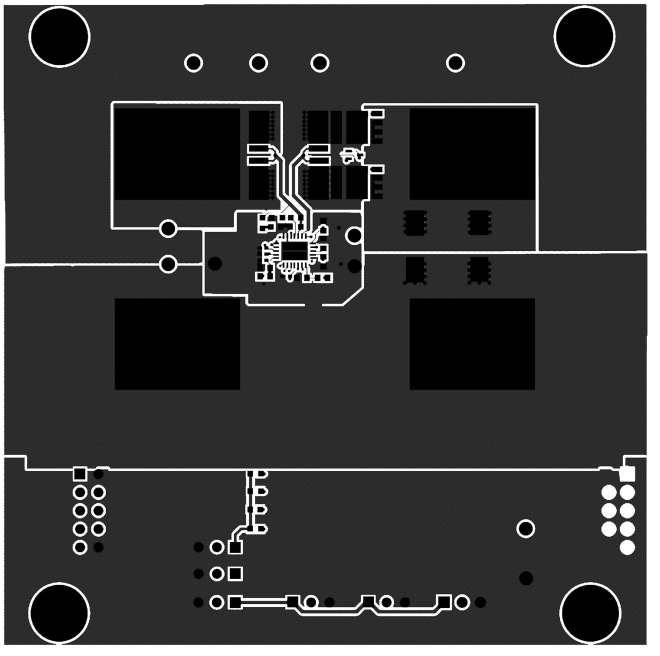
Designator	Value	Description	Manufacturer	Part Number	Qty.
/RETRY, ADR0, ADR1, ADR2	1x3	Header, TH, 100mil, 1x3, Gold plated, 230 mil above insulator	Samtec Inc.	TSW-103-07-G-S	4
J1, J2	5x2	Header, 5-Pin, Dual row, Right Angle, Printed Circuit Board			3
C2	0.1uF	Ceramic, X7R, 50V, 10%	MuRata	GRM188R71H104KA93D	1
C3, C4	1000pF	Ceramic, X8R, 50V, 10%	TDK	C1005X8R1H102K	2
CB, CLIM	1x3	Header, TH, 100mil, 1x3, Tin plated, 230 mil above insulator	Samtec Inc.	TSW-103-07-T-S	2
CIN	1uF	Ceramic, X7R, 50V, 10%	MuRata	GRM21BR71H105KA12L	1
CL, CLx	330uF	AL, 25V, 20%, 0.17 Ohm ESR	Nichicon	UUD1E331MNL1GS	2
CREF, CVDD	1uF	Ceramic, X5R, 6.3V, 20%	TDK	C1005X5R0J105M	2
CT	0.47uF	CAP, CERM, 0.47uF, 16V, +/-10%, X7R, 0603	MuRata	GRM188R71C474KA88D	1
D1, D2		Zener Diode	Used in BOM report	SMBJ16A-TP	2
GND, GNDVO, VIN, VOUT		Terminal 90A Lug	Panduit	CB70-14-CY	4
GND1, GND2, GND3		Test Point, TH, Miniature, Black	Keystone Electronics	5001	3
H1, H2, H3, H4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH	4
H5, H6, H7, H8		Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C	4
PGD		Test Point, TH, Miniature, White	Keystone Electronics	5002	1
Q1, Q1x		MOSFET, N-CH, 20V, 100A	NXP	PSMN1R2-25YL	2
QT		NPN, 0.2A, 40V	Central Semiconductor	CMPT3904	1
R1, R6, RPG	10.0k	RES, 10.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310K0FKEA	3
R2	6.34k	RES, 6.34k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06036K34FKEA	1
R3	49.9k	RES, 49.9k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060349K9FKEA	1
R4	4.12k	RES, 4.12k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06034K12FKEA	1
R5	150k	RES, 150k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603150KFKEA	1
RFB1	22.6k	RES, 22.6k ohm, 0.1%, 0.1W, 0603	Yageo America	RT0603BRD0722K6L	1
RFB2	2.74k	RES, 2.74k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06032K74FKEA	1
RP1, RP2, RP3	10k	5%, 0.1W	Vishay-Dale	CRCW060310K0JNEA	3
RPWR	2.32k	RES, 2.32k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06032K32FKEA	1
RS+, RS-, TIMER, VAUX, VREF		Test Point, TH, Miniature, Yellow	Keystone Electronics	5004	5
RS, RSx	0.0005 Ohm	1%, 3W	Vishay-Dale	WSL3921L5000FEA	2
U1			Used in BOM report	Used in BOM report	1
VIN_TP, VOUT_TP		Test Point, TH, Miniature, Red	Keystone Electronics	5000	2

PC Board Layout



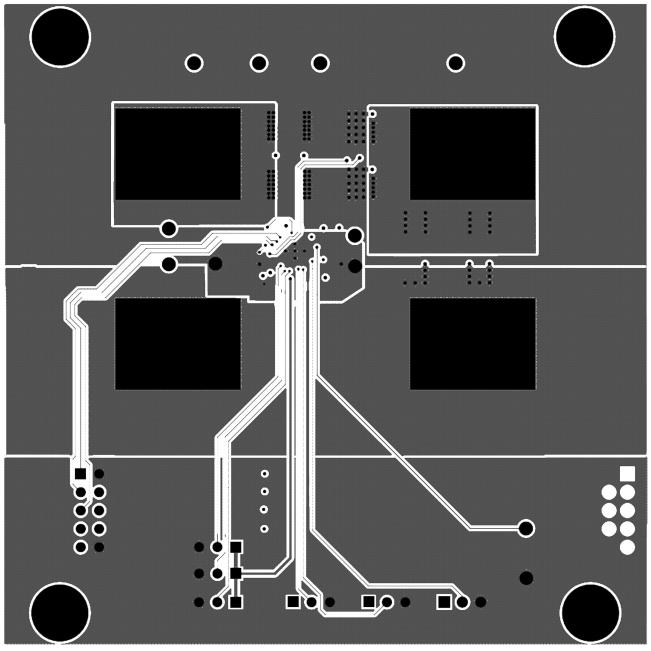
30143541

Board Silkscreen



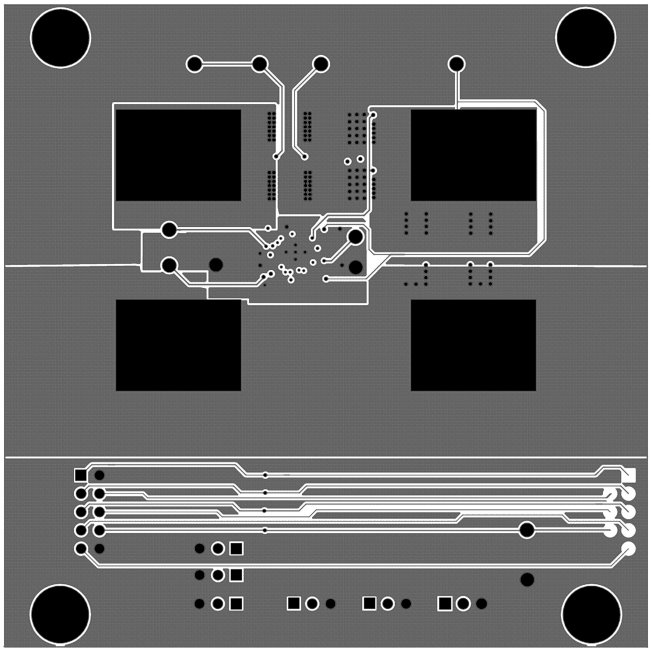
30143542

Board Top Layer



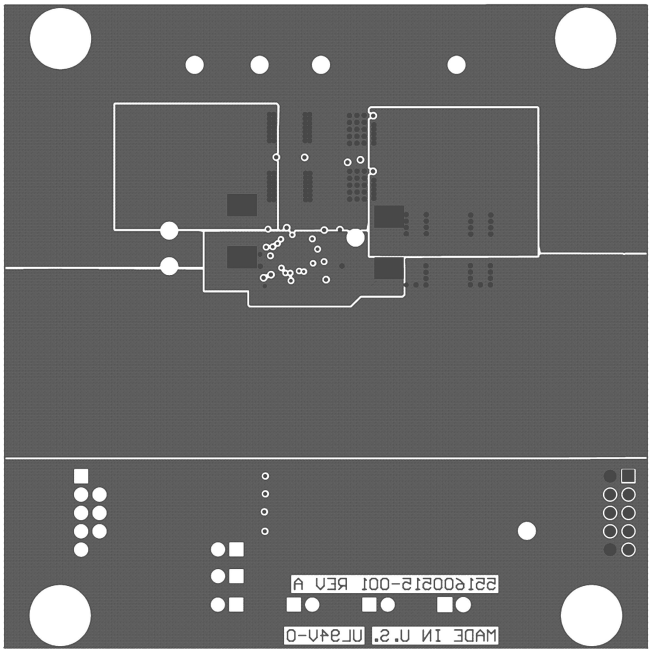
30143543

Board Mid Layer 1



30143544

Board Mid Layer 2



30143545

Board Bottom Layer (viewed from top)

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