

**OBSOLETE PRODUCT  
NO RECOMMENDED REPLACEMENT**  
contact our Technical Support Center at  
1-888-INTERSIL or www.intersil.com/tsc

**50MHz, Video Operational Amplifier**

The HA-2544 is a fast, unity gain stable, monolithic op amp designed to meet the needs required for accurate reproduction of video or high speed signals. It offers high voltage gain (6kV/V) and high phase margin (65 degrees) while maintaining tight gain flatness over the video bandwidth. Built from high quality Dielectric Isolation, the HA-2544 is another addition to the Intersil series of high speed, wideband op amps, and offers true video performance combined with the versatility of an op amp.

The primary features of the HA-2544 include 50MHz Gain Bandwidth, 150V/μs slew rate, 0.03% differential gain error and gain flatness of just 0.12dB at 10MHz. High performance and low power requirements are met with a supply current of only 10mA.

Uses of the HA-2544 range from video test equipment, guidance systems, radar displays and other precise imaging systems where stringent gain and phase requirements have previously been met with costly hybrids and discrete circuitry. The HA-2544 will also be used in non-video systems requiring high speed signal conditioning such as data acquisition systems, medical electronics, specialized instrumentation and communication systems.

Military (/883) product and data sheets are available upon request.

**Part # Information**

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HA3-2544C-5	0 to 75	8 Ld PDIP	E8.3

**Features**

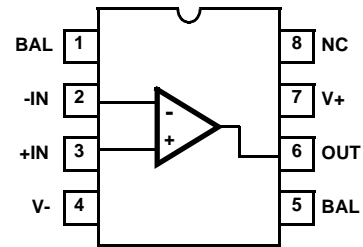
- Gain Bandwidth . . . . . 50MHz
- High Slew Rate . . . . . 150V/μs
- Low Supply Current . . . . . 10mA
- Differential Gain Error . . . . . 0.03%
- Differential Phase Error . . . . . 0.03 Degrees
- Gain Flatness at 10MHz. . . . . 0.12dB

**Applications**

- Video Systems
- Video Test Equipment
- Radar Displays
- Data Acquisition Systems
- Imaging Systems
- Pulse Amplifiers
- Signal Conditioning Circuits

**Pinout**

**HA-2544C (PDIP)**  
TOP VIEW



**Absolute Maximum Ratings**

Voltage Between V+ and V- Terminals ..... 35V  
 Differential Input Voltage (Note 1) ..... 6V  
 Peak Output Current ..... ±40mA

**Thermal Information**

Thermal Resistance (Typical, Note 2)  $\theta_{JA}$  (°C/W)  $\theta_{JC}$  (°C/W)  
 PDIP Package ..... 110 N/A  
 Maximum Junction Temperature (Plastic Packages) ..... 150°C  
 Maximum Storage Temperature Range ..... -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) ..... 300°C

**Operating Conditions**

Temperature Range  
 HA-2544C-5 ..... 0°C to 75°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTES:**

- To achieve optimum AC performance, the input stage was designed without protective diode clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of the input transistors and probable degradation of the input parameters especially  $V_{OS}$ ,  $I_{OS}$  and Noise.
- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications**  $V_{SUPPLY} = \pm 15V$ ,  $C_L \leq 10pF$ ,  $R_L = 1k\Omega$ , Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	-	25	-	15	25	mV
	-	-2, -5	-	-	40	mV
	-	-9	-	-	40	mV
Average Offset Voltage Drift (Note 7)	-	Full	-	10	-	$\mu V/^\circ C$
Bias Current	-	25	-	9	18	$\mu A$
	-	Full	-	-	30	$\mu A$
Average Bias Current Drift (Note 7)	-	Full	-	0.04	-	$\mu A/^\circ C$
Offset Current	-	25	-	0.8	2	$\mu A$
	-	Full	-	-	3	$\mu A$
Offset Current Drift	-	Full	-	10	-	$nA/^\circ C$
Common Mode Range	-	Full	±10	±11.5	-	V
Differential Input Resistance	-	25	50	90	-	$k\Omega$
Differential Input Capacitance	-	25	-	3	-	pF
Input Noise Voltage	f = 1kHz	25	-	20	-	$nV/\sqrt{Hz}$
Input Noise Current	f = 1kHz	25	-	2.4	-	$pA/\sqrt{Hz}$
Input Noise Voltage (Note 7)	0.1Hz to 10Hz	25	-	1.5	-	$\mu V_{P-P}$
	0.1Hz to 1MHz	25	-	4.6	-	$\mu V_{RMS}$
<b>TRANSFER CHARACTERISTICS</b>						
Large Signal Voltage Gain (Note 7)	$V_O = \pm 5V$	25	3	6	-	$kV/V$
		Full	2	-	-	$kV/V$
Common Mode Rejection Ratio (Note 7)	$\Delta V_{CM} = \pm 10V$	-2, -5	70	89	-	dB
		-9	65	89	-	dB
Minimum Stable Gain		25	+1	-	-	V/V
Unity Gain Bandwidth (Note 7)	$V_O = \pm 100mV$	25	-	45	-	MHz
Gain Bandwidth Product (Note 7)	$V_O = \pm 100mV$	25	-	50	-	MHz
Phase Margin		25	-	65	-	Degrees

# HA-2544

## Electrical Specifications $V_{SUPPLY} = \pm 15V$ , $C_L \leq 10pF$ , $R_L = 1k\Omega$ , Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	TYP	MAX	UNITS
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage Swing		Full	±10	±11	-	V
Full Power Bandwidth (Note 6)		25	3.2	4.2	-	MHz
Peak Output Current (Note 7)		25	±25	±35	-	mA
Continuous Output Current (Note 7)		25	±10	-	-	mA
Output Resistance	Open Loop	25	-	20	-	Ω
<b>TRANSIENT RESPONSE</b>						
Rise Time (Note 4)		25	-	7	-	ns
Overshoot (Note 4)		25	-	10	-	%
Slew Rate		25	100	150	-	V/μs
Settling Time (Note 5)		25	-	120	-	ns
<b>VIDEO PARAMETERS <math>R_L = 1k\Omega</math> (Note 8)</b>						
Differential Phase (Note 9)		25	-	0.03	-	Degree
Differential Gain (Notes 3, 9)		25	-	0.0026	-	dB
		25	-	0.03	-	%
Gain Flatness	5MHz	25	-	0.10	-	dB
	10MHz	25	-	0.12	-	dB
Chrominance to Luminance Gain (Note 10)		25	-	0.1	-	dB
Chrominance to Luminance Delay (Note 10)		25	-	7	-	ns
<b>POWER SUPPLY CHARACTERISTICS</b>						
Supply Current		Full	-	10	15	mA
Power Supply Rejection Ratio (Note 7)	$V_S = \pm 10V$ to $\pm 20V$	-2, -5	70	80	-	dB
		-9	65	80	-	dB

**NOTES:**

$$3. A_D(\%) = \left[ 10^{\frac{A_D(\text{dB})}{20}} - 1 \right] \times 100.$$

4. For Rise Time and Overshoot testing,  $V_{OUT}$  is measured from 0 to +200mV and 0 to -200mV.

5. Settling Time is specified to 0.1% of final value for a 10V step and  $A_V = -1$ .

6. Full Power Bandwidth is guaranteed by equation: Full Power Bandwidth =  $\frac{\text{Slew Rate}}{2\pi V_{PEAK}}$  ( $V_{PEAK} = 5V$ ).

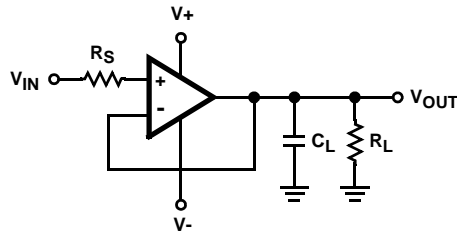
7. Refer to typical performance curve in Data Sheet.

8. The video parameter specifications will degrade as the output load resistance decreases.

9. Tested with a VM700A video tester, using a NTC-7 Composite input signal. For adequate test repeatability, a minimum warm-up of 2 minutes is suggested.  $A_V = +1$ .

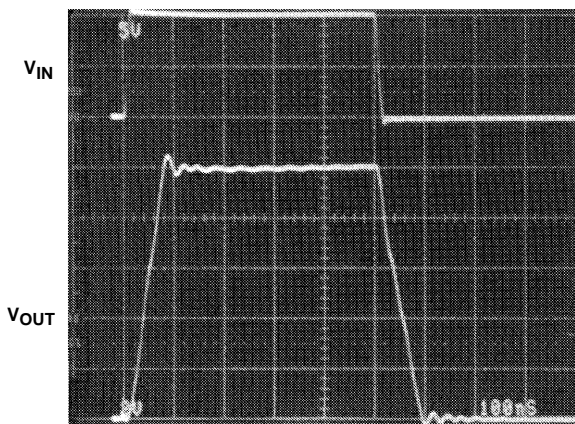
10. C-L Gain and C-L Delay was less than the resolution of the test equipment used which is 0.1dB and 7ns, respectively.

Test Circuits and Waveforms



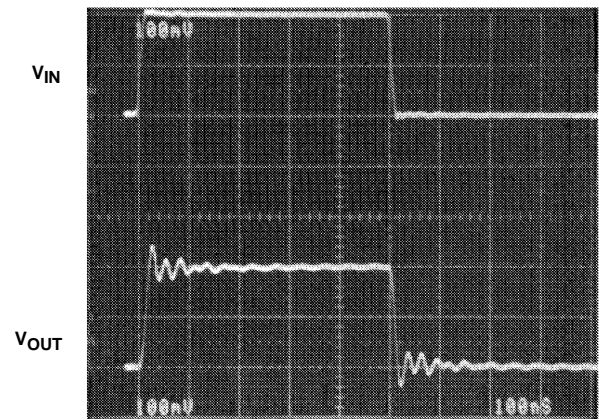
- NOTES:
11.  $V_S = \pm 15V$ .
  12.  $A_V = +1$ .
  13.  $R_S = 50\Omega$  or  $75\Omega$  (Optional).
  14.  $R_L = 1k\Omega$ .
  15.  $C_L < 10pF$ .
  16.  $V_{IN}$  for Large Signal =  $\pm 5V$ .
  17.  $V_{IN}$  for Small Signal = 0 to  $+200mV$  and 0 to  $-200mV$ .

FIGURE 1. TRANSIENT RESPONSE



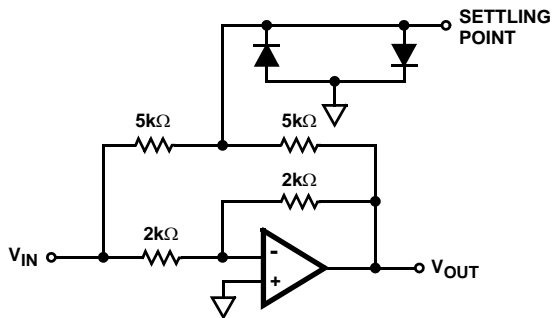
$V_{OUT} = 0$  to  $+10V$   
 Vertical Scale:  $V_{IN} = 5V/Div.$ ;  $V_{OUT} = 2V/Div.$   
 Horizontal Scale:  $100ns/Div.$

LARGE SIGNAL RESPONSE



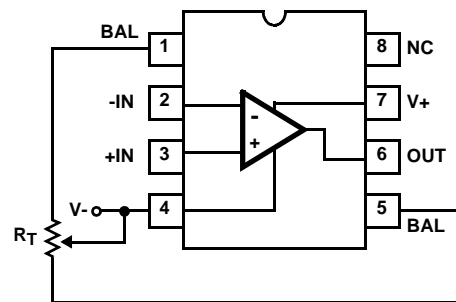
$V_{OUT} = 0$  to  $+200mV$   
 Vertical Scale:  $V_{IN} = 100mV/Div.$ ;  $V_{OUT} = 100mV/Div.$   
 Horizontal Scale:  $100ns/Div.$

SMALL SIGNAL RESPONSE



- NOTES:
18.  $A_V = -1$ .
  19. Feedback and summing resistor ratios should be 0.1% matched.
  20. HP5082-2810 clipping diodes recommended.
  21. Tektronix P6201 FET probe used at settling point.

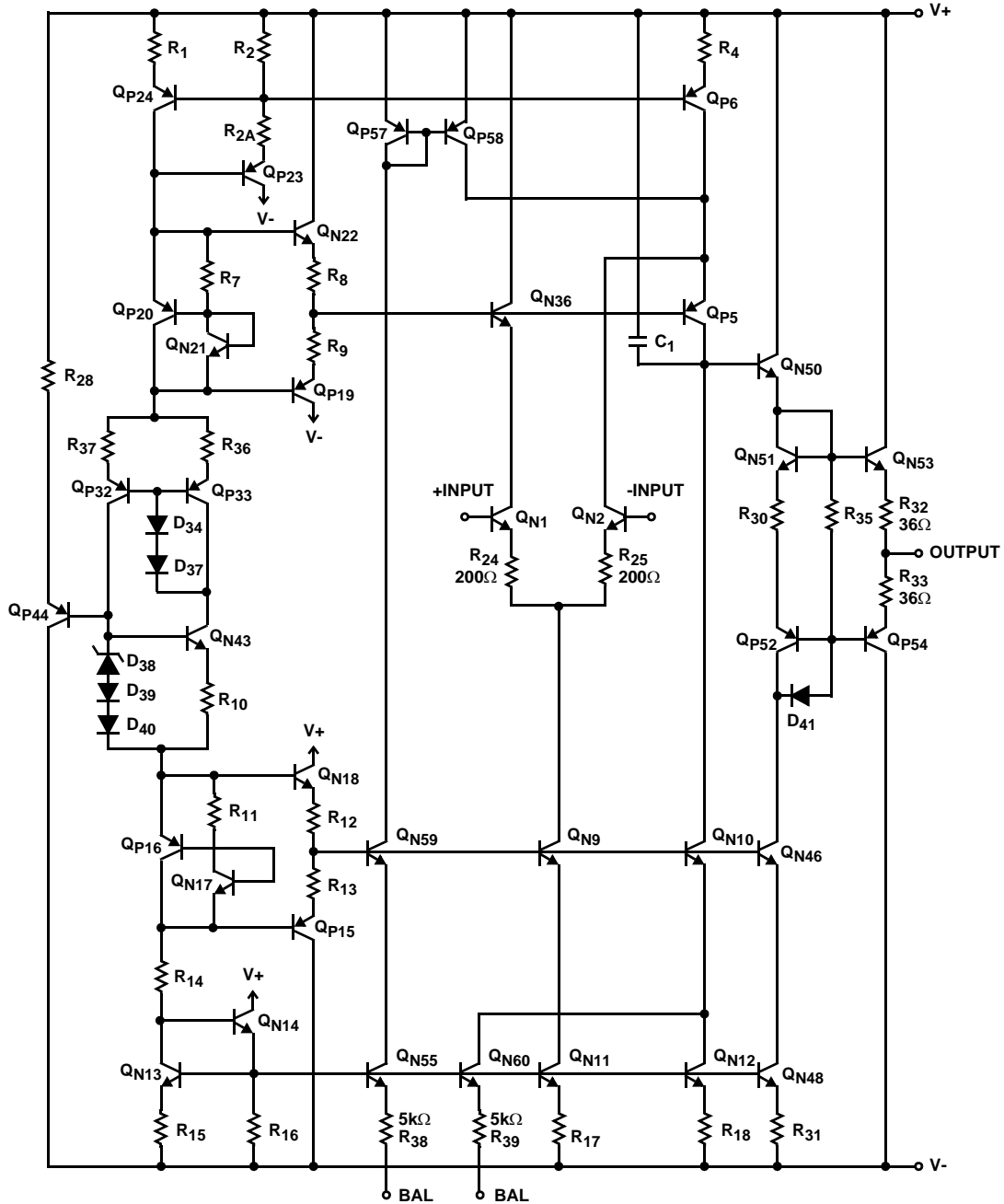
FIGURE 2. SETTLING TIME TEST CIRCUIT



NOTE: Tested offset adjustment range is  $|V_{OS} + 1mV|$  minimum referred to output. Typical range for  $R_T = 20k\Omega$  is approximately  $\pm 30mV$ .

FIGURE 3. OFFSET VOLTAGE ADJUSTMENT

**Schematic Diagram**



**Application Information**

The HA-2544 is a true differential op amp that is as versatile as any op amp but offers the advantages of high unity gain bandwidth, high speed and low supply current. More important than its general purpose applications is that the HA-2544 was especially designed to meet the requirements found in a video amplifier system. These requirements include fine picture resolution and accurate color rendition, and must meet broadcast quality standards.

In a video signal, the video information is carried in the amplitude and phase as well as in the DC level. The amplifier must pass the 30Hz line rate luminance level and the 3.58MHz

(NTSC) or 4.43MHz (PAL) color band without altering phase or gain. The HA-2544's key specifications aimed at meeting this include high bandwidth (50MHz), very low gain flatness (0.12dB at 10MHz), near unmeasurable differential gain and differential phase (0.03% and 0.03 degrees), and low noise (20nV/√Hz). The HA-2544 meets these guidelines.

The HA-2544 also offers the advantage of a full output voltage swing of ±10V into a 1kΩ load. This equates to a full power bandwidth of 2.4MHz for this ±10V signal. If video signal levels of ±2V maximum is used (with  $R_L = 1k\Omega$ ), the full power bandwidth would be 11.9MHz without clipping distortion.

Another usage might be required for a direct 50Ω or 75Ω load where the HA-2544 will still swing this ±2V signal as shown in the above display. One important note that must be realized is that as load resistance decreases the video parameters are also degraded. For optimal video performance a 1kΩ load is recommended.

If lower supply voltages are required, such as ±5V, many of the characterization curves indicate where the parameters vary. As shown the bandwidth, slew rate and supply current are still very well maintained.

**Prototyping and PC Board Layout**

When designing with the HA-2544 video op amp as with any high performance device, care should be taken to use high frequency layout techniques to avoid unwanted parasitic effects. Short lead lengths, low source impedance and lower value feedback resistors help reduce unwanted poles or zeros. This layout would also include ground plane construction and power supply decoupling as close to the supply pins with suggested parallel capacitors of 0.1μF and 0.001μF ceramic to ground.

In the noninverting configuration, the amplifier is sensitive to stray capacitance (<40pF) to ground at the inverting input. Therefore, the inverting node connections should be kept to a minimum. Phase shift will also be introduced as load parasitic capacitance is increased. A small series

resistor (20Ω to 100Ω) before the capacitance effectively decouples this effect.

**Stability/Phase Margin/Compensation**

The HA-2544 has not sacrificed unity gain stability in achieving its superb AC performance. For this device, the phase margin exceeds 60 degrees at the unity crossing point of the open loop frequency response. Large phase margin is critical in order to reduce the differential phase and differential gain errors caused by most other op amps. Because this part is unity gain stable, no compensation pin is brought out. If compensation is desired to reduce the noise bandwidth, most standard methods may be used. One method suggested for an inverting scheme would be a series R-C from the inverting node to ground which will reduce bandwidth, but not effect slew rate. If the user wishes to achieve even higher bandwidth (>50MHz), and can tolerate some slight gain peaking and lower phase margin, experimenting with various load capacitance can be done.

Shown in Application 1 is an excellent Differential Input, Unity Gain Buffer which also will terminate a cable to 75Ω and reject common mode voltages. Application 2 is a method of separating a video signal up into the Sync only signal and the Video and Blanking signal. Application 3 shows the HA-2544 being used as a 100kHz High Pass 2-Pole Butterworth Filter. Also shown is the measured frequency response curves.

**Typical Applications**

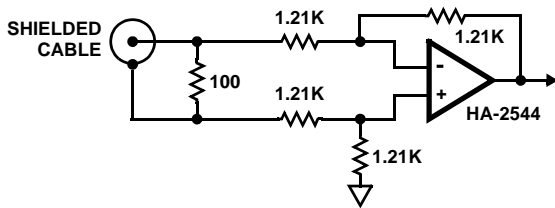


FIGURE 4. APPLICATION 1, 75Ω DIFFERENTIAL INPUT BUFFER

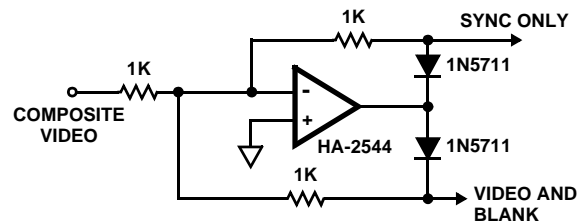


FIGURE 5. APPLICATION 2, COMPOSITE VIDEO SYNC SEPARATOR

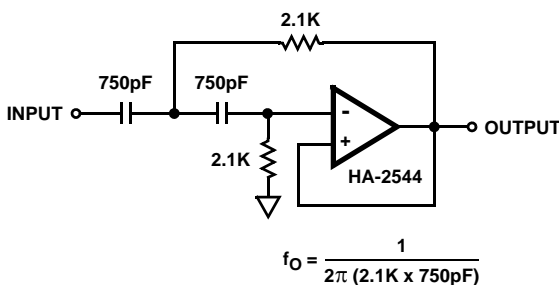


FIGURE 6. APPLICATION 3, 100kHz HIGH PASS 2-POLE BUTTERWORTH FILTER

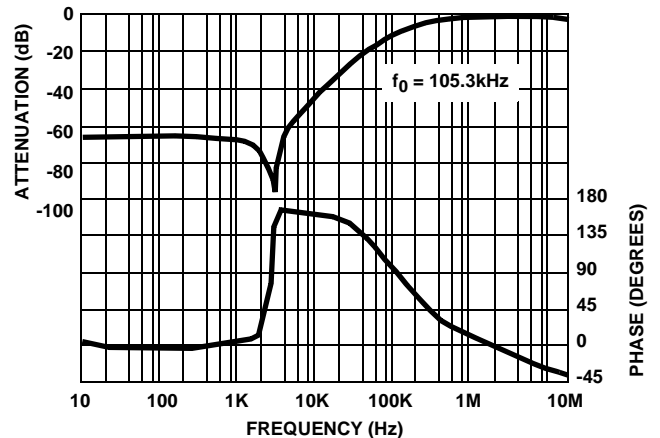


FIGURE 7. MEASURED FREQUENCY RESPONSE OF APPLICATION 3



Typical Performance Curves

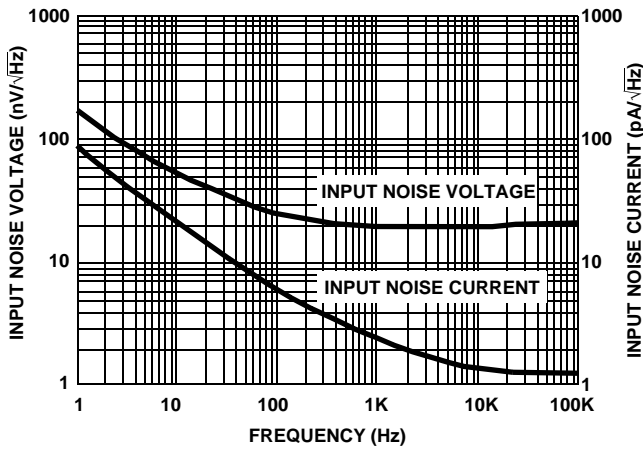


FIGURE 8. INPUT NOISE VOLTAGE AND NOISE CURRENT vs FREQUENCY

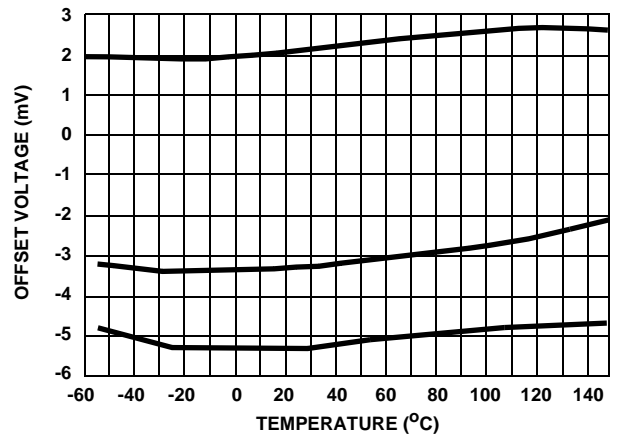
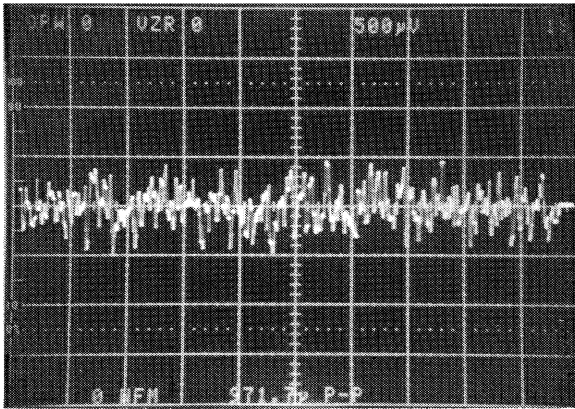


FIGURE 9. INPUT OFFSET VOLTAGE vs TEMPERATURE (3 TYPICAL UNITS)



0.1Hz to 10Hz, Noise Voltage = 0.97 μV<sub>p-p</sub>

FIGURE 10. NOISE VOLTAGE ( $A_v = 1000$ )

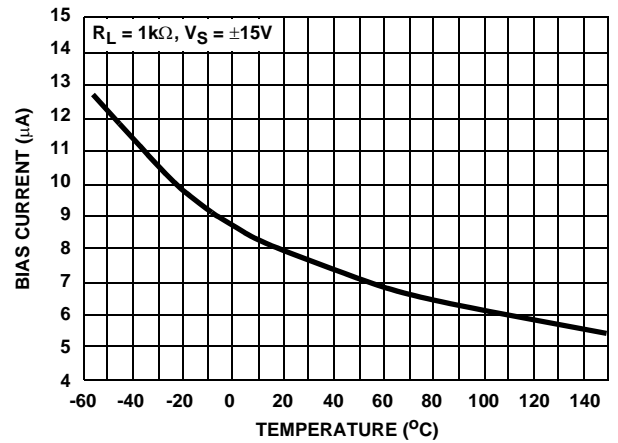


FIGURE 11. INPUT BIAS CURRENT vs TEMPERATURE

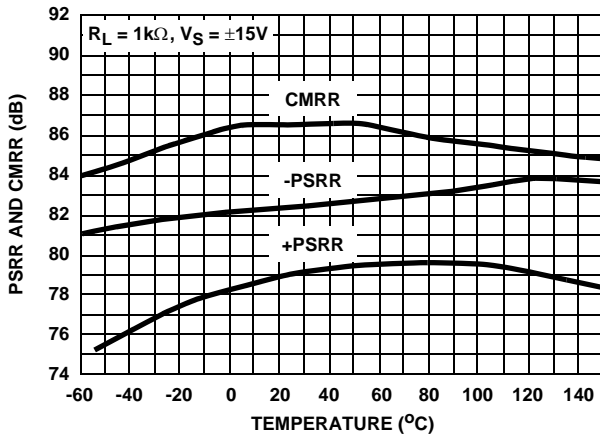


FIGURE 12. PSRR AND CMRR vs TEMPERATURE

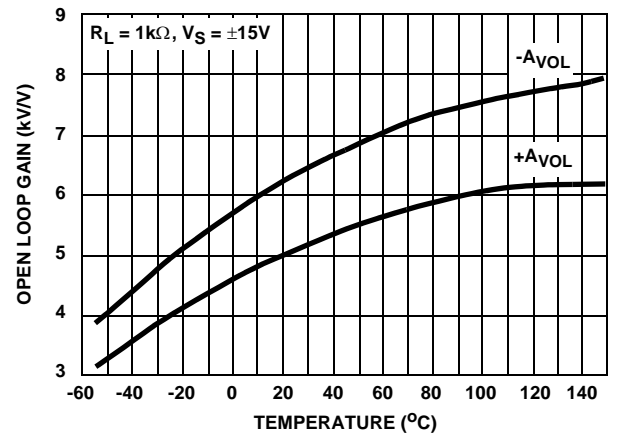


FIGURE 13. OPEN LOOP GAIN vs TEMPERATURE

Typical Performance Curves (Continued)

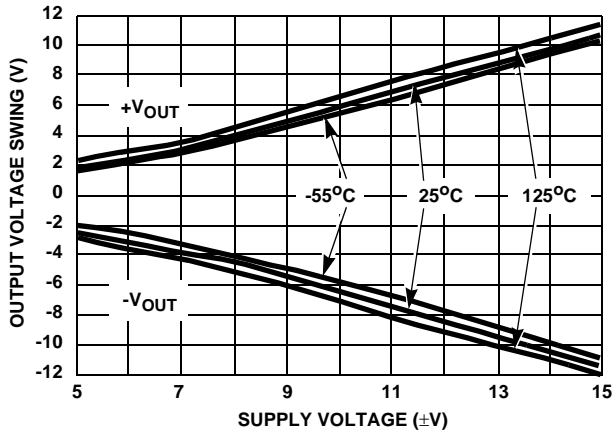


FIGURE 14. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

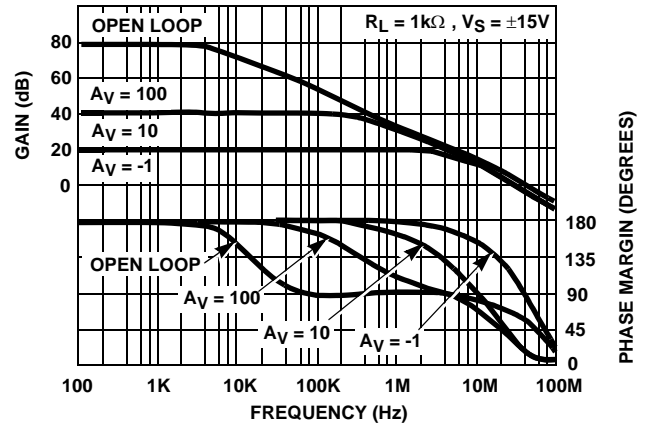


FIGURE 15. FREQUENCY RESPONSE AT VARIOUS GAINS

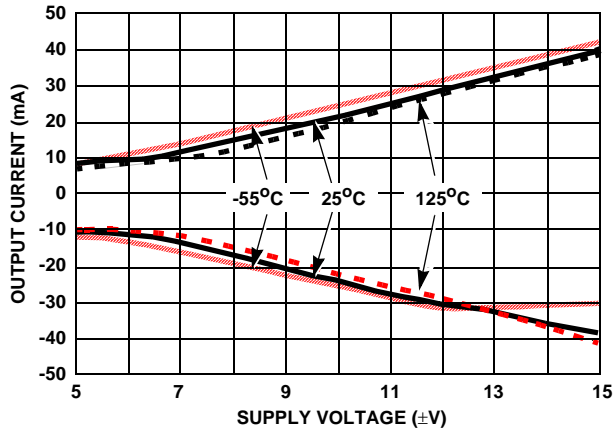


FIGURE 16. OUTPUT CURRENT vs SUPPLY VOLTAGE

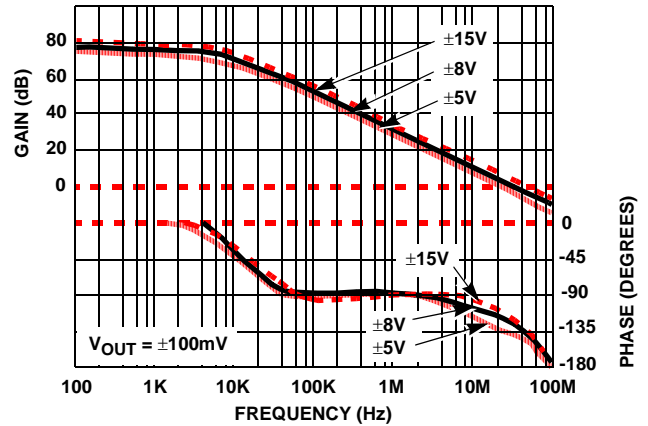


FIGURE 17. OPEN LOOP RESPONSE

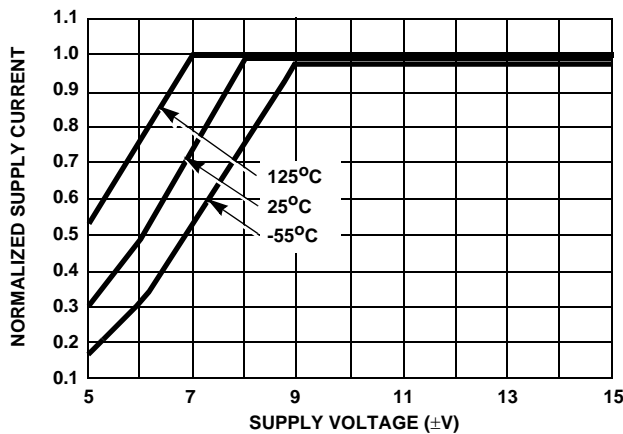


FIGURE 18. SUPPLY CURRENT vs SUPPLY VOLTAGE (NORMALIZED TO  $V_S = \pm 15V$  AT  $25^\circ C$ )

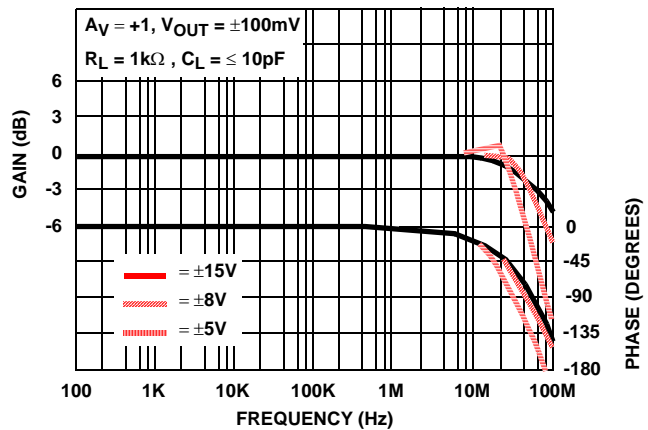


FIGURE 19. VOLTAGE FOLLOWER RESPONSE



Typical Video Performance Curves

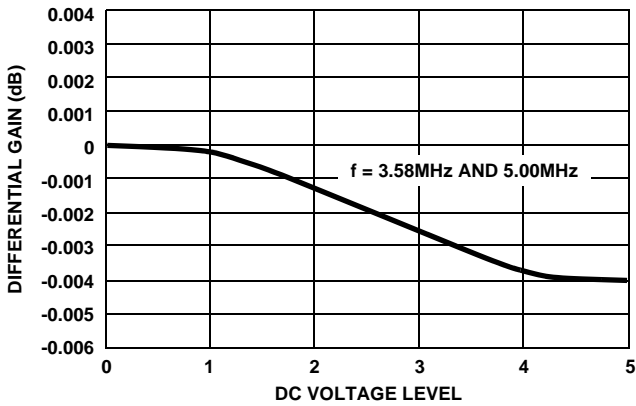


FIGURE 20. AC GAIN VARIATION vs DC OFFSET LEVELS (DIFFERENTIAL GAIN)

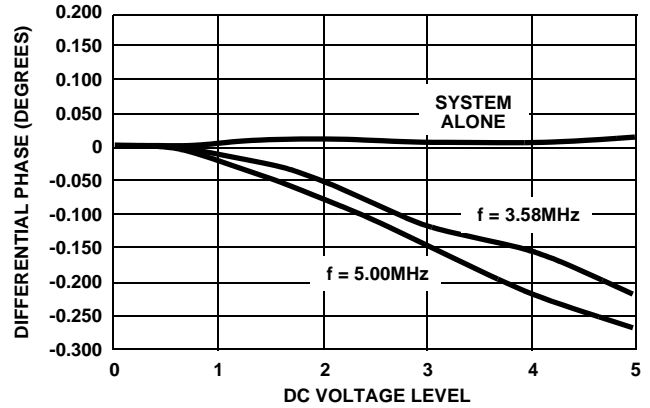
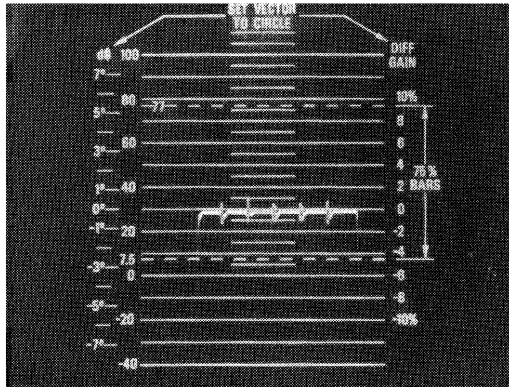
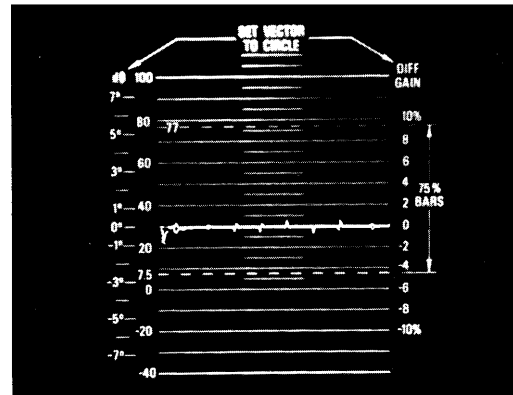


FIGURE 21. AC PHASE VARIATION vs DC OFFSET LEVELS (DIFFERENTIAL PHASE)



NTSC Method,  $R_L = 1k\Omega$ , Differential Gain  $< 0.05\%$  at  $T_A = 75^\circ C$   
No Visual Difference at  $T_A = -55^\circ C$  or  $125^\circ C$

FIGURE 22. DIFFERENTIAL GAIN



NTSC Method,  $R_L = 1k\Omega$ ,  
Differential Phase  $< 0.05$  Degree at  $T_A = 75^\circ C$   
No Visual Difference at  $T_A = -55^\circ C$  or  $125^\circ C$

FIGURE 23. DIFFERENTIAL PHASE

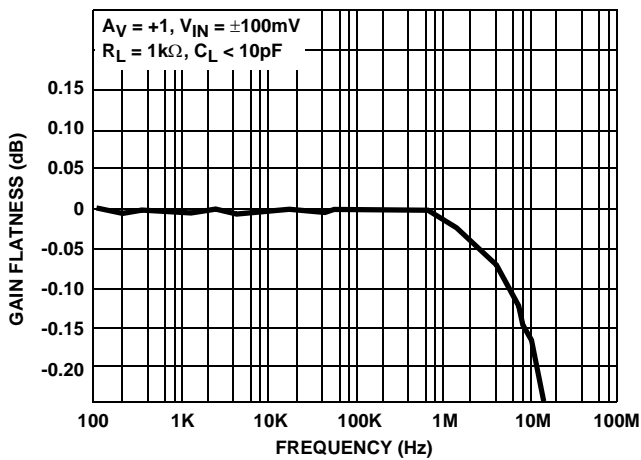
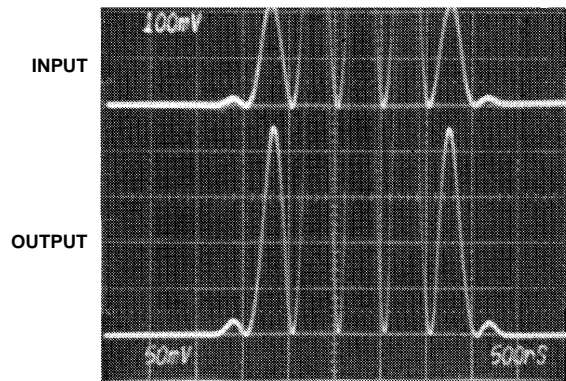


FIGURE 24. GAIN FLATNESS



NTSC Method,  $R_L = 1k\Omega$ , C-L Delay  $< 7ns$  at  $T_A = 75^\circ C$   
No Visual Difference at  $T_A = -55^\circ C$  or  $125^\circ C$   
Vertical Scale: Input = 100mV/Div., Output = 50mV/Div.  
Horizontal Scale: 500ns/Div.

FIGURE 25. CHROMINANCE TO LUMINANCE DELAY

Typical Video Performance Curves (Continued)

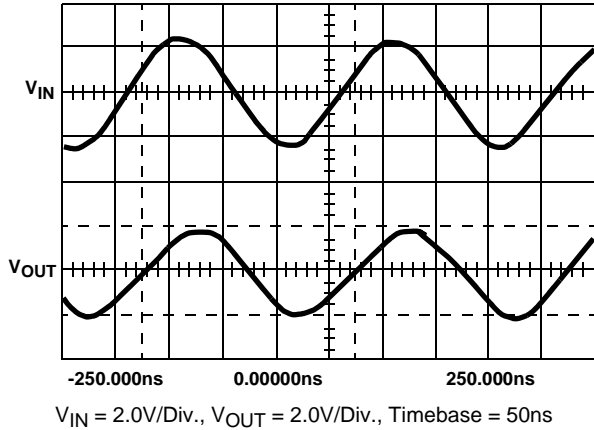


FIGURE 26.  $\pm 2V$  OUTPUT SWING (WITH  $R_{LOAD} = 75\Omega$ , FREQUENCY = 5.00MHz)

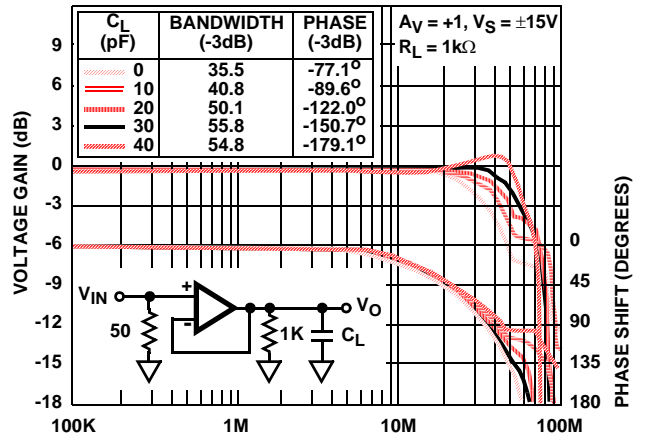


FIGURE 27. BANDWIDTH vs LOAD CAPACITANCE

Die Characteristics

DIE DIMENSIONS:

80 mils x 64 mils x 19 mils  
 2030 $\mu$ m x 1630 $\mu$ m x 483 $\mu$ m

METALLIZATION:

Type: Al, 1% Cu  
 Thickness: 16k $\text{\AA}$   $\pm$  2k $\text{\AA}$

PASSIVATION:

Type: Nitride ( $\text{Si}_3\text{N}_4$ ) over Silox ( $\text{SiO}_2$ , 5% Phos.)  
 Silox Thickness: 12k $\text{\AA}$   $\pm$  2k $\text{\AA}$   
 Nitride Thickness: 3.5k $\text{\AA}$   $\pm$  1.5k $\text{\AA}$

SUBSTRATE POTENTIAL (POWERED UP):

V-

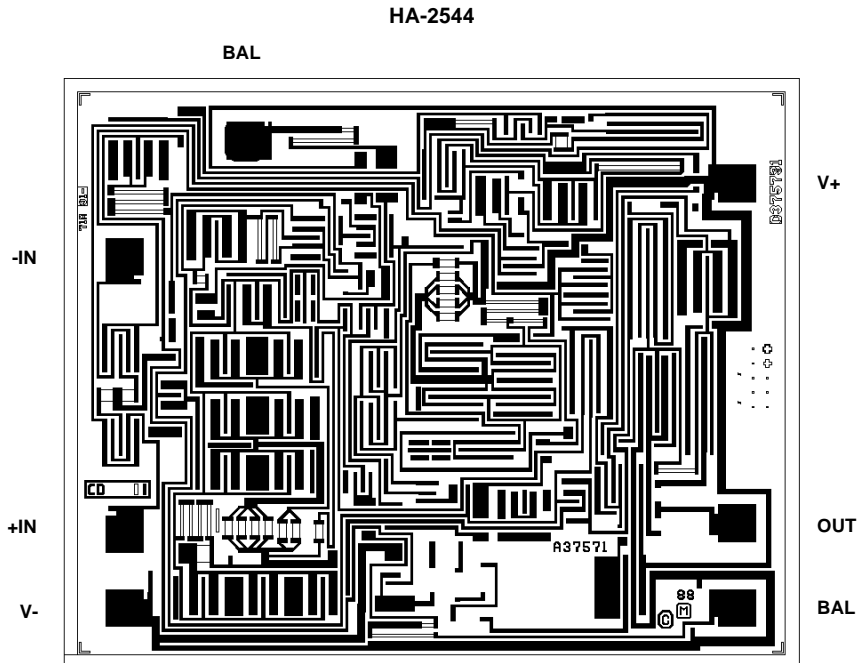
TRANSISTOR COUNT:

44

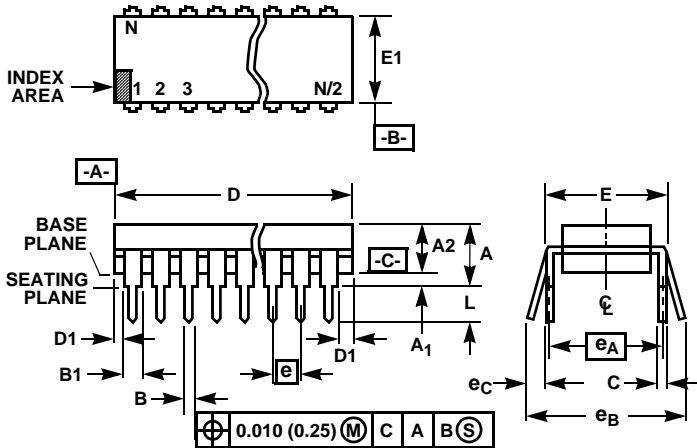
PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout



Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and  $e_A$  are measured with the leads constrained to be perpendicular to datum  $-C-$ .
7.  $e_B$  and  $e_C$  are measured at the lead tips with the leads unconstrained.  $e_C$  must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)  
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
$e_A$	0.300 BSC		7.62 BSC		6
$e_B$	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93

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