

### FEATURES

- Dual Device Module
- Electrically Isolated Package
- Pressure Contact Construction
- International Standard Footprint
- Alumina (Non Toxic) Isolation Medium
- Integral Water Cooled Heatsink

### APPLICATIONS

- Motor Control
- Controlled Rectifier Bridges
- Heater Control
- AC Phase Control

### VOLTAGE RATINGS

Type Number	Repetitive Peak Voltages $V_{DRM}$ $V_{RRM}$	Conditions
MP04TT500-28	2800	$T_{vj} = 0^\circ \text{ to } 125^\circ \text{C}$ , $I_{DRM} = I_{RRM} = 50\text{mA}$ $V_{DSM} = V_{RSM} =$ $V_{DRM} = V_{RRM} + 100\text{V}$ respectively
MP04TT500-27	2700	
MP04TT500-26	2600	
MP04TT500-25	2500	

Lower voltage grades available

### ORDERING INFORMATION

Order As:

<b>MP04TT500-XX-W2</b>	1/4 - 18 NPT connection
<b>MP04TT500-XX-W3</b>	1/4 - 18 NPT connection
<b>MP04TT500-XX-W3A</b>	1/4 - 18 NPT water connection thread

XX shown in the part number about represents  $V_{DRM}/100$  selection required, eg. MP04TT500-27-W2

Note: When ordering, please use the complete part number.

### KEY PARAMETERS

$V_{DRM}$	<b>2800V</b>
$I_{T(AV)}$ (per arm)	<b>480A</b>
$I_{TSM}$ (per arm)	<b>11200A</b>
$I_{T(RMS)}$ (per arm)	<b>753A</b>
$V_{isol}$	<b>3000V</b>

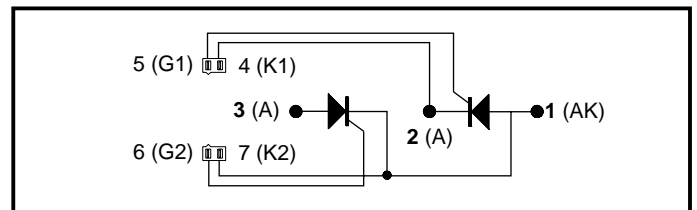


Fig. 1 TT Circuit diagram

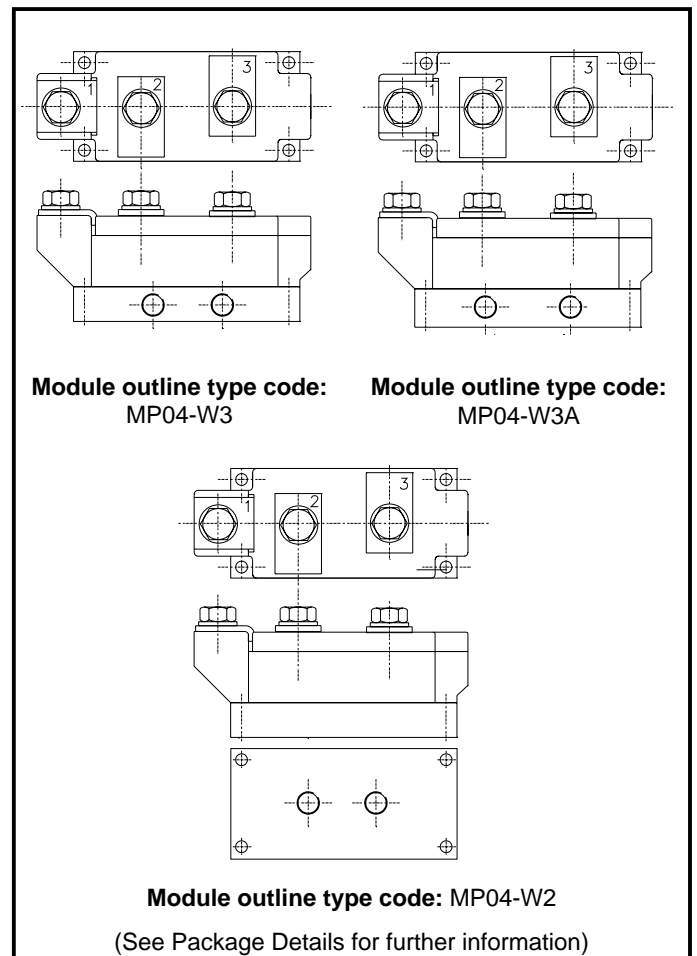


Fig. 2 Module package variants - (not to scale)

## ABSOLUTE MAXIMUM RATINGS - PER ARM

Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed. Exposure to Absolute Maximum Ratings may affect device reliability.

Symbol	Parameter	Test Conditions	Max.	Units	
$I_{T(AV)}$	Mean on-state current	Half wave resistive load, 4.5 Ltr/min	$T_{water (in)} = 25^{\circ}C$	540	A
			$T_{water (in)} = 40^{\circ}C$	480	A
$I_{T(RMS)}$	RMS value	$T_{water (in)} = 25^{\circ}C @ 4.5 \text{ Ltr/min}$		845	A
		$T_{water (in)} = 40^{\circ}C @ 4.5 \text{ Ltr/min}$		753	A
$I_{TSM}$	Surge (non-repetitive) on-current	10ms half sine, $T_j = 125^{\circ}C$		11.25	kA
$I^2t$	$I^2t$ for fusing	$V_R = 0$		$633 \times 10^3$	$A^2s$
$I_{TSM}$	Surge (non-repetitive) on-current	10ms half sine, $T_j = 125^{\circ}C$		9	kA
$I^2t$	$I^2t$ for fusing	$V_R = 50\% V_{DRM}$		$506 \times 10^3$	$A^2s$
$V_{isol}$	Isolation voltage	Commoned terminals to base plate. AC RMS, 1 min, 50Hz		3000	V

## THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units
$R_{th(j-w)}$	Thermal resistance - junction to water (per thyristor)	dc, 4.5 Ltr/min	-	0.102	$^{\circ}C/kW$
		Half wave, 4.5 Ltr/min	-	0.106	$^{\circ}C/kW$
		3 Phase, 4.5 Ltr/min	-	0.112	$^{\circ}C/kW$
$T_{vj}$	Virtual junction temperature	Reverse (blocking)	-	125	$^{\circ}C$
$T_{stg}$	Storage temperature range	-	-40	125	$^{\circ}C$
-	Screw torque	Mounting - M6	6 (53)	-	Nm (lb.ins)
		Electrical connections - M10	-	12 (106)	Nm (lb.ins)

**DYNAMIC CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Min.	Max.	Units
$I_{RRM}/I_{DRM}$	Peak reverse and off-state current	At $V_{RRM}/V_{DRM}$ , $T_j = 125^\circ\text{C}$	-	50	mA
dV/dt	Linear rate of rise of off-state voltage	To 67% $V_{DRM}$ , $T_j = 125^\circ\text{C}$	-	1000	V/ $\mu\text{s}$
dI/dt	Rate of rise of on-state current	From 67% $V_{DRM}$ to 500A, gate source 10V, 5 $\Omega$ $t_r = 0.5\mu\text{s}$ , $T_j = 125^\circ\text{C}$	-	500	A/ $\mu\text{s}$
$V_{T(TO)}$	Threshold voltage. (See note 1)	At $T_{vj} = 125^\circ\text{C}$	-	0.91	V
$r_T$	On-state slope resistance. (See note 1)	At $T_{vj} = 125^\circ\text{C}$	-	0.65	m $\Omega$

**Note 1:** The data given in this datasheet with regard to forward voltage drop is for calculation of the power dissipation in the semiconductor elements only. Forward voltage drops measured at the power terminals of the module will be in excess of these figures due to the impedance of the busbar from the terminal to the semiconductor.

**GATE TRIGGER CHARACTERISTICS AND RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
$V_{GT}$	Gate trigger voltage	$V_{DRM} = 5\text{V}$ , $T_{case} = 25^\circ\text{C}$	3.5	V
$I_{GT}$	Gate trigger current	$V_{DRM} = 5\text{V}$ , $T_{case} = 25^\circ\text{C}$	200	mA
$V_{GD}$	Gate non-trigger voltage	At $V_{DRM}$ , $T_{case} = 125^\circ\text{C}$	0.25	V
$V_{FGM}$	Peak forward gate voltage	Anode positive with respect to cathode	30	V
$V_{FGN}$	Peak forward gate voltage	Anode negative with respect to cathode	0.25	V
$V_{RGM}$	Peak reverse gate voltage	-	5	V
$I_{FGM}$	Peak forward gate current	Anode positive with respect to cathode	10	A
$P_{GM}$	Peak gate power	See table fig. 5	150	W
$P_{G(AV)}$	Mean gate power	-	10	W

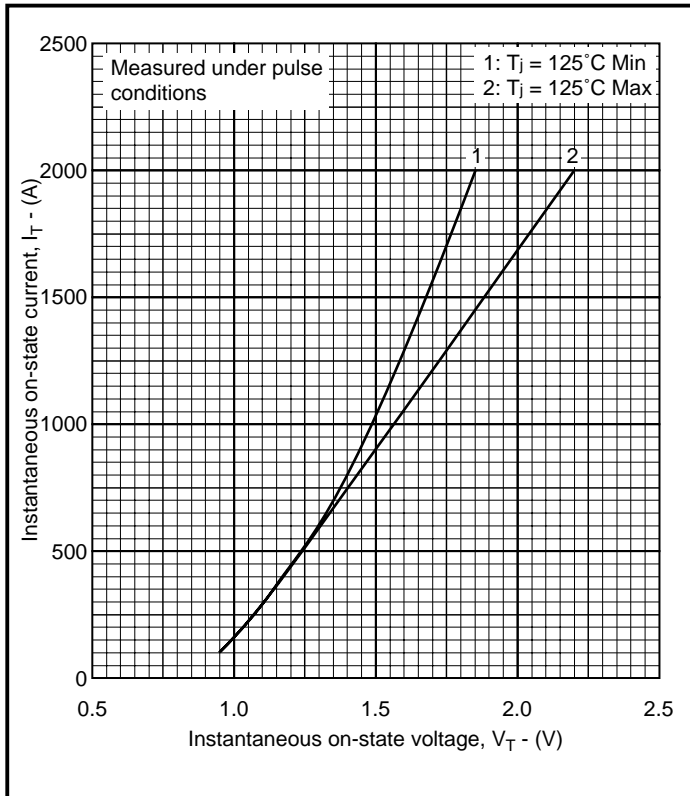


Fig. 3 Maximum (limit) on-state characteristics

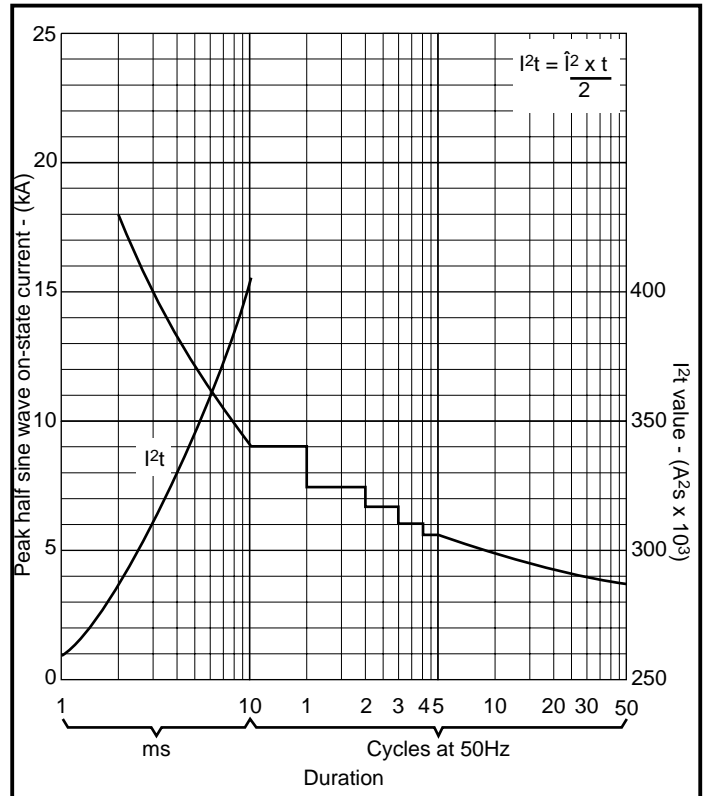


Fig. 4 Surge (non-repetitive) on-state current vs time (with 50%  $V_{RSM}$  at  $T_{case} = 125^\circ\text{C}$ )

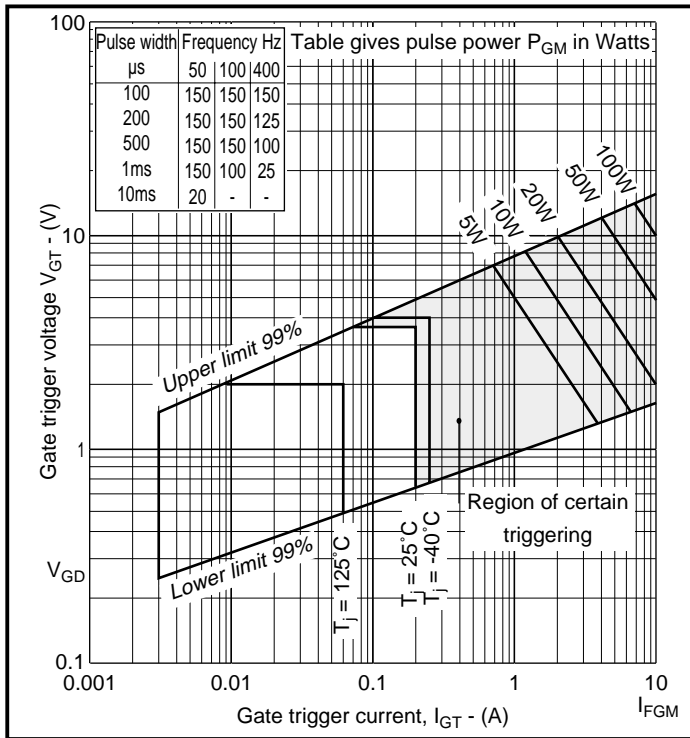


Fig. 5 Gate characteristics

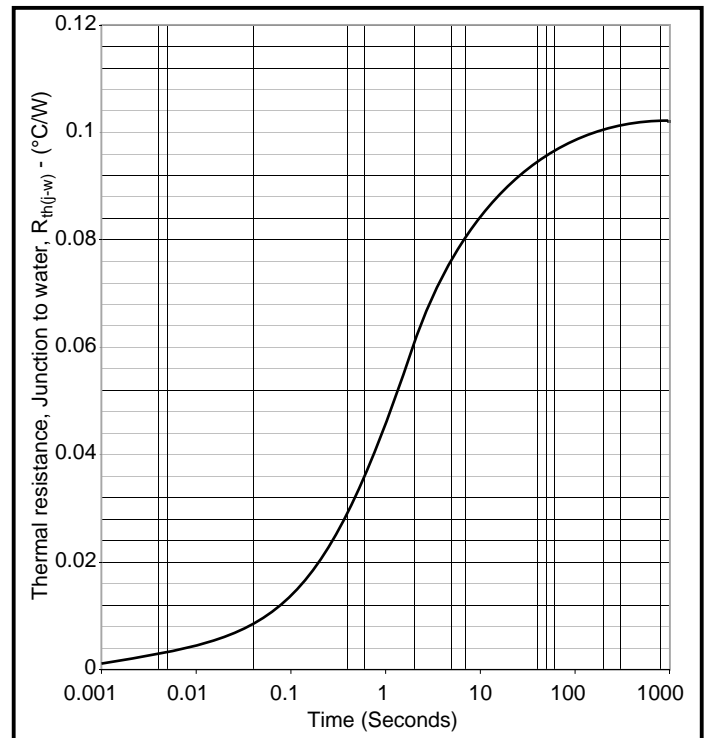
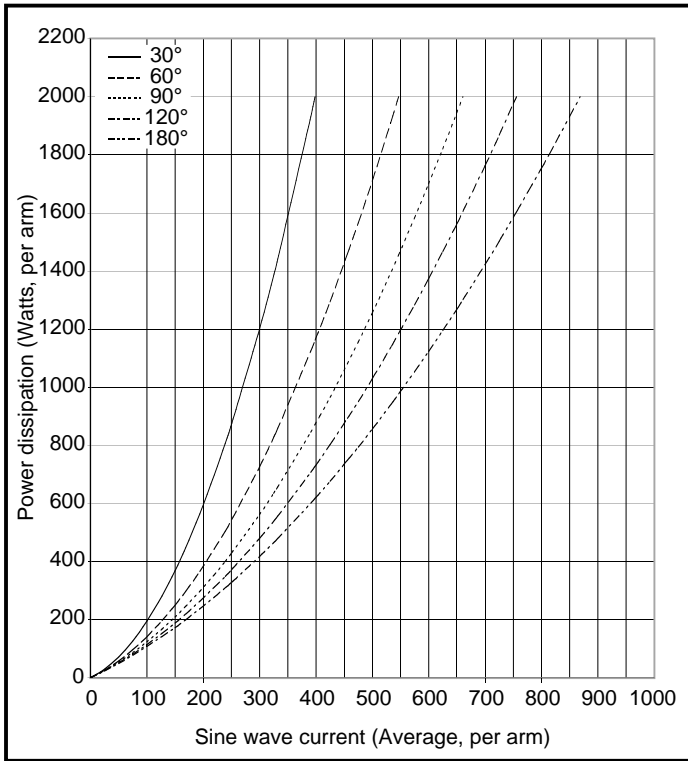
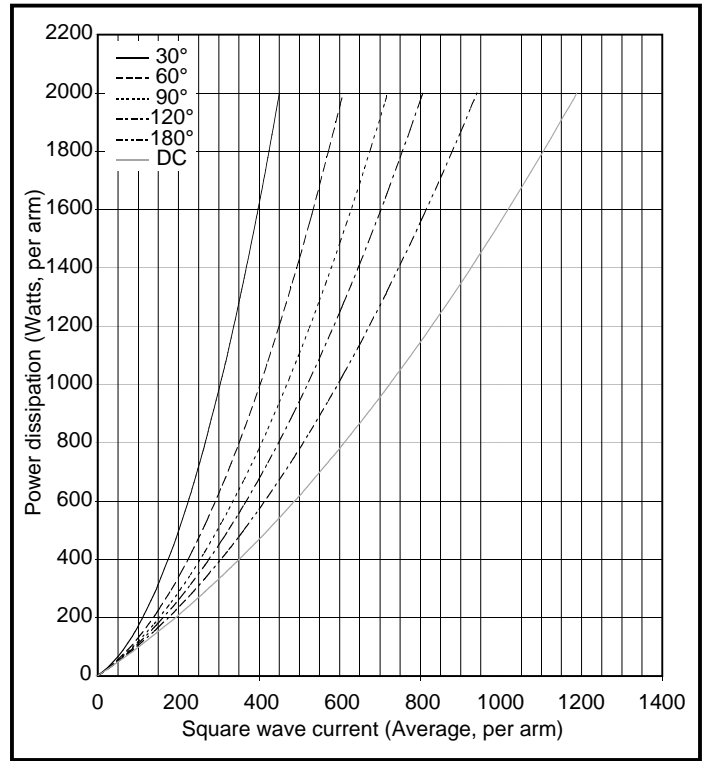


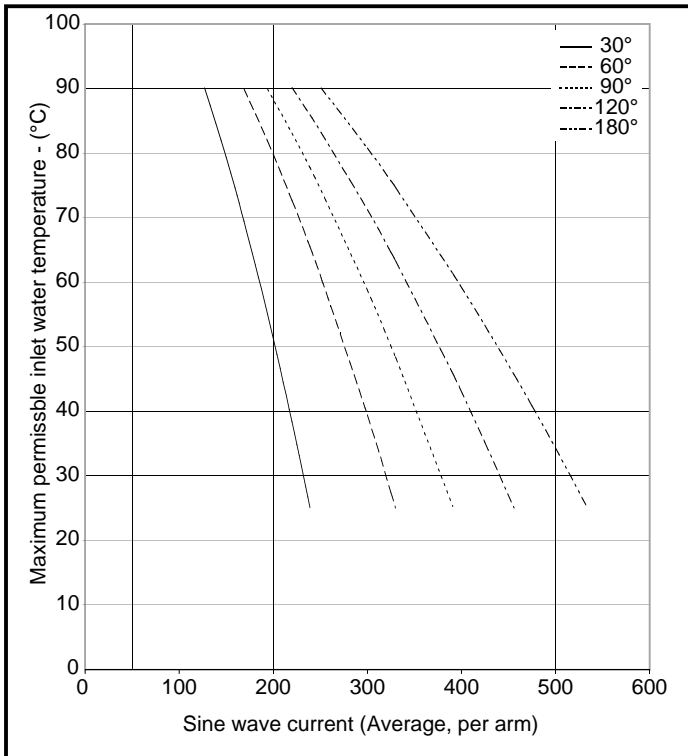
Fig. 6 Transient thermal impedance - dc



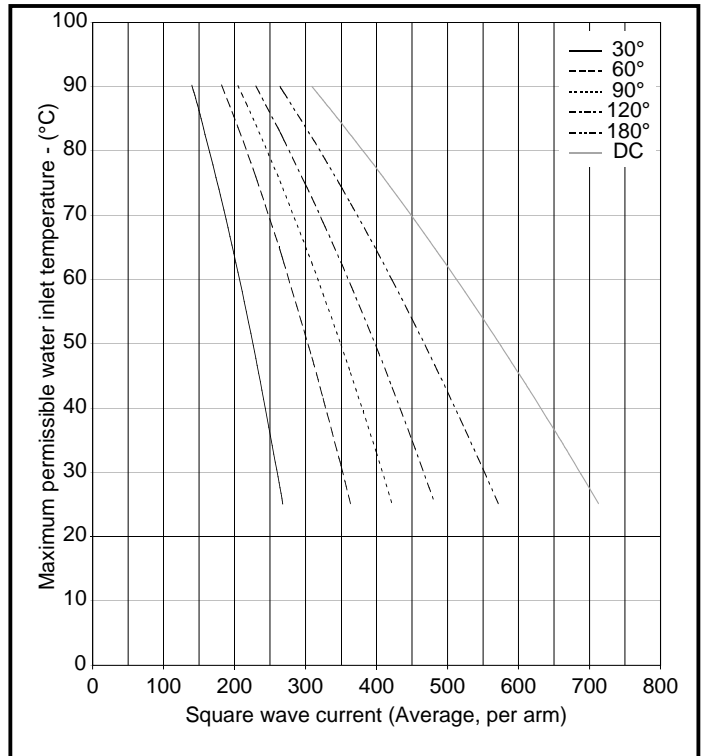
**Fig. 7 On-state power loss per arm vs on-state current at specified conduction angles, sine wave 50/60Hz**



**Fig. 8 On-state power loss per arm vs on-state current at specified conduction angles, square wave 50/60Hz**



**Fig. 9 Maximum permissible water inlet temperature vs on-state current at specified conduction angles, sine wave 50/60Hz**



**Fig. 10 Maximum permissible water inlet temperature vs on-state current at specified conduction angles, square wave 50/60Hz**

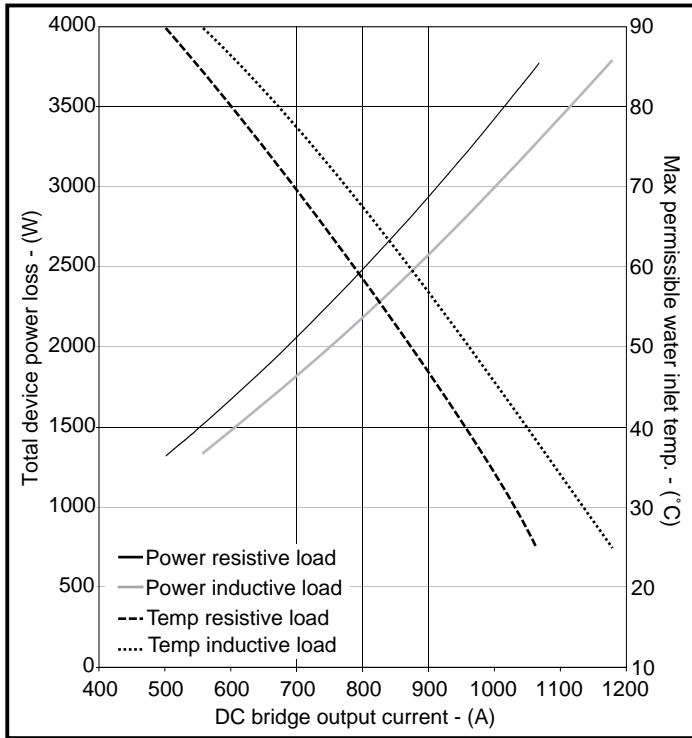


Fig. 11 50/60Hz single phase bridge DC output current vs power loss and maximum permissible water inlet

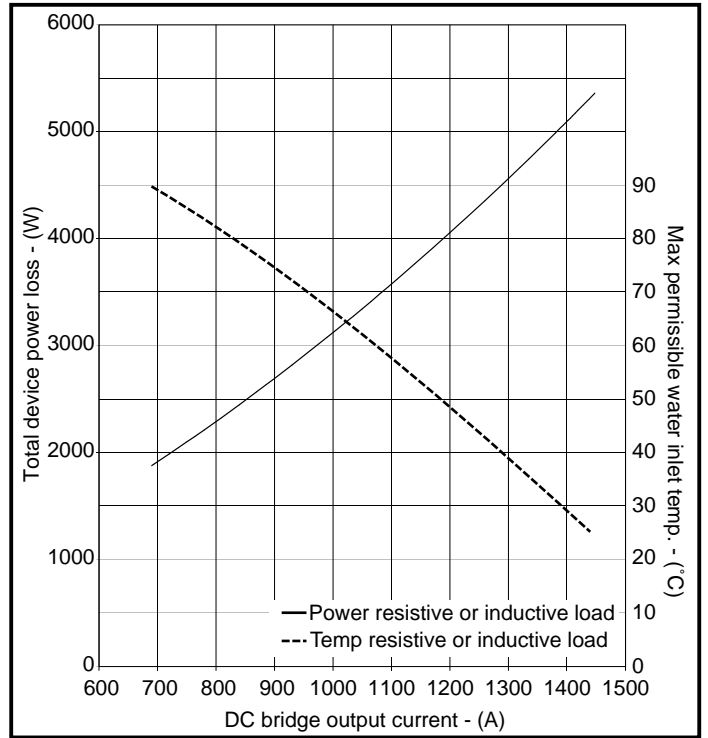
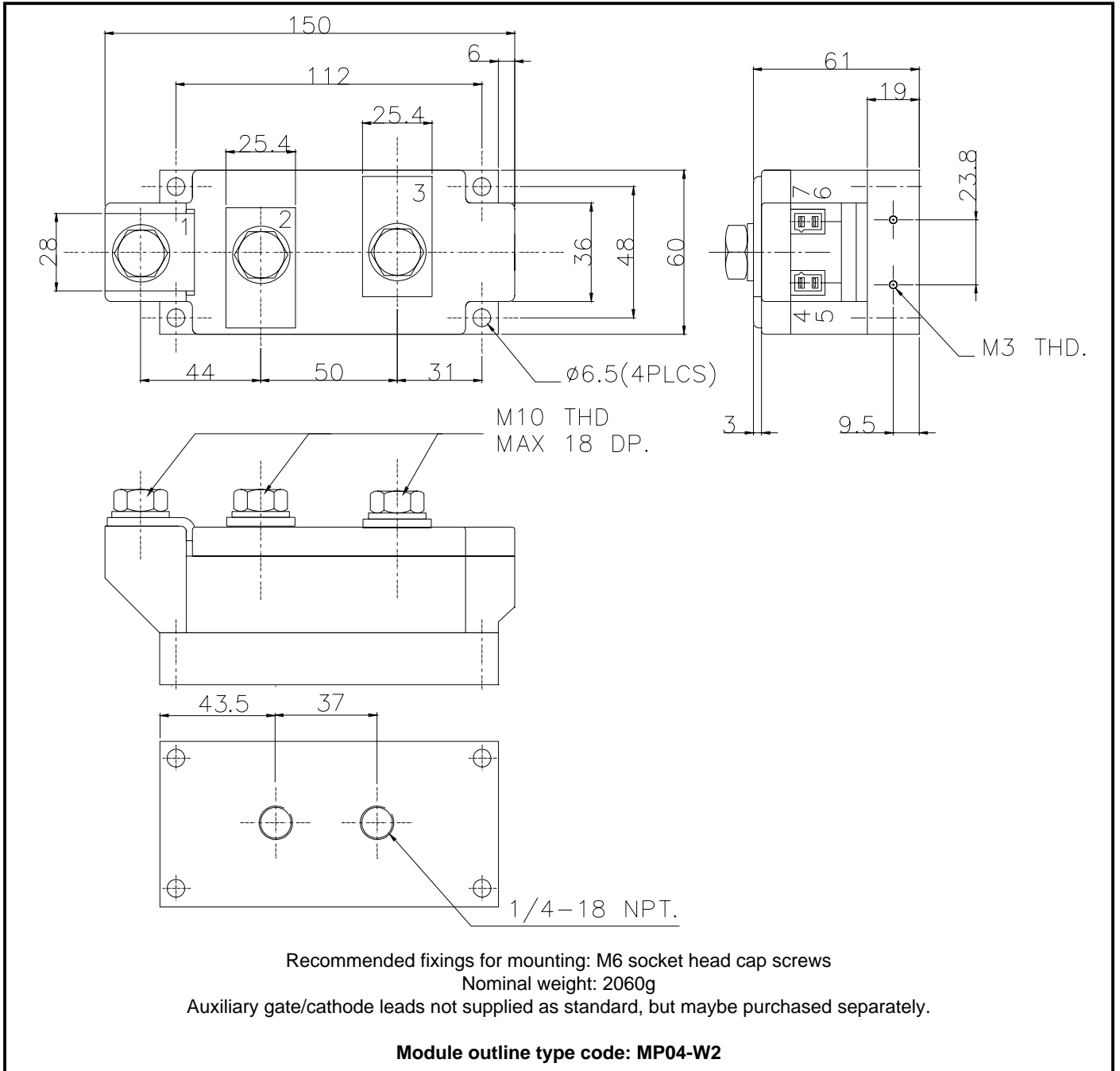


Fig. 12 50/60Hz three phase bridge DC output current vs power loss and maximum permissible water inlet

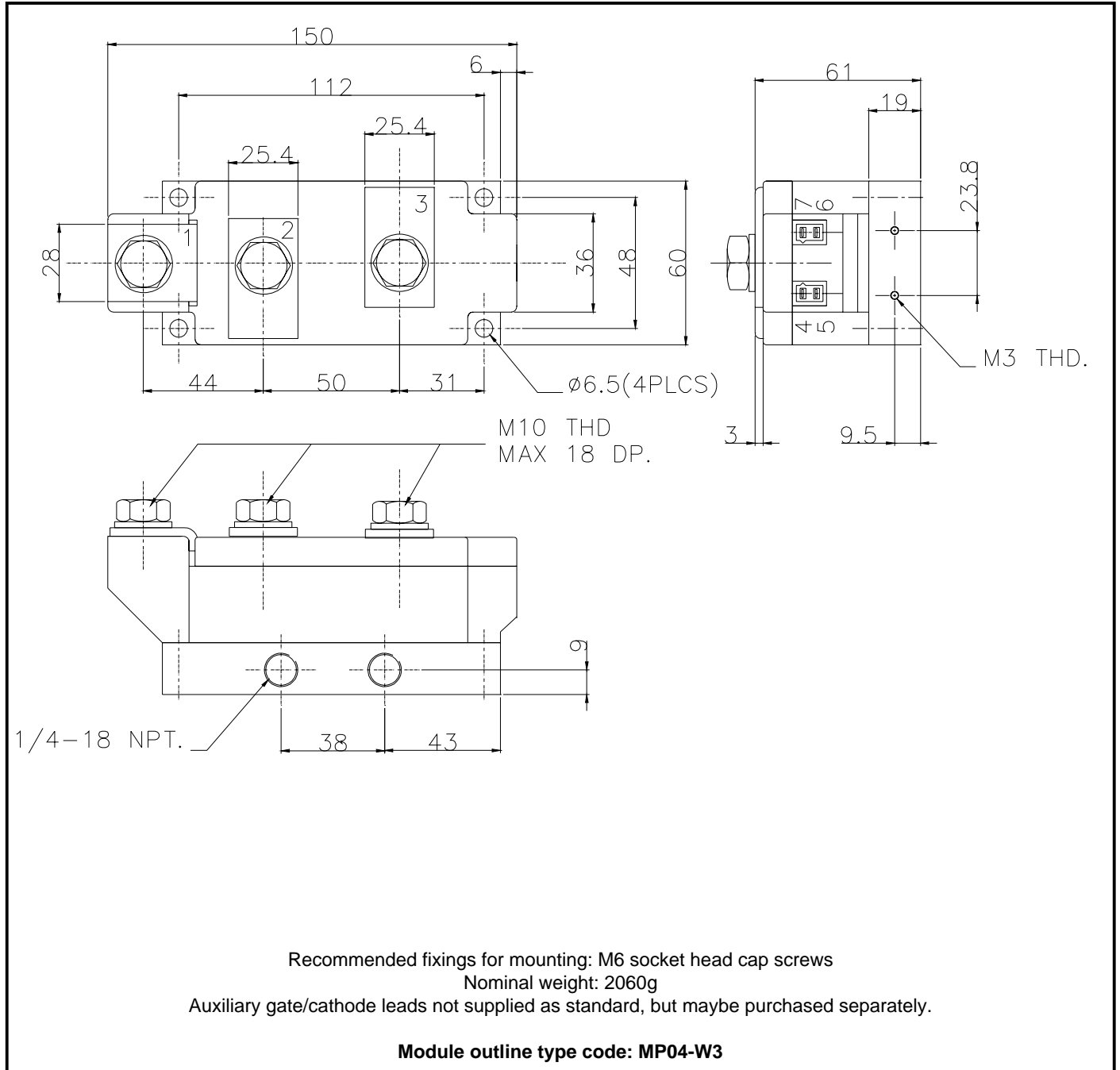
**PACKAGE DETAILS**

For further package information, please visit our website or contact your nearest Customer Service Centre. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



**PACKAGE DETAILS**

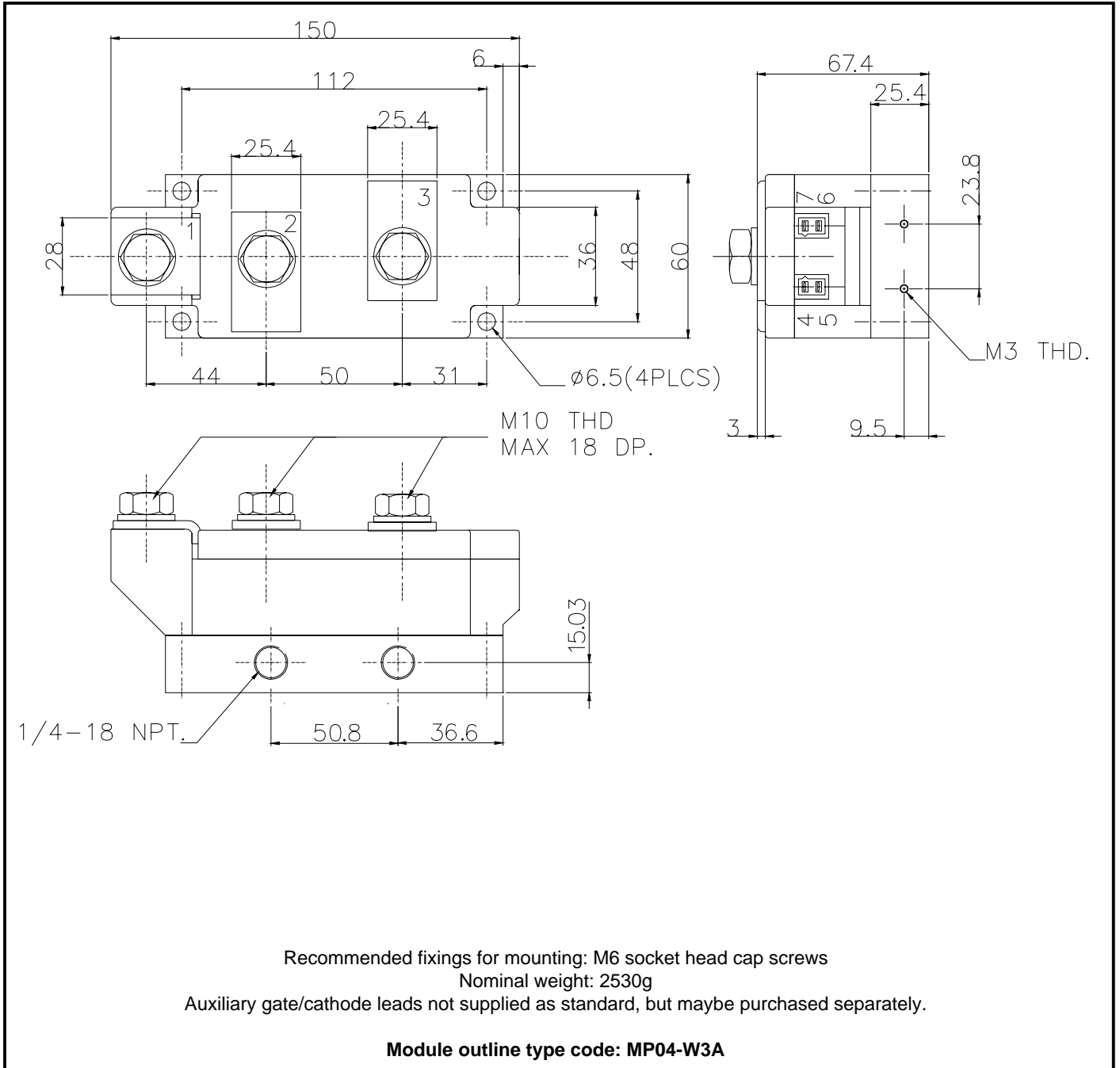
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The Power Assembly group provides support for those customers requiring more than the basic semiconductor switch. Using CAD design tools the group has developed a flexible range of heatsink / clamping systems in line with advances in device types and the voltage and current capability of Dynex semiconductors.

An extensive range of air and liquid cooled assemblies is available covering the range of circuit designs in general use today.

## HEATSINKS

The Power Assembly group has a proprietary range of extruded aluminium heatsinks. These were designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or customer service office.



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