HB52E649E12-A6B/B6B

512 MB Registered SDRAM DIMM
64-Mword × 72-bit, 100 MHz Memory Bus, 1-Bank Module
(18 pcs of 64 M × 4 Components)
PC100 SDRAM

E0020H20 (Ver. 2.0)
Aug. 20, 2001 (K)

Description

The HB52E649E12 belongs to 8-byte DIMM (Dual In-line Memory Module) family, and has been developed as an optimized main memory solution for 8-byte processor applications. The HB52E649E12 is a 64M × 72 × 1-bank Synchronous Dynamic RAM Registered Module, mounted 18 pieces of 256-Mbit SDRAM (HM5225405BTT) sealed in TSOP package, 1 piece of PLL clock driver, 2 pieces of register driver and 1 piece of serial EEPROM (2-kbit) for Presence Detect (PD). An outline of the HB52E649E12 is 168-pin socket type package (dual lead out). Therefore, the HB52E649E12 makes high density mounting possible without surface mount technology. The HB52E649E12 provides common data inputs and outputs. Decoupling capacitors are mounted beside each TSOP on the module board.

Features

- Fully compatible with : JEDEC standard outline 8-byte DIMM
  : Intel PCB Reference design (Rev.1.2)
- 168-pin socket type package (dual lead out)
  - Outline: 133.37 mm (Length) × 43.18 mm (Height) × 4.00 mm (Thickness)
  - Lead pitch: 1.27 mm
- 3.3 V power supply
- Clock frequency: 100 MHz (max)
- LVTTL interface
- Data bus width: × 72 ECC
- Single pulsed $\overline{RAS}$
- 4 Banks can operates simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length: 1/2/4/8
- 2 variations of burst sequence
  - Sequential

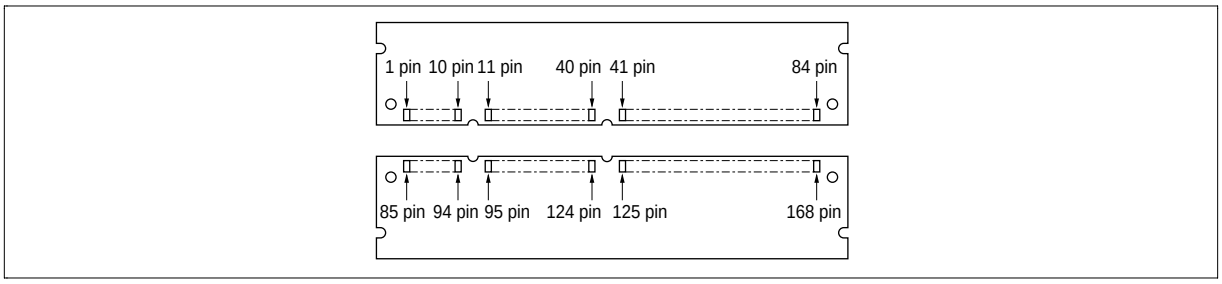
— Interleave

- Programmable $\overline{CE}$ latency : 3/4 (HB52E649E12-A6B)
  : 4 (HB52E649E12-B6B)
- Byte control by DQMB
- Refresh cycles: 8192 refresh cycles/64 ms
- 2 variations of refresh
  — Auto refresh
  — Self refresh

Ordering Information

Type No.	Frequency	$\overline{CE}$ latency	Package	Contact pad
HB52E649E12-A6B	100 MHz	3/4	168-pin dual lead out socket type	Gold
HB52E649E12-B6B	100 MHz	4		

Pin Arrangement



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	$\overline{S2}$	87	DQ33	129	NC
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V_{CC}	48	NC	90	V_{CC}	132	NC
7	DQ4	49	V_{CC}	91	DQ36	133	V_{CC}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{CC}	101	DQ45	143	V_{CC}
18	V_{CC}	60	DQ20	102	V_{CC}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	NC	105	CB4	147	REGE
22	CB1	64	V_{SS}	106	CB5	148	V_{SS}
23	V_{SS}	65	DQ21	107	V_{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V_{CC}	68	V_{SS}	110	V_{CC}	152	V_{SS}
27	$\overline{W}$	69	DQ24	111	$\overline{CE}$	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	$\overline{S0}$	72	DQ27	114	NC	156	DQ59
31	NC	73	V_{CC}	115	$\overline{RE}$	157	V_{CC}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	CK2	121	A9	163	CK3
38	A10 (AP)	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	V_{CC}	82	SDA	124	V_{CC}	166	SA1
41	V_{CC}	83	SCL	125	CK1	167	SA2
42	CK0	84	V_{CC}	126	A12	168	V_{CC}

Pin Description

Pin name	Function
A0 to A12	Address input — Row address A0 to A12 — Column address A0 to A9, A11
BA0/BA1	Bank select address
DQ0 to DQ63	Data input/output
CB0 to CB7	Check bit (Data input/output)
$\overline{S0}$, $\overline{S2}$	Chip select input
$\overline{RE}$	Row enable (RAS) input
$\overline{CE}$	Column enable (CAS) input
$\overline{W}$	Write enable input
DQMB0 to DQMB7	Byte data mask
CK0 to CK3	Clock input
CKE0	Clock enable input
WP	Write protect for serial PD
REGE*[1]	Register/Buffer enable
SDA	Data input/output for serial PD
SCL	Clock input for serial PD
SA0 to SA2	Serial address input
V_{CC}	Primary positive power supply
V_{SS}	Ground
NC	No connection

Note: 1. REGE $\geq V_{IH}$: Register mode.
REGE $\leq V_{IL}$: Buffer mode.

Serial PD Matrix*[1]

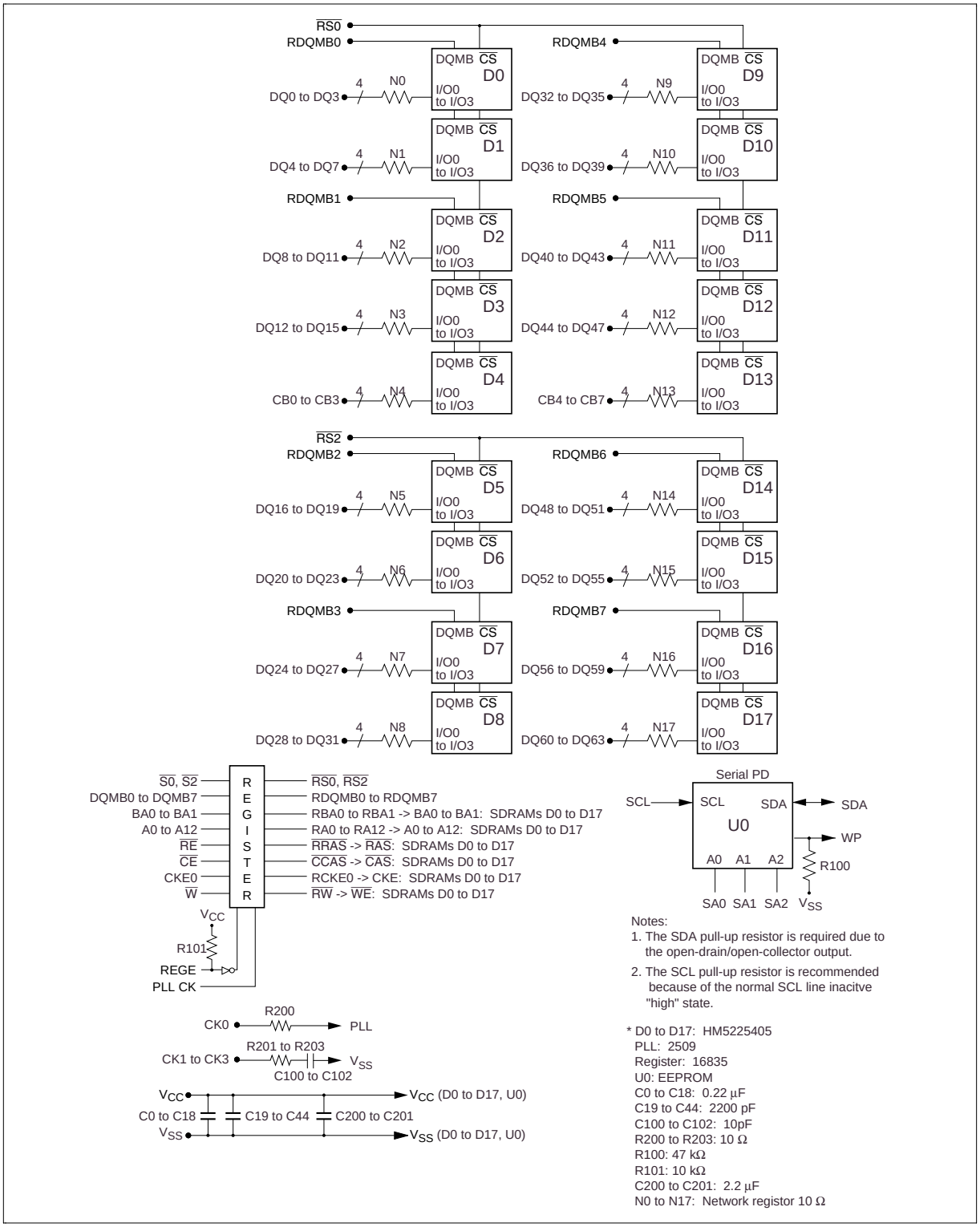
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes used by module manufacturer	1	0	0	0	0	0	0	0	80	128
1	Total SPD memory size	0	0	0	0	1	0	0	0	08	256 byte
2	Memory type	0	0	0	0	0	1	0	0	04	SDRAM
3	Number of row addresses bits	0	0	0	0	1	1	0	1	0D	13
4	Number of column addresses bits	0	0	0	0	1	0	1	1	0B	11
5	Number of banks	0	0	0	0	0	0	0	1	01	1
6	Module data width	0	1	0	0	1	0	0	0	48	72 bit
7	Module data width (continued)	0	0	0	0	0	0	0	0	00	0 (+)
8	Module interface signal levels	0	0	0	0	0	0	0	1	01	LVTTL
9	SDRAM cycle time (highest $\overline{CE}$ latency) 10 ns	1	0	1	0	0	0	0	0	A0	CL = 3
10	SDRAM access from Clock (highest $\overline{CE}$ latency) 6 ns	0	1	1	0	0	0	0	0	60	*[7]
11	Module configuration type	0	0	0	0	0	0	1	0	02	ECC
12	Refresh rate/type	1	0	0	0	0	0	1	0	82	Normal (7.8125 µs) Self refresh
13	SDRAM width	0	0	0	0	0	1	0	0	04	64M × 4
14	Error checking SDRAM width	0	0	0	0	0	1	0	0	04	× 4
15	SDRAM device attributes: minimum clock delay for back-to-back random column addresses	0	0	0	0	0	0	0	1	01	1 CLK
16	SDRAM device attributes: Burst lengths supported	0	0	0	0	1	1	1	1	0F	1, 2, 4, 8
17	SDRAM device attributes: number of banks on SDRAM device	0	0	0	0	0	1	0	0	04	4
18	SDRAM device attributes: $\overline{CE}$ latency (-A6B)	0	0	0	0	0	1	1	0	06	2/3
	(-B6B)	0	0	0	0	0	1	0	0	04	3
19	SDRAM device attributes: $\overline{S}$ latency	0	0	0	0	0	0	0	1	01	0
20	SDRAM device attributes: $\overline{W}$ latency	0	0	0	0	0	0	0	1	01	0
21	SDRAM device attributes	0	0	0	1	1	1	1	1	1F	Registered

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
22	SDRAM device attributes: General	0	0	0	0	1	1	1	0	0E	V_{CC} ± 10%
23	SDRAM cycle time (2nd highest $\overline{CE}$ latency) (-A6B) 10 ns	1	0	1	0	0	0	0	0	A0	CL = 2 *7
	(-B6B) Undefined	0	0	0	0	0	0	0	0	00	
24	SDRAM access from Clock (2nd highest $\overline{CE}$ latency) (-A6B) 6 ns	0	1	1	0	0	0	0	0	60	
	(-B6B) Undefined	0	0	0	0	0	0	0	0	00	
25	SDRAM cycle time (3rd highest $\overline{CE}$ latency) Undefined	0	0	0	0	0	0	0	0	00	
26	SDRAM access from Clock (3rd highest $\overline{CE}$ latency) Undefined	0	0	0	0	0	0	0	0	00	
27	Minimum row precharge time	0	0	0	1	0	1	0	0	14	20 ns
28	Row active to row active min	0	0	0	1	0	1	0	0	14	20 ns
29	$\overline{RE}$ to $\overline{CE}$ delay min	0	0	0	1	0	1	0	0	14	20 ns
30	Minimum $\overline{RE}$ pulse width	0	0	1	1	0	0	1	0	32	50 ns
31	Density of each bank on module	1	0	0	0	0	0	0	0	80	1 bank 512M byte
32	Address and command signal input setup time	0	0	1	0	0	0	0	0	20	2 ns*7
33	Address and command signal input hold time	0	0	0	1	0	0	0	0	10	1 ns*7
34	Data signal input setup time	0	0	1	0	0	0	0	0	20	2 ns*7
35	Data signal input hold time	0	0	0	1	0	0	0	0	10	1 ns*7
36 to 61	Superset information	0	0	0	0	0	0	0	0	00	Future use
62	SPD data revision code	0	0	0	1	0	0	1	0	12	Rev. 1.2A
63	Checksum for bytes 0 to 62 (-A6B)	0	0	1	0	0	0	1	1	23	35
	(-B6B)	0	0	1	0	0	0	0	1	21	33
64	Manufacturer's JEDEC ID code	0	0	0	0	0	1	1	1	07	HITACHI
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00	
72	Manufacturing location	×	×	×	×	×	×	×	×	××	*3 (ASCII-8bit code)
73	Manufacturer's part number	0	1	0	0	1	0	0	0	48	H
74	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
75	Manufacturer's part number	0	0	1	1	0	1	0	1	35	5
76	Manufacturer's part number	0	0	1	1	0	0	1	0	32	2

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
77	Manufacturer's part number	0	1	0	0	0	1	0	1	45	E
78	Manufacturer's part number	0	0	1	1	0	1	1	0	36	6
79	Manufacturer's part	0	0	1	1	0	1	0	0	34	4
80	Manufacturer's part number	0	0	1	1	1	0	0	1	39	9
81	Manufacturer's part number	0	1	0	0	0	1	0	1	45	E
82	Manufacturer's part number	0	0	1	1	0	0	0	1	31	1
83	Manufacturer's part number	0	0	1	1	0	0	1	0	32	2
84	Manufacturer's part number	0	0	1	0	1	1	0	1	2D	—
85	Manufacturer's part number (-A6B)	0	1	0	0	0	0	0	1	41	A
	(-B6B)	0	1	0	0	0	0	1	0	42	B
86	Manufacturer's part number	0	0	1	1	0	1	1	0	36	6
87	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
88	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
89	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
90	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30	Initial
92	Revision code	0	0	1	0	0	0	0	0	20	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	××	Year code (BCD)*[4]
94	Manufacturing date	×	×	×	×	×	×	×	×	××	Week code (BCD)*[4]
95 to 98	Assembly serial number	*[6]									
99 to 125	Manufacturer specific data	—	—	—	—	—	—	—	—	—	*[5]
126	Intel specification frequency	0	1	1	0	0	1	0	0	64	100 MHz
127	Intel specification $\overline{CE}$# latency support (-A6B)	1	0	0	0	0	1	1	1	87	CL = 2/3
	(-B6B)	1	0	0	0	0	1	0	1	85	CL = 3

Notes:
1. All serial PD data are not protected. 0: Serial data, "driven Low", 1: Serial data, "driven High" These SPD are based on Intel specification (Rev.1.2A).
2. Regarding byte32 to 35, based on JEDEC Committee Ballot JC42.5-97-119.
3. Byte72 is manufacturing location code. (ex: In case of Japan, byte72 is 4AH. 4AH shows "J" on ASCII code.)
4. Regarding byte93 and 94, based on JEDEC Committee Ballot JC42.5-97-135. BCD is "Binary Coded Decimal".
5. All bits of 99 through 125 are not defined ("1" or "0").
6. Bytes 95 through 98 are assembly serial number.
7. These specifications are defined based on component specification, not module.

Block Diagram



Notes:
1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacitve "high" state.

* D0 to D17: HM5225405
PLL: 2509
Register: 16835
U0: EEPROM
C0 to C18: 0.22 µF
C19 to C44: 2200 pF
C100 to C102: 10pF
R200 to R203: 10 Ω
R100: 47 kΩ
R101: 10 kΩ
C200 to C201: 2.2 µF
N0 to N17: Network registor 10 Ω

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	–0.5 to V_{CC} + 0.5 (≤ 4.6 (max))	V	1
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +4.6	V	1
Short circuit output current	Iout	50	mA	
Power dissipation	P_T	18.0	W	
Operating temperature	Topr	0 to +55	°C	
Storage temperature	Tstg	–50 to +100	°C	

Note: 1. Respect to V_{SS}

DC Operating Conditions (Ta = 0 to +55°C)

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage	V_{CC}	3.0	3.6	V	1, 2
	V_{SS}	0	0	V	3
Input high voltage	V_{IH}	2.0	V_{CC}	V	1, 4
Input low voltage	V_{IL}	0	0.8	V	1, 5

Notes: 1. All voltage referred to V_{SS}
2. The supply voltage with all V_{CC} pins must be on the same level.
3. The supply voltage with all V_{SS} pins must be on the same level.
4. V_{IH} (max) = V_{CC} + 2.0 V for pulse width ≤ 3 ns at V_{CC}.
5. V_{IL} (min) = V_{SS} – 2.0 V for pulse width ≤ 3 ns at V_{SS}.

DC Characteristics (Ta = 0 to 55°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

		HB52E649E12						
		-A6B		-B6B				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current ($\overline{CE}$ latency = 3)	I_{CC1}	—	2220	—	—	mA	Burst length = 1 t_{RC} = min	1, 2, 3
($\overline{CE}$ latency = 4)	I_{CC1}	—	2220	—	2220	mA		
Standby current in power down	I_{CC2P}	—	564	—	564	mA	CKE = V_{IL}, t_{CK} = 12 ns	6
Standby current in power down (input signal stable)	I_{CC2PS}	—	546	—	546	mA	CKE = V_{IL}, t_{CK} = ∞	7
Standby current in non power down	I_{CC2N}	—	870	—	870	mA	CKE, $\overline{S}$ = V_{IH}, t_{CK} = 12 ns	4
Active standby current in power down	I_{CC3P}	—	582	—	582	mA	CKE = V_{IL}, t_{CK} = 12 ns	1, 2, 6
Active standby current in non power down	I_{CC3N}	—	1050	—	1050	mA	CKE, $\overline{S}$ = V_{IH}, t_{CK} = 12 ns	1, 2, 4
Burst operating current ($\overline{CE}$ latency = 3)	I_{CC4}	—	2220	—	—	mA	t_{CK} = min, BL = 4	1, 2, 5
($\overline{CE}$ latency = 4)	I_{CC4}	—	2220	—	2220	mA		
Refresh current	I_{CC5}	—	4470	—	4470	mA		
Self refresh current	I_{CC6}	—	564	—	564	mA	$V_{IH} \geq V_{CC}$ – 0.2 V $V_{IL} \leq$ 0.2 V	8
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 ≤ Vin ≤ V_{CC}	
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 ≤ Vout ≤ V_{CC} DQ = disable	
Output high voltage	V_{OH}	2.4	—	2.4	—	V	I_{OH} = –4 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	V	I_{OL} = 4 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signals are changed once per one clock.
4. Input signals are changed once per two clocks.
5. Input signals are changed once per four clocks.
6. After power down mode, CK operating current.
7. After power down mode, no CK operating current.
8. After self refresh mode set, self refresh current.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	Symbol	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	15	pF	1, 2, 4
Input capacitance ($\overline{RE}$, $\overline{CE}$, $\overline{W}$)	C_{I2}	15	pF	1, 2, 4
Input capacitance (CKE)	C_{I3}	23	pF	1, 2, 4
Input capacitance ($\overline{S}$)	C_{I4}	15	pF	1, 2, 4
Input capacitance (CK)	C_{I5}	40	pF	1, 2, 4
Input capacitance (DQMB)	C_{I6}	15	pF	1, 2, 4
Input/Output capacitance (DQ)	$C_{I/O1}$	15	pF	1, 2, 3, 4

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. Measurement condition: f = 1 MHz, 1.4 V bias, 200 mV swing.
3. DQMB = V_{IH} to disable Data-out.
4. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 55°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

			HB52E649E12 -A6B/B6B			
Parameter	Symbol	PC100 Symbol	Min	Max	Unit	Notes
System clock cycle time ($\overline{CE}$ latency = 3)	t_{CK}	Tclk	10	—	ns	1
($\overline{CE}$ latency = 4)	t_{CK}	Tclk	10	—	ns	
CK high pulse width	t_{CKH}	Tch	4	—	ns	1
CK low pulse width	t_{CKL}	Tcl	4	—	ns	1
Access time from CK ($\overline{CE}$ latency = 3)	t_{AC}	Tac	—	6.9	ns	1, 2
($\overline{CE}$ latency = 4)	t_{AC}	Tac	—	6.9	ns	
Data-out hold time	t_{OH}	Toh	2.1	—	ns	1, 2
CK to Data-out low impedance	t_{LZ}		1.1	—	ns	1, 2, 3
CK to Data-out high impedance	t_{HZ}		—	6.9	ns	1, 4
Data-in setup time	t_{DS}	Tsi	2.9	—	ns	1
Data in hold time	t_{DH}	Thi	1.9	—	ns	1
Address setup time	t_{AS}	Tsi	2.6	—	ns	1
Address hold time	t_{AH}	Thi	1.6	—	ns	1, 5
CKE setup time	t_{CES}	Tsi	2.6	—	ns	1, 5
CKE setup time for power down exit	t_{CESP}	Tpde	2.6	—	ns	1
CKE hold time	t_{CEH}	Thi	1.6	—	ns	1

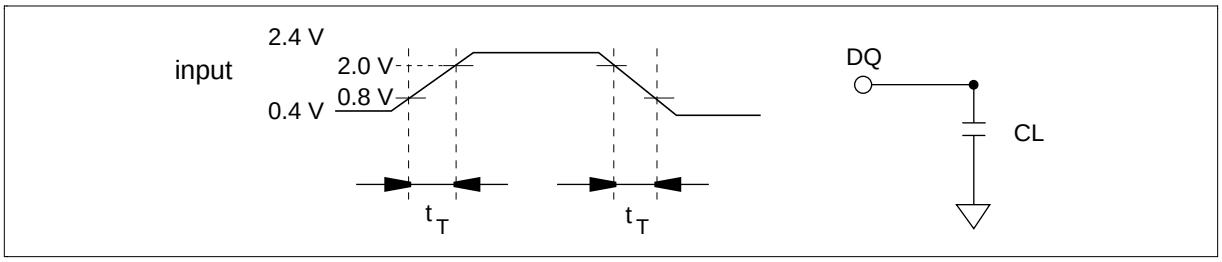
AC Characteristics (Ta = 0 to 55°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (cont)

			HB52E649E12 -A6B/B6B			
Parameter	**Symbol**	**PC100 Symbol**	**Min**	**Max**	**Unit**	**Notes**
Command setup time	t_{CS}	Tsi	2.6	—	ns	1
Command hold time	t_{CH}	Thi	1.6	—	ns	1
Ref/Active to Ref/Active command period	t_{RC}	Trc	70	—	ns	1
Active to precharge command period	t_{RAS}	Tras	50	120000	ns	1
Active command to column command (same bank)	t_{RCD}	Trcd	20	—	ns	1
Precharge to active command period	t_{RP}	Trp	20	—	ns	1
Write recovery or data-in to precharge lead time	t_{DPL}	Tdpl	10	—	ns	1
Active (a) to Active (b) command period	t_{RRD}	Trrd	20	—	ns	1
Transition time (rise to fall)	t_T		1	5	ns	
Refresh period	t_{REF}		—	64	ms	

Notes: 1. AC measurement assumes t_T = 1 ns. Reference level for timing of input signals is 1.5 V.
2. Access time is measured at 1.5 V. Load condition is C_L = 50 pF.
3. t_{LZ} (min) defines the time at which the outputs achieves the low impedance state.
4. t_{HZ} (max) defines the time at which the outputs achieves the high impedance state.
5. t_{CES} defines CKE setup time to CK rising edge except power down exit command.

Test Conditions

- Input and output timing reference levels: 1.5 V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

Parameter			HB52E649E12	
Frequency (MHz)			**-A6B/B6B**	
t_{CK} (ns)	**Symbol**	**PC100 Symbol**	**10**	**Notes**
Active command to column command (same bank)	I_{RCD}		2	1
Active command to active command (same bank)	I_{RC}		7	= [I_{RAS} + I_{RP}] 1
Active command to precharge command (same bank)	I_{RAS}		5	1
Precharge command to active command (same bank)	I_{RP}		2	1
Write recovery or data-in to precharge command (same bank)	I_{DPL}	Tdpl	1	1
Active command to active command (different bank)	I_{RRD}		2	1
Self refresh exit time	I_{SREX}	Tsrx	2	2
Last data in to active command (Auto precharge, same bank)	I_{APW}	Tdal	3	= [I_{DPL} + I_{RP}]
Self refresh exit to command input	I_{SEC}		7	= [I_{RC}] 3
Precharge command to high impedance ($\overline{CE}$ latency = 3)	I_{HZP}	Troh	3	
($\overline{CE}$ latency = 4)	I_{HZP}	Troh	4	
Last data out to active command (auto precharge) (same bank)	I_{APR}		0	
Last data out to precharge (early precharge) ($\overline{CE}$ latency = 3)	I_{EP}		–2	
($\overline{CE}$ latency = 4)	I_{EP}		–3	
Column command to column command	I_{CCD}	Tccd	1	
Write command to data in latency	I_{WCD}	Tdwd	1	
DQMB to data in	I_{DID}	Tdqm	1	
DQMB to data out	I_{DOD}	Tdqz	3	
CKE to CK disable	I_{CLE}	Tcke	2	
Register set to active command	I_{RSA}	Tmrd	1	
$\overline{S}$ to command disable	I_{CDD}		0	
Power down exit to command input	I_{PEC}		1	

Notes: 1. I_{RCD} to I_{RRD} are recommended value.
2. Be valid [DESL] or [NOP] at next command of self refresh exit.
3. Except [DESL] and [NOP]

Pin Functions

CK0 to CK3 (input pin): CK is the master clock input to this pin. The other input signals are referred at CK rising edge.

$\overline{S0}$, $\overline{S2}$ (input pin): When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

$\overline{RE}$, $\overline{CE}$ and $\overline{W}$ (input pins): Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.

A0 to A12 (input pins): Row address (AX0 to AX12) is determined by A0 to A12 level at the bank active command cycle CK rising edge. Column address (AY0 to AY9, AY11) is determined by A0 to A9, A11 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, all banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0/BA1 (BA) is precharged.

BA0/BA1 (input pin): BA0/BA1 are bank select signal (BA). The memory array is divided into bank 0, bank 1, bank 2 and bank 3. If BA0 is Low and BA1 is Low, bank 0 is selected. If BA0 is High and BA1 is Low, bank 1 is selected. If BA0 is Low and BA1 is High, bank 2 is selected. If BA0 is High and BA1 is High, bank 3 is selected.

CKE0 (input pin): This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.

DQMB0 to DQMB7 (input pins): Read operation: If DQMB is High, the output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z.

Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.

DQ0 to DQ63, CB0 to CB7 (input/output pins): Data is input to and output from these pins.

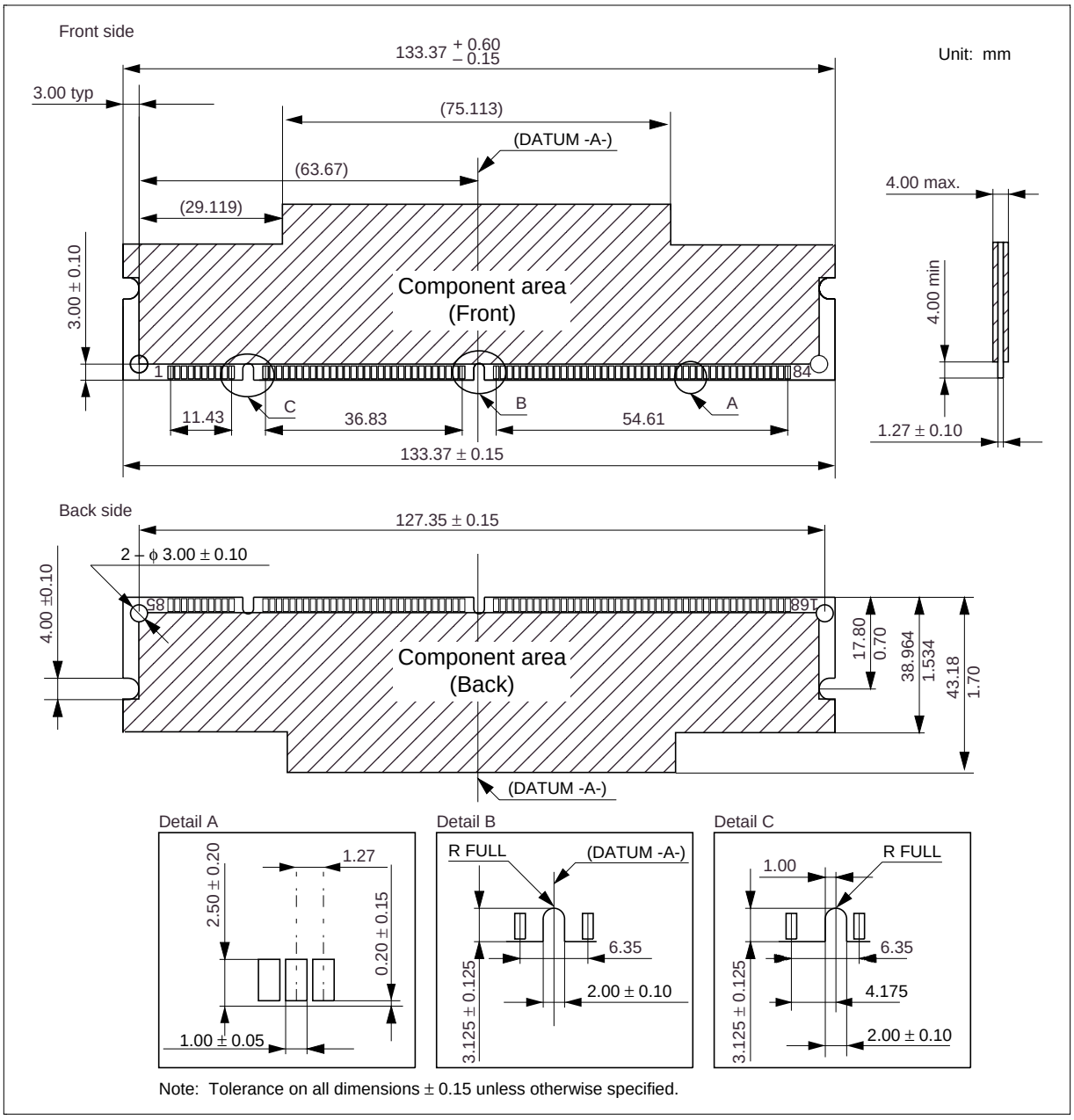
V_{CC} (power supply pins): 3.3 V is applied.

V_{SS} (power supply pins): Ground is connected.

Detailed Operation Part

Refer to the HM5225165B/HM5225805B/HM5225405B-75/A6/B6 datasheet (E0082H).

Physical Outline



Note: Tolerance on all dimensions ± 0.15 unless otherwise specified.

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