

## Features

- ESD protect for 4 high-speed I/O channels
- Provide transient protection for each channel to  
IEC 61000-4-2 (ESD)  $\pm 30\text{kV}$  (air / contact)  
IEC 61000-4-4 (EFT) 80A (5/50ns)  
IEC 61000-4-5 (Lightning) 20A (8/20 $\mu\text{s}$ ) for any  
I/O-to-GND  
IEC 61000-4-5 (Lightning) 70A (8/20 $\mu\text{s}$ ) for  
VDD-to-GND
- For low operating voltage applications: 5V  
maximum
- Low capacitance : 1.8pF typical
- Fast turn-on and low clamping voltage
- Array of surge rated diodes with internal  
equivalent TVS diode
- Small package saves board space
- Solid-state silicon-avalanche and active circuit  
triggering technology
- **Green part**

## Applications

- Video graphics cards
- LAN application
- USB2.0 power and data lines protection
- Notebook and PC computers
- Monitors and flat panel displays

## Description

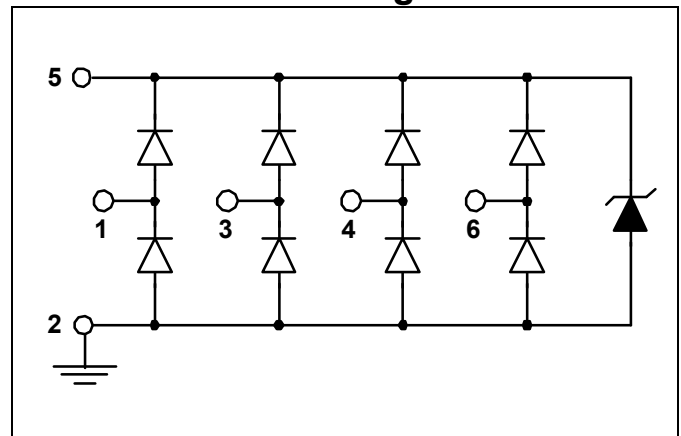
AZ1575-04S is a high-performance design which includes surge rated diode arrays to protect high-speed data interfaces. The AZ1575-04S has been specifically designed to protect sensitive components, which are connected to data and transmission lines, from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

AZ1575-04S is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct

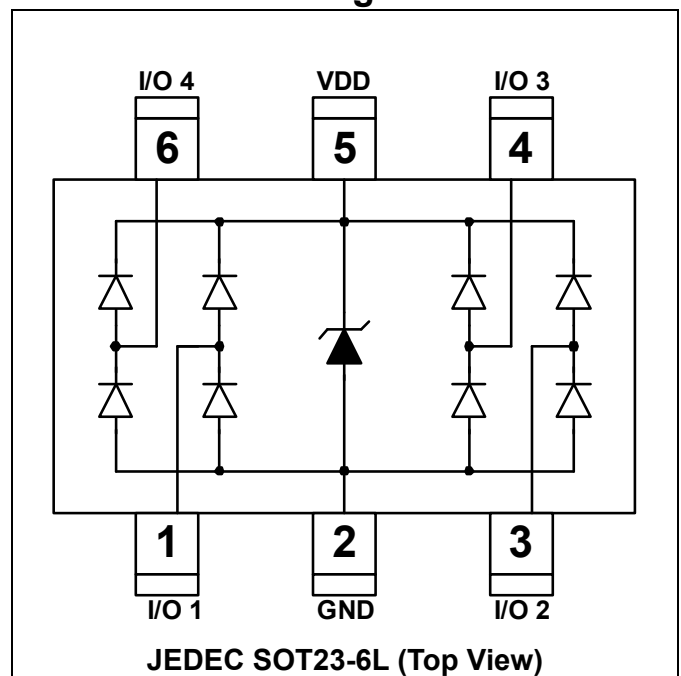
the transient to either the power supply line or to the ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components.

AZ1575-04S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ( $\pm 15\text{kV}$  air,  $\pm 8\text{kV}$  contact discharge).

## Circuit Diagram



## Pin Configuration



## Specifications

Absolute Maximum Ratings (T <sub>A</sub> = 25°C, unless otherwise specified)			
Parameter	Symbol	Rating	Unit
Peak Pulse Current (t <sub>p</sub> = 8/20μs, I/O-to-GND)	I <sub>PP-1</sub>	20	A
Peak Pulse Current (t <sub>p</sub> = 8/20μs, VDD-to-GND)	I <sub>PP-2</sub>	70	A
Operating Voltage (VDD-to-GND)	V <sub>DC</sub>	5.5	V
ESD per IEC 61000-4-2 (Air / Contact)	V <sub>ESD</sub>	±30	kV
Lead Soldering Temperature	T <sub>SOL</sub>	260 (10 sec.)	°C
Operating Temperature	T <sub>OP</sub>	-55 to +125	°C
Storage Temperature	T <sub>STO</sub>	-55 to +150	°C

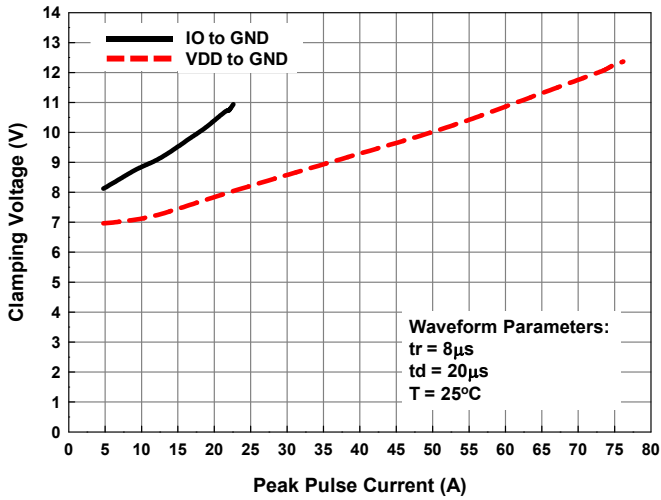
Electrical Characteristics						
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V <sub>RWM</sub>	Pin-5 to pin-2, T = 25 °C.			5	V
Reverse Leakage Current	I <sub>Leak</sub>	V <sub>RWM</sub> = 5V, T = 25 °C, pin-5 to pin-2.			1	μA
Channel Leakage Current	I <sub>CH-Leak</sub>	V <sub>pin-5</sub> = 5V, V <sub>pin-2</sub> = 0V, T = 25 °C, any I/O pin to GND.			1	μA
Reverse Breakdown Voltage	V <sub>BV</sub>	I <sub>BV</sub> = 1mA, T = 25 °C, pin-5 to pin-2.	5.8		8.5	V
Forward Voltage	V <sub>F</sub>	I <sub>F</sub> = 15mA, T = 25 °C, pin-2 to pin-5.	0.6		1.2	V
ESD Clamping Voltage –I/O (Note 1)	V <sub>CL_ESD_I/O</sub>	IEC 61000-4-2 +8kV (I <sub>TLP</sub> = 16A), T = 25 °C, contact mode, any I/O pin to GND.		10		V
ESD Clamping Voltage –VDD (Note 1)	V <sub>CL_ESD_VDD</sub>	IEC 61000-4-2 +8kV (I <sub>TLP</sub> = 16A), T = 25 °C, contact mode, VDD pin to GND.		8		V
ESD Dynamic Turn on Resistance –I/O	R <sub>dynamic_I/O</sub>	IEC 61000-4-2, 0~+8kV, T=25 °C, contact mode, any I/O pin to GND.		0.14		Ω
ESD Dynamic Turn on Resistance –VDD	R <sub>dynamic_VDD</sub>	IEC 61000-4-2, 0~+8kV, T=25 °C, contact mode, VDD pin to GND.		0.05		Ω
Surge Clamping Voltage –I/O	V <sub>CL_surge_I/O</sub>	I <sub>PP</sub> =20A, t <sub>p</sub> =8/20μs, T = 25 °C, any I/O pin to GND.		11		V
Surge Clamping Voltage –VDD	V <sub>CL_surge_VDD</sub>	I <sub>PP</sub> =70A, t <sub>p</sub> =8/20μs, T = 25 °C, VDD pin to GND.		12		V
Channel Input Capacitance	C <sub>IN</sub>	V <sub>pin-5</sub> = 5V, V <sub>pin-2</sub> = 0V, V <sub>IN</sub> = 2.5V, f = 1MHz, T = 25 °C, any I/O pin to GND.		1.8	2.5	pF
		V <sub>pin-5</sub> = floated, V <sub>pin-2</sub> = 0V, V <sub>IN</sub> = 2.5V, f = 1MHz, T = 25 °C, any I/O pin to GND.		2.3	3	pF
Channel to Channel Capacitance	C <sub>I/O-to-I/O</sub>	V <sub>IN</sub> = 2.5V, f = 1MHz, T = 25 °C, between I/O pins.		1.3	1.8	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

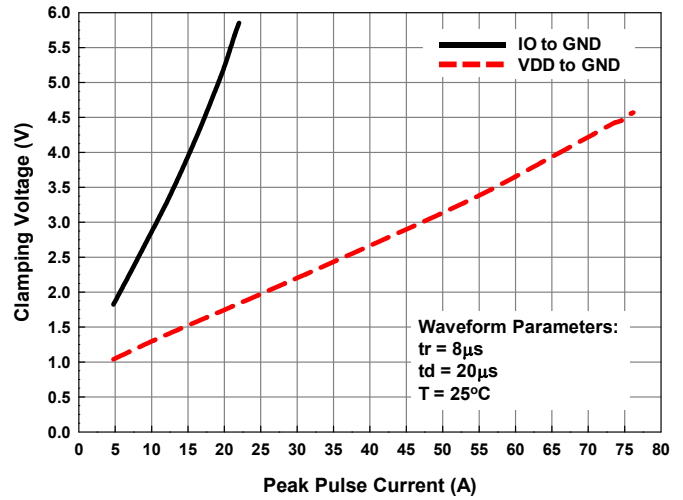
TLP conditions: Z<sub>0</sub> = 50Ω, t<sub>p</sub> = 100ns, t<sub>r</sub> = 1ns.

## Typical Characteristics

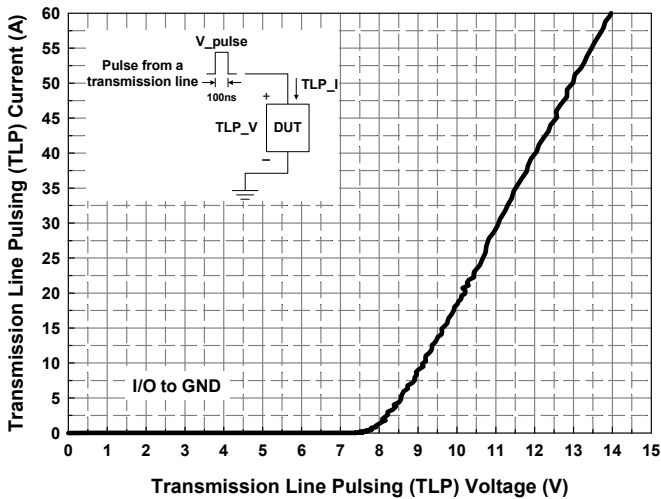
Reverse Clamping Voltage vs. Peak Pulse Current



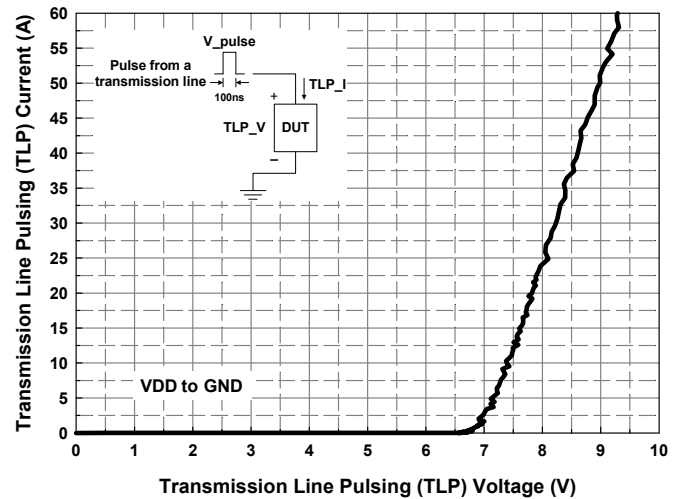
Forward Clamping Voltage vs. Peak Pulse Current



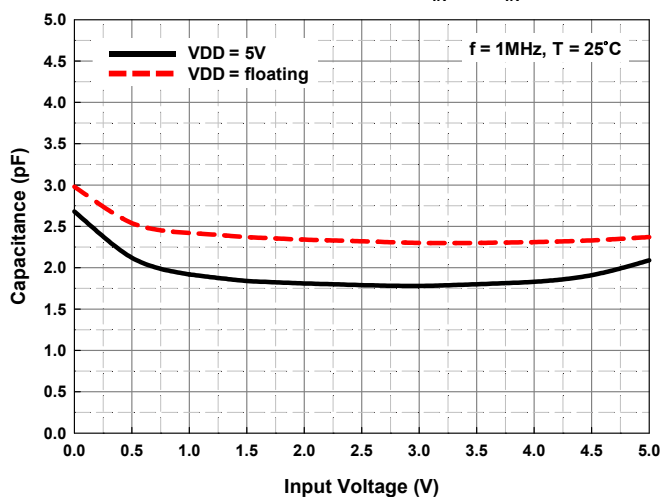
Transmission Line Pulsing (TLP) Measurement



Transmission Line Pulsing (TLP) Measurement



Typical Variation of  $C_{IN}$  vs.  $V_{IN}$



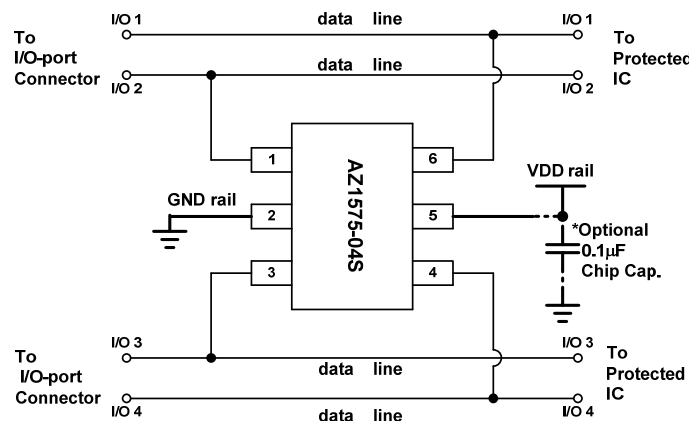
## Applications Information

The AZ1575-04S is designed to protect four data lines and power rails from transient over-voltage (such as ESD stress pulse). The device connection of AZ1575-04S is shown in the Fig. 1. In Fig. 1, the four protected data lines are connected to the ESD protection pins (pin-1, pin-3, pin-4, and pin-6) of AZ1575-04S. The ground pin (pin-2) of AZ1575-04S is a negative reference pin. This pin should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible. In addition, the power pin (pin-5) of AZ1575-04S is a positive reference pin. This pin should directly connect to the VDD rail of PCB., then the VDD rail also can be protected by the power-rail ESD clamped circuit (not shown) of AZ1575-04S.

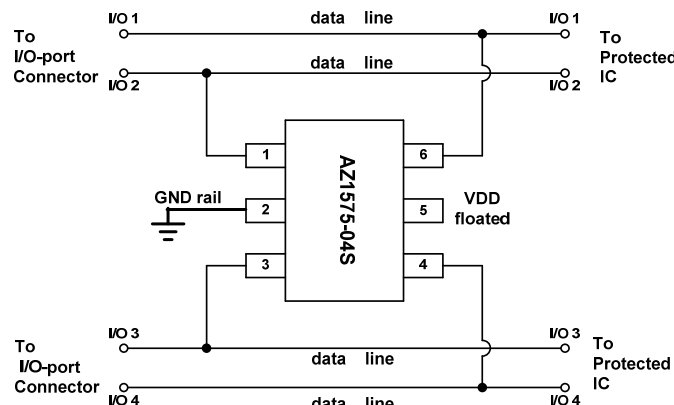
AZ1575-04S can provide protection for 4 I/O signal lines simultaneously. If the number of I/O signal lines is less than 4, the unused I/O pins can be simply left as NC pins.

In some cases, systems are not allowed to be reset or restart after the ESD stress directly applying at the I/O-port connector. Under this situation, in order to enhance the sustainable ESD level, a 0.1 $\mu$ F chip capacitor can be added between the VDD and GND rails. The place of this chip capacitor should be as close as possible to the AZ1575-04S.

In some cases, there isn't power rail presented on the PCB. Under this situation, the power pin (pin-5) of AZ1575-04S can be left as floated. The protection will not be affected, only the load capacitance of I/O pins will be slightly increased. Fig. 2 shows the detail connection.



**Fig. 1 Data lines and power rails connection of AZ1575-04S.**



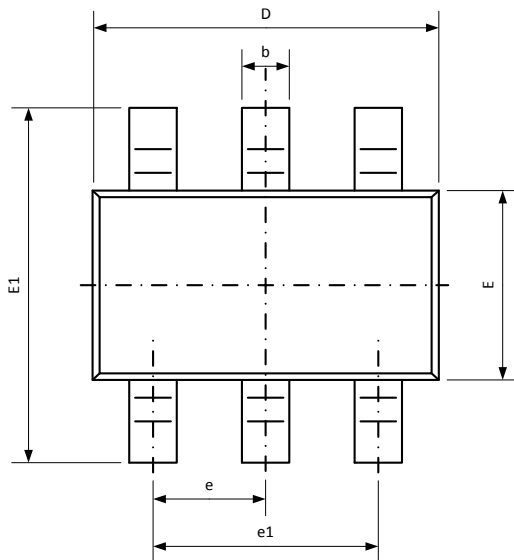
**Fig. 2 Data lines and power rails connection of AZ1575-04S. VDD pin is left as floating when no power rail presented on the PCB.**

## Mechanical Details

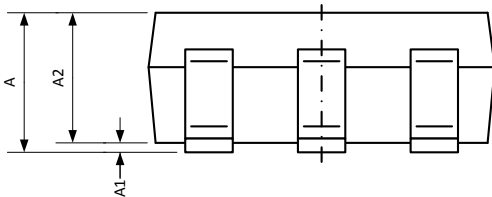
### SOT23-6L

#### Package Diagrams

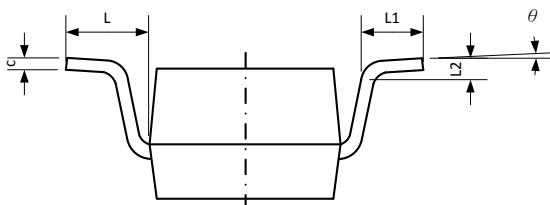
TOP VIEW



SIDE VIEW



END VIEW



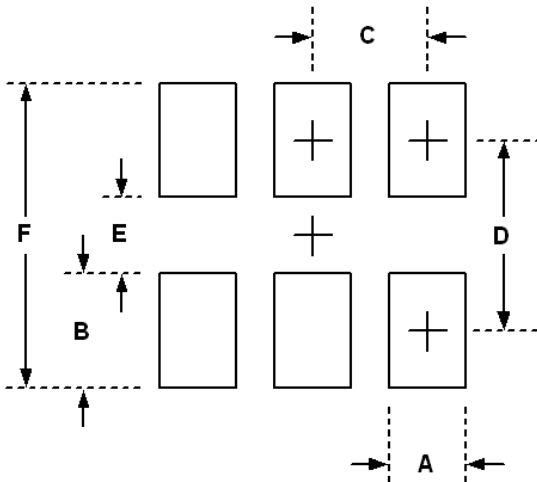
#### Package Dimensions

Symbol	Millimeters	
	Min.	Max.
<b>A</b>	-	1.25
<b>A1</b>	0.00	0.10
<b>A2</b>	0.90	1.20
<b>b</b>	0.30	0.50
<b>c</b>	0.08	0.21
<b>D</b>	2.72	3.12
<b>E</b>	1.40	1.80
<b>E1</b>	2.60	3.00
<b>e</b>	0.95 BSC	
<b>e1</b>	1.90 BSC	
<b>L1</b>	0.30	0.60
<b>L</b>	0.70 REF	
<b>L2</b>	0.25 BSC	
<b>θ</b>	0	8

#### Notes:

- This dimension complies with JEDEC outline standard MO-178 Variation AB.
- Dimensioning and tolerancing per ASME Y14.5M-1994.
- All dimensions are in millimeters.

## Land Layout

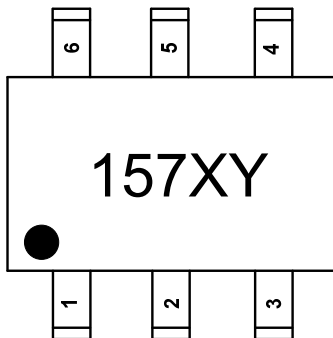


Dimensions		
Index	Millimeter	Inches
A	0.60	0.024
B	1.10	0.043
C	0.95	0.037
D	2.50	0.098
E	1.40	0.055
F	3.60	0.141

### Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

## Marking code



Part Number	Marking Code
AZ1575-04S.R7G (Green Part)	157XY

Note : Green means Pb-free, RoHS, and Halogen free compliant.

157 = Device Code  
X = Date Code  
Y = Control Code

## Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ1575-04S.R7G	Green	T/R	7 inch	3,000/reel	4 reels=12,000/box	6 boxes=72,000/carton



## Revision History

Revision	Modification Description
Revision 2021/04/28	Formal Release.