



## LR1143

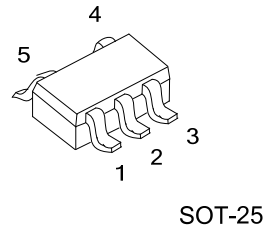
## LINEAR INTEGRATED CIRCUIT

### HIGH PSRR, LOW DROPOUT, 400mA ADJUSTABLE LDO REGULATOR

#### DESCRIPTION

The UTC **LR1143** is a CMOS-based 400mA voltage regulator with low supply current, low dropout, adjustable output voltage, The device offering high PSRR and low dropout. The quiescent current is as low as 35µA, further prolonging the battery life. The UTC **LR1143** also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in handheld wireless devices.

The UTC **LR1143** consumes typical 0.7µA in shutdown mode. The other features include low dropout voltage, high output accuracy, current limit protection, and enable/shutdown control.



#### FEATURES

- \* Wide operating voltage range : 3.0V~5.5V
- \* Adjustable output voltage
- \* Enable/shutdown control
- \* Low-noise for RF application
- \* Ultra-Fast response in line/load transient
- \* Current limit protection
- \* Output only 1µF capacitor required for stability
- \* High power supply rejection ratio

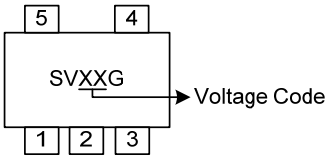
#### ORDERING INFORMATION

Ordering Number	Package	Packing
LR1143G-xx-AF5-R	SOT-25	Tape Reel

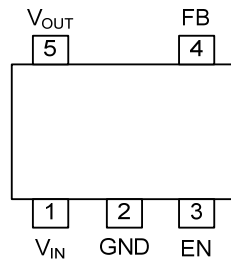
Note: xx: Output Voltage, refer to Marking Information.

LR1143G-xx-AF5-R	(1)Packing Type	(1) R: Tape Reel
	(2)Package Type	(2) AF5: SOT-25
	(3)Output Voltage Code	(3) xx: refer to Marking Information
	(4)Green Package	(4) G: Halogen Free and Lead Free

### MARKING INFORMATION

PACKAGE	VOLTAGE CODE	MARKING
SOT-25	AD: ADJ	

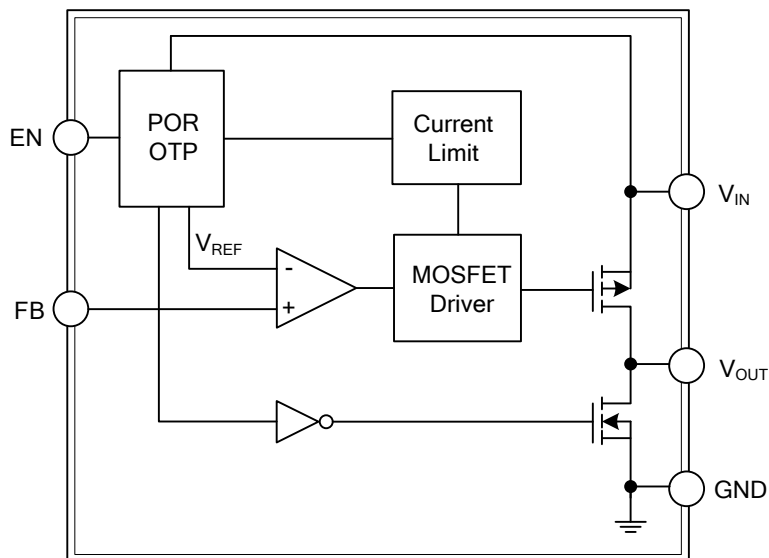
### PIN CONFIGURATION



### PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	$V_{IN}$	Voltage Input.
2	GND	Ground.
3	EN	Chip Enable (Active High).
4	FB	Output Voltage Feedback.
5	$V_{OUT}$	Voltage Output.

### BLOCK DIAGRAM



### ■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Input Voltage	$V_{IN}$	6	V
EN Input Voltage		6	V
Power Dissipation ( $T_A=25^\circ\text{C}$ )	$P_D$	0.4	W
Junction Temperature	$T_J$	150	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-65~+150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

### ■ RECOMMENDED OPERATING CONDITIONS (Note 3)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Ambient Temperature Range	$T_A$	-20		85	$^\circ\text{C}$

Note: The device is not guaranteed to function outside its operating conditions.

### ■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	260	$^\circ\text{C/W}$

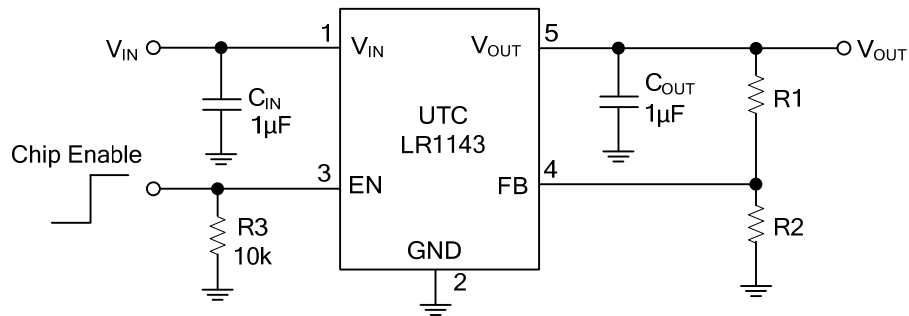
Note:  $\theta_{JA}$  is measured in the natural convection at  $T_A=25^\circ\text{C}$  on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

### ■ ELECTRICAL CHARACTERISTICS

( $V_{IN}=3.7\text{V}$ ,  $T_A=25^\circ\text{C}$ ,  $C_{IN}=C_{OUT}=1\mu\text{F}$ ,  $I_{OUT}=20\text{mA}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range	$V_{IN}$		3.0		5.5	V
Reference Voltage	$V_{REF}$		1.188	1.200	1.212	V
Quiescent Current	$I_Q$	$I_{OUT}=0\text{mA}$		35	50	$\mu\text{A}$
Shutdown Current	$I_{SHDN}$	$V_{EN}=0\text{V}$		0.7	1.5	$\mu\text{A}$
Current Limit	$I_{LIM}$	$3.0\text{V} \leq V_{IN} < 5.5\text{V}$	400	650		mA
Dropout Voltage	$V_{DROP}$	$I_{OUT}=400\text{mA}$		800		mV
Load Regulation	$\Delta V_{LOAD}$	$1\text{mA} < I_{OUT} < 400\text{mA}$ $3.0\text{V} \leq V_{IN} < 5.5\text{V}$			1	%
Line Regulation	$\Delta V_{LINE}$	$V_{IN}=(V_{OUT} + 0.5\text{V}) \sim 5.5\text{V}$ , $I_{OUT}=1\text{mA}$		0.01	0.2	%/V
EN Threshold	Logic-Low Voltage	$V_{IL}$	0		0.6	V
	Logic-High Voltage	$V_{IH}$	1.6		5.5	V
EN Pin Current	$I_{EN}$			0.1	1	$\mu\text{A}$
FB Pin Current	$I_{FB}$			0.1	1	$\mu\text{A}$
Power Supply Rejection Ratio	PSRR	$f=1\text{kHz}$ , $I_{OUT}=10\text{mA}$		67		dB
		$f=10\text{kHz}$ , $I_{OUT}=10\text{mA}$		56		dB
Output Noise Voltage	$V_{ON}$	$V_{OUT}=1.5\text{V}$ , $C_{OUT}=1\mu\text{F}$ , $I_{OUT}=0\text{mA}$		30		$\mu\text{V}_{RMS}$

### ■ TYPICAL APPLICATION CIRCUIT



$$V_{OUT} = V_{FB} \left(1 + \frac{R1}{R2}\right)$$

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