

One Cell Li-ion and Li-poly Battery Protection IC

Features

- Protection of Charger Reverse Connection
- Protection of Battery Cell Reverse Connection
- Over-temperature Protection
- Overcharge Current Protection
- Two-step Overcurrent Detection:
Over Discharge Current
Load Short Circuiting
- Charger Detection Function
- 0V Battery Charging Function
- RoHS Compliant and Lead (Pb) Free
- 50mΩ Low $R_{SS(ON)}$ Internal Power MOSFET
- Delay Times are generated inside
- High-accuracy Voltage Detection
- Low Current Consumption
Operation Mode: 3μA typ.
Power-down Mode: 2μA typ.
- Only One External Capacitor Required
- Available in SOT23-5 Package
- -40°C to +85°C Temperature Range

Applications

- One-Cell Li-ion Battery Pack
- Power Bank
- One-Cell Li-poly Battery Pack
- IOT Sensor/Electronic Toys

General Description

The J O 7656 is a high integration solution for lithium-ion/polymer battery protection. J O 7656 contains internal power MOSFET, high-accuracy voltage detection circuits and delay circuits. J O 7656 has all the protection functions required in the battery application including overcharging, over discharging, overcurrent and load short circuiting protection etc. The accurate overcharging detection voltage ensures safe and full utilization charging. The low standby current drains little current from the cell while in storage. The device is not only targeted for digital cellular phones, but also for any other Li-Ion and Li-Poly battery-powered information appliances requiring long-term battery life.

The J O 7656 requires a minimal number of readily available, external components and is available in a space saving SOT23-5 package.

Typical Application Circuit

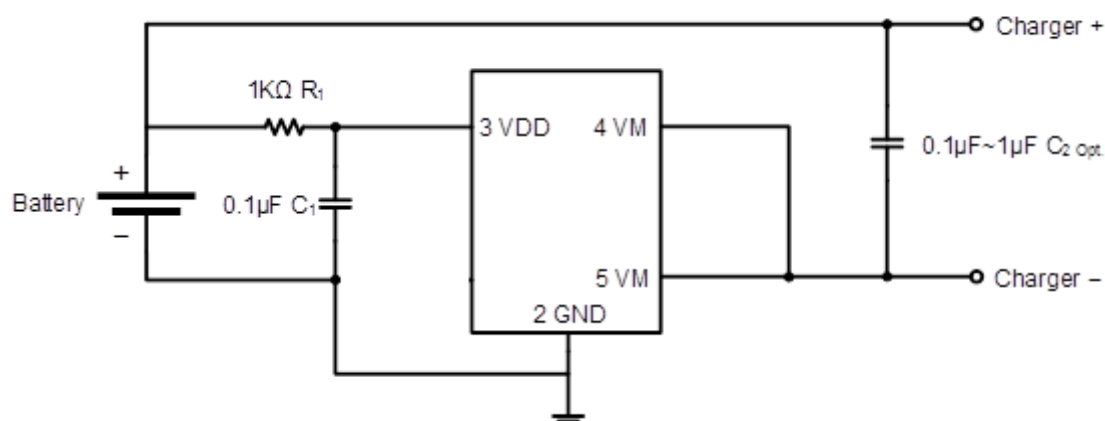


Figure 1. Typical Application Circuit

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Pin Description

Pin Configuration

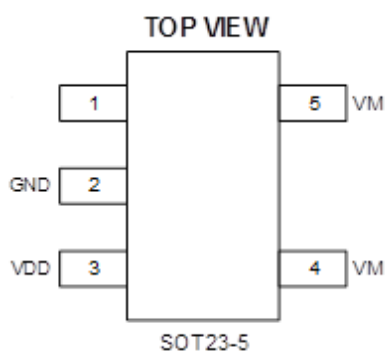


Figure 2. Pin Configuration

Top Marking: MKYLL (device code: MK, Y=year code, LL= lot number code)

Pin Description

Pin	Name	Function
1	NC	NC
2	GND	Ground Pin
3	VDD	Power Supply Pin
4	VM	The negative terminal of the battery pack. The internal FET switch connects this terminal to GND
5	VM	The negative terminal of the battery pack. The internal FET switch connects this terminal to GND

Order Information

Marking	Part No.	Model	Description	Package	MOQ
MKYLL	70702030	J O 7656	J O 7656 One Cell Li-ion and Li-poly Battery Protection IC, SOT23-5	SOT235	3000PCS

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Absolute Maximum Ratings ^{(1) (2)}

VDD Input Voltage	-0.3V to 6V	VM Input Voltage	-6V to 10V V _{BS}
Operating Temperature Range	-40°C to +85°C	Storage Temperature Range	-55°C to 150°C
Lead Temperature (Soldering, 10s)	+300°C	Junction Temperature.....	+125°C
θ _{JA}	250°C/W	ESD (Human Body Made) HMB.....	2KV
θ _{JC}	130°C/W	ESD (Machine Made) MM.....	200V

Note 1: Exceeding these ratings may damage the device.

Note 2: The device is not guaranteed to function outside of its operating conditions.

Electrical Characteristics ⁽³⁾

Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
Detection Voltage						
Overcharge Detection Voltage	V _{CU}		4.25	4.3	4.35	V
Overcharge Release Voltage	V _{CL}		4.05	4.1	4.15	V
Overdischarge Detection Voltage	V _{DL}		2.3	2.4	2.5	V
Overdischarge Release Voltage	V _{DR}		2.9	3.0	3.1	V
Charger Detection Voltage	*V _{CHA}			-0.12		V
Detection Current						
Overdischarge Current1 Detection	*I _{IOV1}	V _{DD} =3.6V		3		A
Load Short-Circuiting Detection	*I _{SHORT}	V _{DD} =3.6V		15		A
Current Consumption						
Current Consumption in Operation	I _{OPE}	V _{DD} =3.6V VM=0V		2.5	5	μA
Current Consumption in power Down	I _{PDN}	V _{DD} =2.0V VM floating		1.5	4	μA
VM Internal Resistance						
Resistance between VM and V _{DD}	*R _{VMD}	V _{DD} =3.6V VM=1.0V		320		kΩ
Resistance between VM and GND	*R _{VMS}	V _{DD} =2.0V VM=1.0V		25		kΩ
FET on Resistance						
Equivalent FET on Resistance	*R _{SS(ON)}	V _{DD} =3.6V I _{VM} =1.0A		50		mΩ
Over Temperature Protection						
Over Temperature Protection	*T _{SHD+}			130		°C
Over Temperature Recovery Degree	*T _{SHD-}			100		°C
Detection Delay Time						
Overcharge Voltage Detection Delay Time	t _{CU}			128	200	mS
Overdischarge Voltage Detection Delay Time	t _{DL}			40	60	mS

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Overdischarge Current Detection Delay Time	* t_{IOV}	$V_{DD}=3.6V$		10		mS
Load Short-Circuiting Detection Delay Time	* t_{SHORT}	$V_{DD}=3.6V$		80		μS

Note 3: *The parameter is guaranteed by design.

Functional Block Diagram

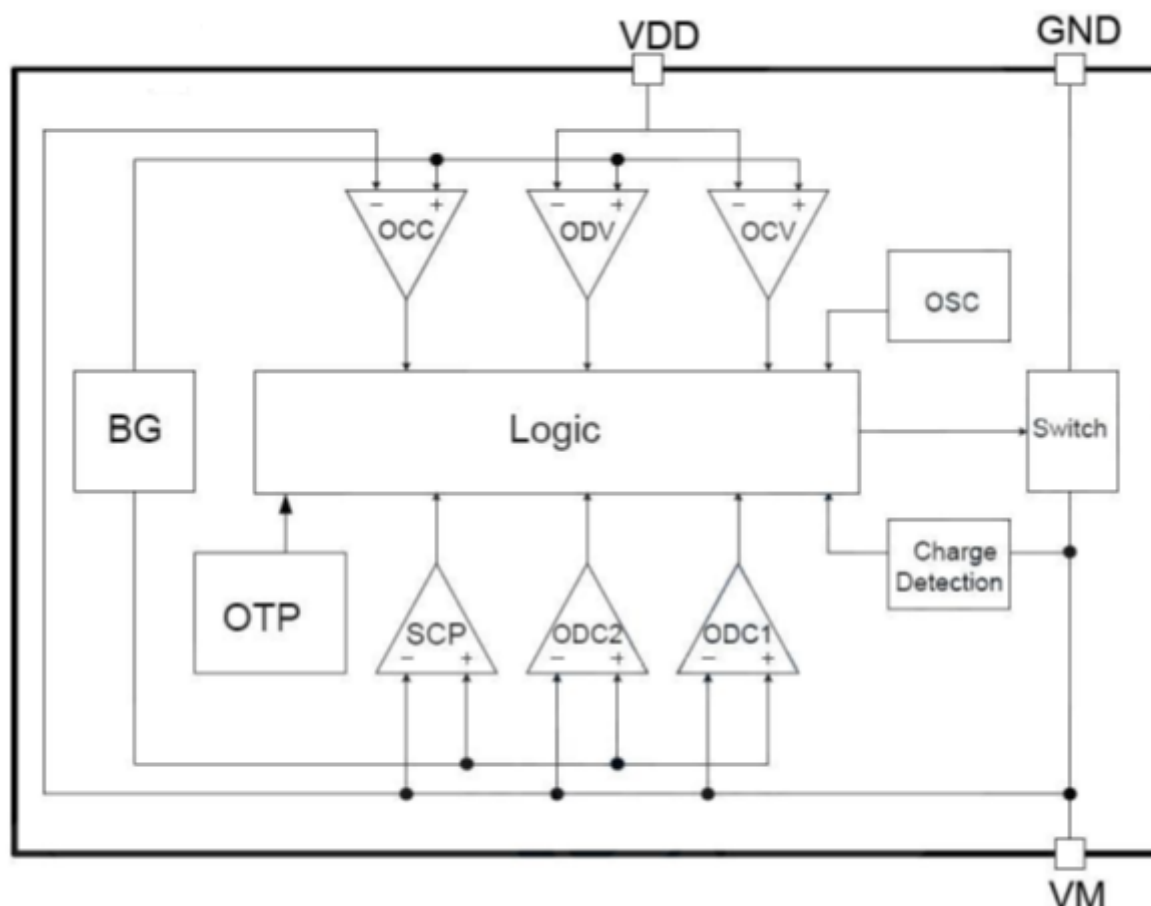


Figure 3. Functional Block Diagram

Functions Description

The J O 7656 monitors the voltage and current of a battery and protects it from being damaged due to overcharge voltage, over discharge voltage, over discharge current, and short circuit conditions by disconnecting the batter from the load or charger. These functions are required in order to operate the battery cell within specified limits. The device requires only one external capacitor. The MOSFET is integrated and its $R_{SS(ON)}$ is as low as 50m Ω typical.

Normal operating mode

If no exception condition is detected, charging and discharging can be carried out freely. This condition is called the normal operating mode.

Overcharge Condition

When the battery voltage becomes higher than the overcharge detection voltage (V_{CU}) during charging under

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normal condition and the state continues for the overcharge detection delay time (t_{CU}) or longer, the J O 7656 turns the charging control FET off to stop charging. This condition is called the overcharge condition. The overcharge condition is released in the following two cases:

1. When the battery voltage drops below the overcharge release voltage (V_{CL}), the J O 7656 turns the charging control FET on and returns to the normal condition.
2. When a load is connected and discharging starts, the J O 7656 turns the charging control FET on and returns to the normal condition. The release mechanism is as follows: the discharging current flows through an internal parasitic diode of the charging FET immediately after a load is connected and discharging starts, and the VM pin voltage increases about 0.7V (forward voltage of the diode) from the GND pin voltage momentarily. The J O 7656 detects this voltage and releases the overcharge condition. Consequently, in the case that the battery voltage is equal to or lower than the overcharge detection voltage (V_{CU}), the J O 7656 returns to the normal condition immediately, but in the case the battery voltage is higher than the overcharge detection voltage (V_{CU}), the chip does not return to the normal condition until the battery voltage drops below the overcharge detection voltage (V_{CU}) even if the load is connected. In addition, if the VM pin voltage is equal to or lower than the overcurrent 1 detection voltage when a load is connected and discharging starts, the chip does not return to the normal condition. **Remark** If the battery is charged to a voltage higher than the overcharge detection voltage (V_{CU}) and the battery voltage does not drop below the overcharge detection voltage (V_{CU}) even when a heavy load, which causes an overcurrent, is connected, the overcurrent 1 and overcurrent 2 do not work until the battery voltage drops below the overcharge detection voltage (V_{CU}). Since an actual battery has, however, an internal impedance of several dozens of $m\Omega$, and the battery voltage drops immediately after a heavy load which causes an overcurrent is connected, the overcurrent 1 and overcurrent 2 work. Detection of load short circuiting works regardless of the battery voltage.

Overdischarge Condition

When the battery voltage drops below the overdischarge detection voltage (V_{DL}) during discharging under normal condition and it continues for the overdischarge detection delay time (t_{DL}) or longer, the J O 7656 turns the discharging control FET off and stops discharging. This condition is called overdischarge condition. After the discharging control FET is turned off, the VM pin is pulled up by the R_{VMD} resistor between VM and VDD in J O 7656. Meanwhile when VM is bigger than 1.5 V (typ.) (the load short-circuiting detection voltage), the current of the chip is reduced to the power-down current (I_{PDN}). This condition is called power-down condition. The VM and VDD pins are shorted by the R_{VMD} resistor in the IC under the overdischarge and power-down conditions. The power-down condition is released when a charger is connected and the potential difference between VM and VDD becomes 1.3 V (typ.) or higher (load shortcircuiting detection voltage). At this time, the FET is still off. When the battery voltage becomes the overdischarge detection voltage (V_{DL}) or higher (see note), the J O 7656 turns the FET on and changes to the normal condition from the overdischarge condition. **Remark** If the VM pin voltage is no less than the charger detection voltage (V_{CHA}), when the battery under overdischarge condition is connected to a charger, the overdischarge condition is released (the discharging control FET is turned on) as usual, provided that the battery voltage reaches the overdischarge release voltage (V_{DU}) or higher.

Overcurrent Condition

When the discharging current becomes equal to or higher than a specified value (the VM pin voltage is equal to or higher than the overcurrent detection voltage) during discharging under normal condition and the state continues for the overcurrent detection delay time or longer, the J O 7656 turns off the discharging control FET to stop

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discharging. This condition is called overcurrent condition. (The overcurrent includes overcurrent, or load shortcircuiting.) The VM and GND pins are shorted internally by the R_{VMS} resistor under the overcurrent condition. When a load is connected, the VM pin voltage equals the VDD voltage due to the load. The overcurrent condition returns to the normal condition when the load is released and the impedance between the B+ and B- pins becomes higher than the automatic recoverable impedance. When the load is removed, the VM pin goes back to the GND potential since the VM pin is shorted the GND pin with the R_{VMS} resistor. Detecting that the VM pin potential is lower than the overcurrent detection voltage (V_{IOV}), the IC returns to the normal condition.

Abnormal Charge Current Detection

the VM pin voltage drops below the charger detection voltage (V_{CHA}) during charging under the normal condition and it continues for the overcharge detection delay time (t_{CU}) or longer, the J O 7656 turns the charging control FET off and stops charging. This action is called abnormal charge current detection. Abnormal charge current detection works when the discharging control FET is on and the VM pin voltage drops below the charger detection voltage (V_{CHA}). When an abnormal charge current flows into a battery in the overdischarge condition, the J O 7656 consequently turns the charging control FET off and stops charging after the battery voltage becomes the overdischarge detection voltage and the overcharge detection delay time (t_{CU}) elapses. Abnormal charge current detection is released when the voltage difference between VM pin and GND pin becomes lower than the charger detection voltage (V_{CHA}) by separating the charger. Since the 0V battery charging function has higher priority than the abnormal charge current detection function, abnormal charge current may not be detected by the product with the 0V battery charging function while the battery voltage is low.

Load Short-circuiting condition

If voltage of VM pin is equal or below short-circuiting protection voltage (V_{SHORT}), the J O 7656 will stop discharging and battery is disconnected from load. The maximum delay time to switch current off is t_{SHORT} . This status is released when voltage of VM pin is higher than short protection voltage (V_{SHORT}), such as when disconnecting the load.

Delay Circuits

The detection delay time for overdischarge current 2 and load short-circuiting starts when overdischarge current 1 is detected. As soon as overdischarge current 2 or load short-circuiting is detected over detection delay time for overdischarge current 2 or load short-circuiting, the J O 7656 stops discharging. When battery voltage falls below overdischarge detection voltage due to overdischarge current, the J O 7656 stop discharging by overdischarge current detection. In this case the recovery of battery voltage is so slow that if battery voltage after overdischarge voltage detection delay time is still lower than overdischarge detection voltage, the J O 7656 shifts to power-down.

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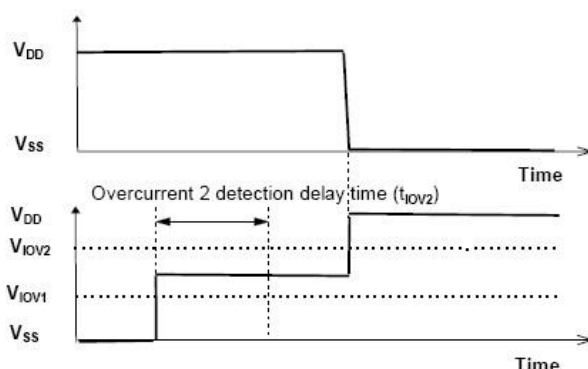


Figure 4. Overcurrent delay time

0V Battery Charging Function (4)(5)(6)

The recommended inductor values are shown in the Application Diagram. It is important to guarantee the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the peak load current plus the ripple current: Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer.

This function enables the charging of a connected battery whose voltage is 0V by self-discharge. When a charger having 0V battery start charging charger voltage (V_{0CHA}) or higher is connected between B+ and B- pins, the charging control FET gate is fixed to VDD potential. When the voltage between the gate and the source of the charging control FET becomes equal to or higher than the turn-on voltage by the charger voltage, the charging control FET is turned on to start charging. At this time, the discharging control FET is off and the charging current flows through the internal parasitic diode in the discharging control FET. If the battery voltage becomes equal to or higher than the overdischarge release voltage (V_{DU}), the normal condition returns.

Note

Note 4: Some battery providers do not recommend charging of completely discharged batteries. Please refer to battery providers before the selection of 0 V battery charging function. Note 5: The 0V battery charging function has higher priority than the abnormal charge current detection function. Consequently, a product with the 0 V battery charging function charges a battery and abnormal charge current cannot be detected during the battery voltage is low (at most 1.8 V or lower).

Note 6: When a battery is connected to the IC for the first time, the IC may not enter the normal condition in which discharging is possible. In this case, set the VM pin voltage equal to the GND voltage (short the VM and

GND pins or connect a charger) to enter the normal condition. **Timing Chart**

Overcharge and overdischarge detection

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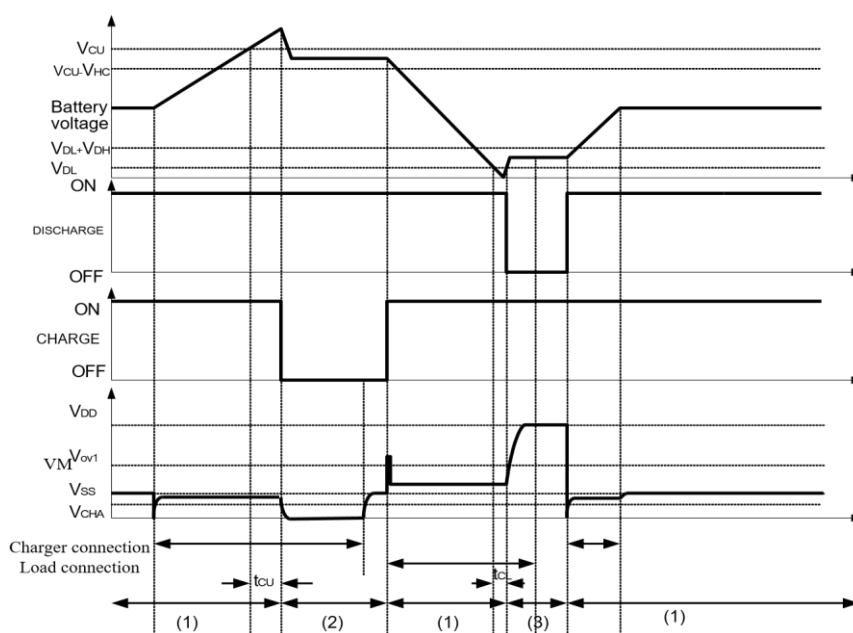


Figure5-1 Overcharge and Overdischarge Voltage Detection

Remark:

- (1) Normal condition (2) Overcharge voltage condition
(3) Overdischarge voltage condition (4) Overcurrent condition

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Overdischarge current detection

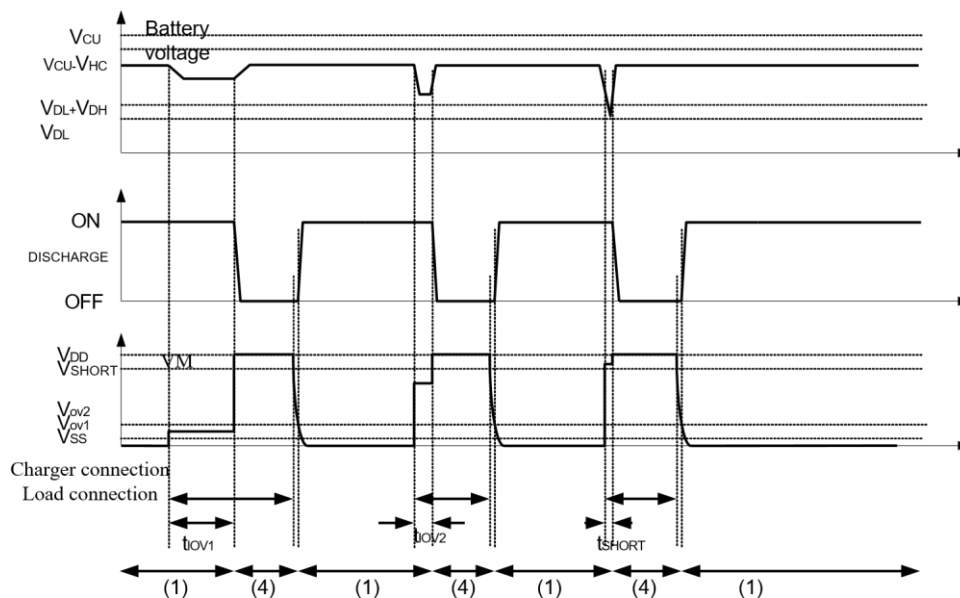


Figure5-2 Overdischarge Current Detection

Remark:

- (1) Normal condition (2) Overcharge voltage condition
(3) Overdischarge voltage condition (4) Overcurrent condition

Charger Detection

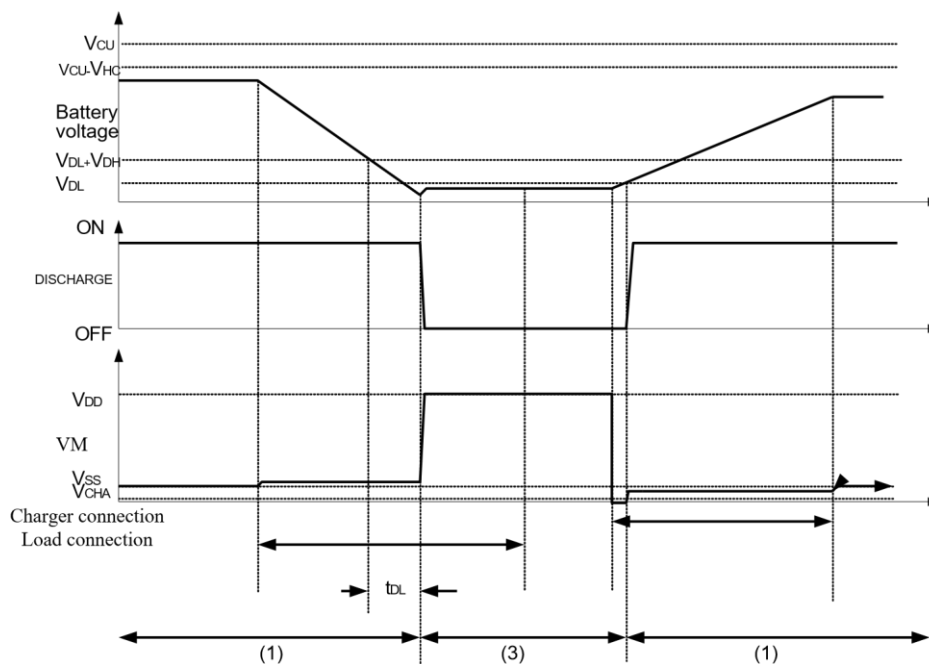


Figure5-3 Charger Detection

Remark:

- (1) Normal condition (2) Overcharge voltage condition

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(3) Overdischarge voltage condition (4) Overcurrent condition

Abnormal Charger Detection

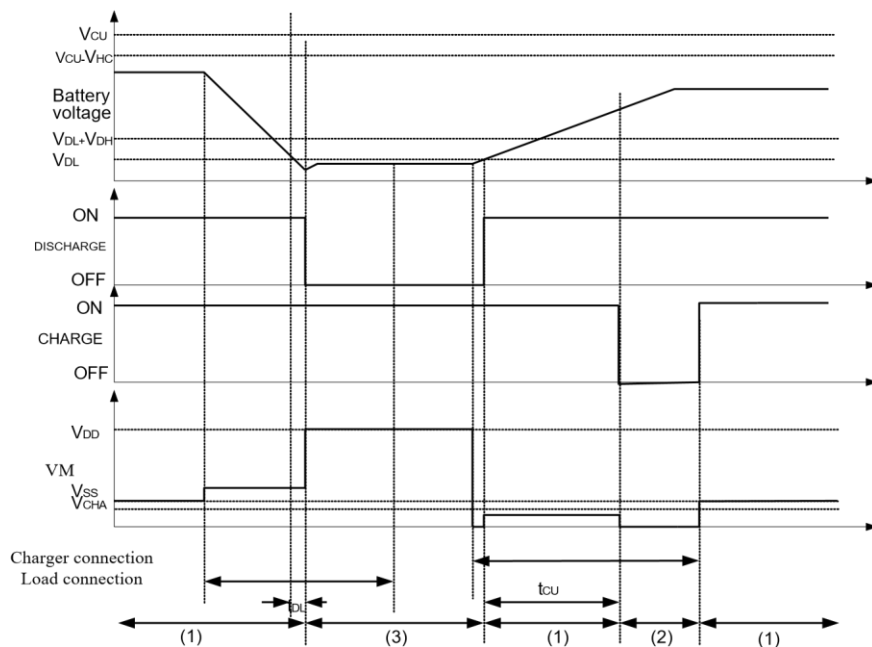


Figure5-4 Abnormal Charger Detection

Remark:

(1) Normal condition (2) Overcharge voltage condition
(3) Overdischarge voltage condition (4) Overcurrent condition

Typical Application

As shown in Figure 1, the bold line is the high density current path which must be kept as short as possible. For thermal management, ensure that these trace widths are adequate. C1 & R1 is a decoupling capacitor & resistor which should be placed as close as possible to HM5434.

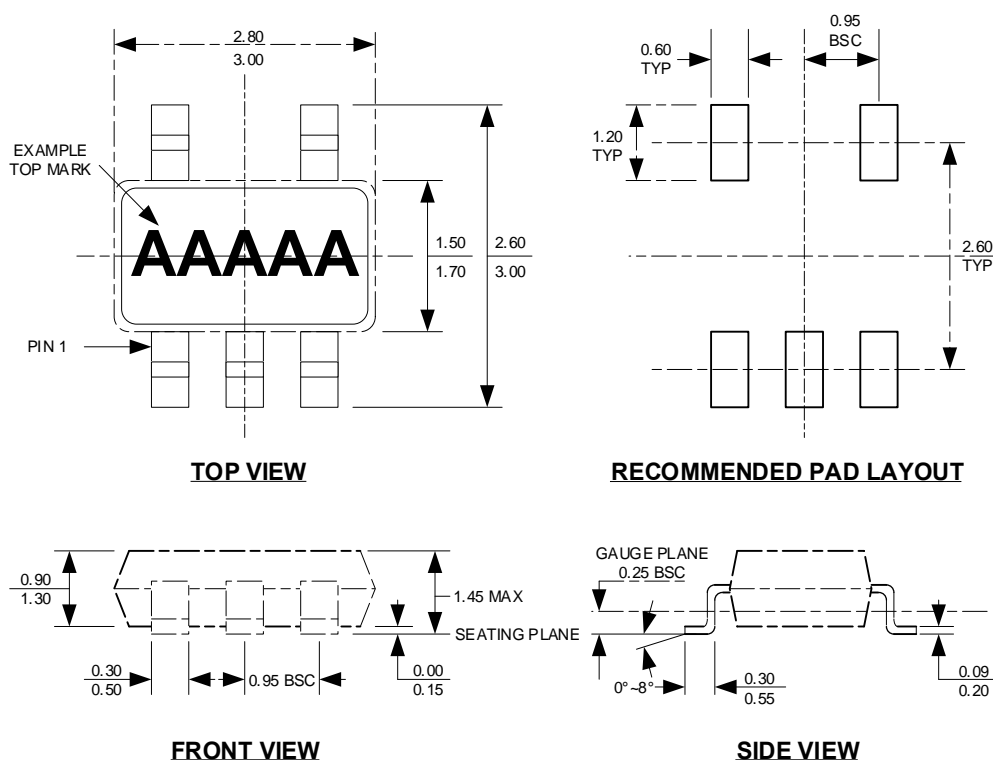
Precautions

- Pay attention to the operating conditions for input/output voltage and load current so that the power loss in J O 7656 does not exceed the power dissipation of the package.
- Do not apply an electrostatic discharge to this J O 7656 that exceeds the performance ratings of the built-in electrostatic protection circuit.

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Package Description

SOT23-5



NOTE:

1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.