

MSM27V3255CZ

1,048,576-Double Word x 32-Bit or 2,097,152-Word x 16-Bit

4-Double Word x 32-Bit or 8-Word x 16-Bit Page Mode One Time PROM

DESCRIPTION

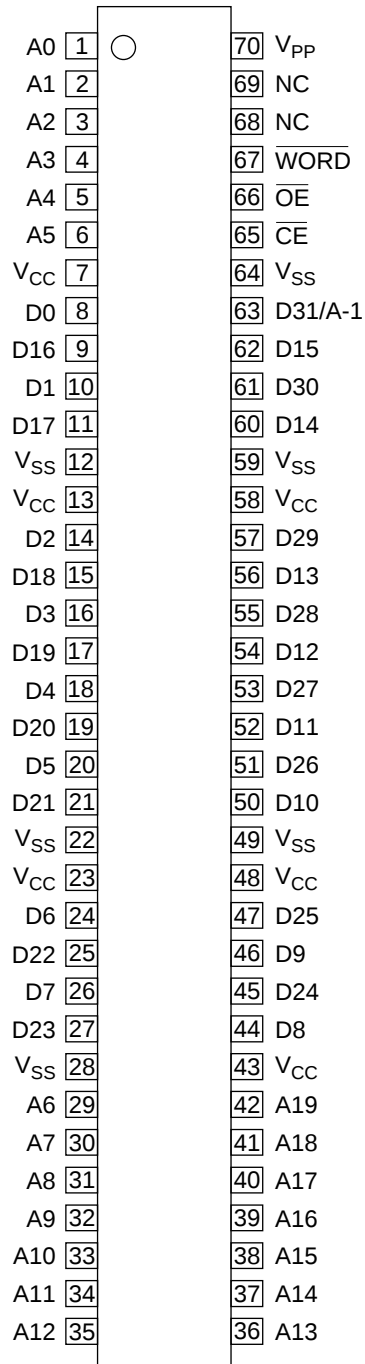
The MSM27V3255CZ is a 32Mbit electrically Programmable Read-Only Memory with page mode. Its configuration can be electrically switched between 1,048,576 double word x 32bit and 2,097,152 word x 16bit. The MSM27V3255CZ operates on a single +3.3V power supply and is TTL compatible. The MSM27V3255CZ provides Page mode which can greatly reduce the read access time. Since the MSM27V3255CZ operates asynchronously, external clocks are not required, making this device easy-to-use. The MSM27V3255CZ is suitable as large-capacity fixed memory for microcomputers and data terminals. It is manufactured using a CMOS double silicon gate technology and is offered in 70-pin SSOP package.

FEATURES

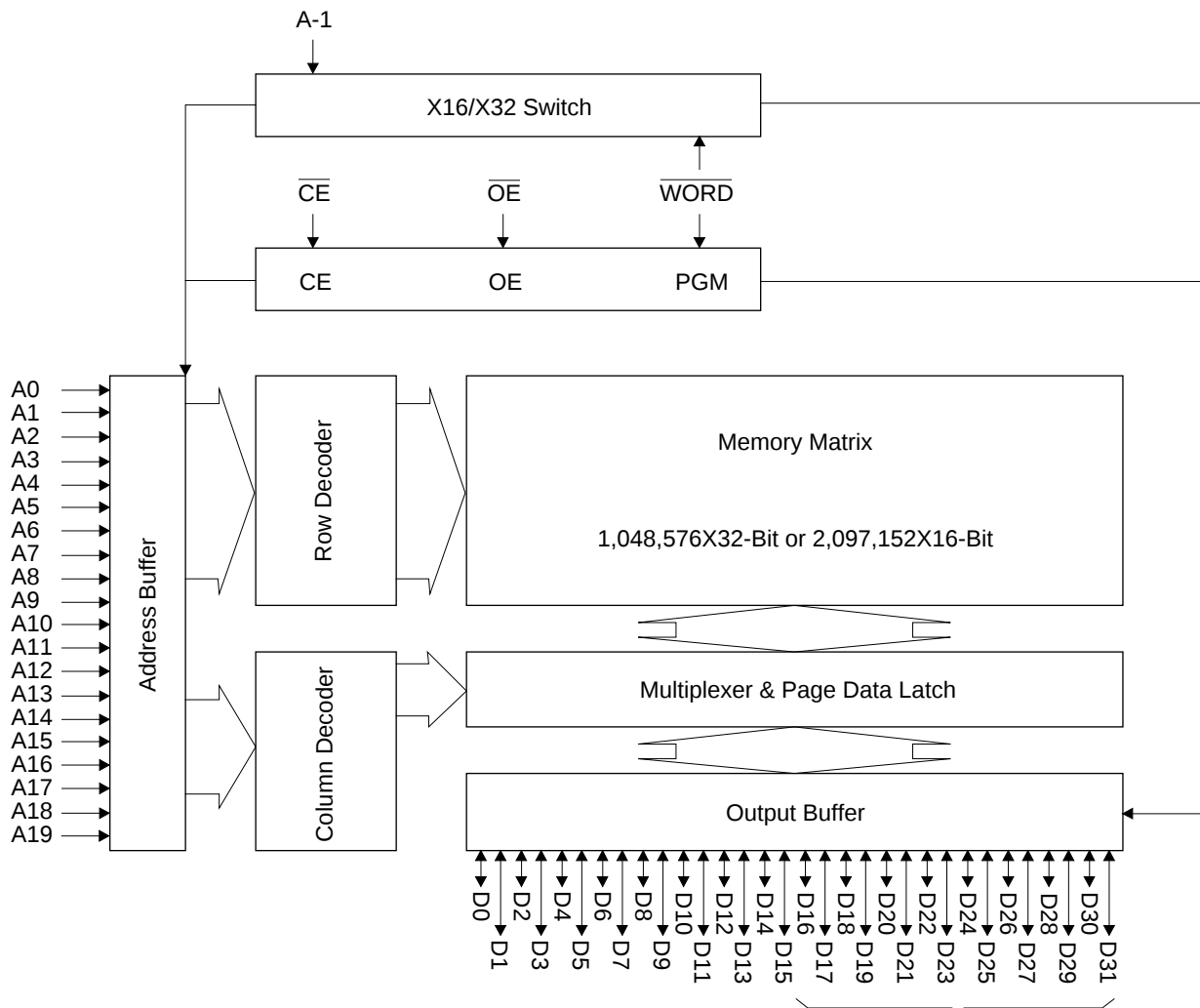
- 1,048,576 double word x 32bit / 2,097,152 word x 16bit electrically switchable configuration
- Single +3.3V power supply
- Access time 100ns
 - Page mode access time 30ns
- Input / Output TTL compatible
- Three-state output
- Packages

70-pin plastic SSOP (SSOP70-P-500-0.80-K)

PIN CONFIGURATION (TOP VIEW)



PIN NAMES	FUNCTIONS
D31/A-1	Data output / Address input
A0 - A19	Address input
D0 - D30	Data output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply voltage
V_{SS}	GND
$\overline{WORD}$	Mode switch
V_{PP}	Program power supply voltage
NC	Non connection

BLOCK DIAGRAM

In 16-bit output mode, these pins are three-stated and pin D31 functions as the A-1 address pin.

FUNCTION TABLE

MODE	CE	OE	WORD	V _{PP}	V _{CC}	D0 - D15	D16 - D30	D31/A-1	
READ (32-Bit)	L	L	H	*	3.3V	D _{OUT}			
READ (16-Bit)	L	L	L			D _{OUT}	Hi-Z	L/H	
OUTPUT DISABLE	L	H	H			Hi-Z			*
			L						
STAND-BY	H	*	H	11.0V	5.0V	Hi-Z			
			L			*			
PROGRAM	L	H	L			D _{IN}	Hi-Z	L/H	
PROGRAM INHIBIT	H	H				Hi-Z			
PROGRAM VERIFY	H	L		D _{OUT}	Hi-Z	L/H			

* : Don't Care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	T_{opr}	-	0 to 70	°C
Storage temperature	T_{stg}		-55 to 125	°C
Input voltage	V_I	relative to V_{SS}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_O		-0.5 to $V_{CC} + 0.5$	V
Power supply voltage	V_{CC}		-0.5 to 7	V
Program power supply voltage	V_{PP}		-0.5 to 12.5	V
Power dissipation per package	P_D	-	1.0	W

RECOMMENDED OPERATING CONDITIONS FOR READ

(Ta=0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{CC} power supply voltage	V_{CC}	$V_{CC}=3.0V-3.6V$	3.0	-	3.6	V
V_{PP} power supply voltage	V_{PP}		-0.5	-	$V_{CC}+0.5$	V
Input "H" level	V_{IH}		2.2	-	$V_{CC}+0.5$	V
Input "L" level	V_{IL}		-0.5	-	0.6	V

Voltage is relative to Vss

ELECTRICAL CHARACTERISTICS (Read operation)**DC Characteristics**(V_{CC}=3.3V±0.3V, Ta=0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I _{LI}	V _I =0 to V _{CC}	-	-	10	μA
Output leakage current	I _{LO}	V _O =0 to V _{CC}	-	-	10	μA
V _{CC} power supply current (Standby)	I _{CS1}	$\overline{CE}=V_{CC}$	-	-	50	μA
	I _{CS2}	$\overline{CE}=V_{IH}$	-	-	1	mA
V _{CC} power supply current (Read)	I _{CCA}	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$ tc=100ns	-	-	80	mA
V _{PP} power supply current	I _{PP}	V _{PP} =V _{CC}	-	-	10	μA
Input "H" level	V _{IH}	-	2.2	-	V _{CC} +0.5	V
Input "L" level	V _{IL}	-	-0.5	-	0.6	V
Output "H" level	V _{OH}	I _{OH} =-400μA	2.4	-	-	V
Output "L" level	V _{OL}	I _{OL} =2.1mA	-	-	0.45	V

Voltage is relative to Vss

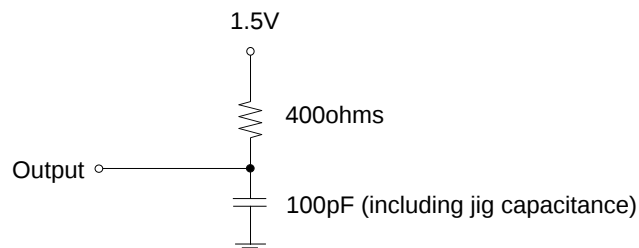
AC Characteristics(V_{CC}=3.3V±0.3V, Ta=0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Address access cycle time	T _C	-	100	-	ns
Address access time	T _{ACC}	$\overline{CE}=\overline{OE}=V_{IL}$	-	100	ns
Page set up time	T _{PSET}	NOTE(1)	120	-	ns
Page access cycle time	T _{PC}	-	30	-	ns
Page access time	T _{PAC}	-	-	30	ns
$\overline{CE}$ access time	T _{CE}	$\overline{OE}=V_{IL}$	-	100	ns
$\overline{OE}$ access time	T _{OE}	$\overline{CE}=V_{IL}$	-	30	ns
Output disable time	T _{CHZ}	$\overline{OE}=V_{IL}$	0	30	ns
	T _{OHZ}	$\overline{CE}=V_{IL}$	0	25	ns
Output hold time	T _{OH}	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	ns

NOTE(1) T_{PSET} is defined as the end of either $\overline{CE}$ trailing edge or address transition in random access term until the first page address transition.

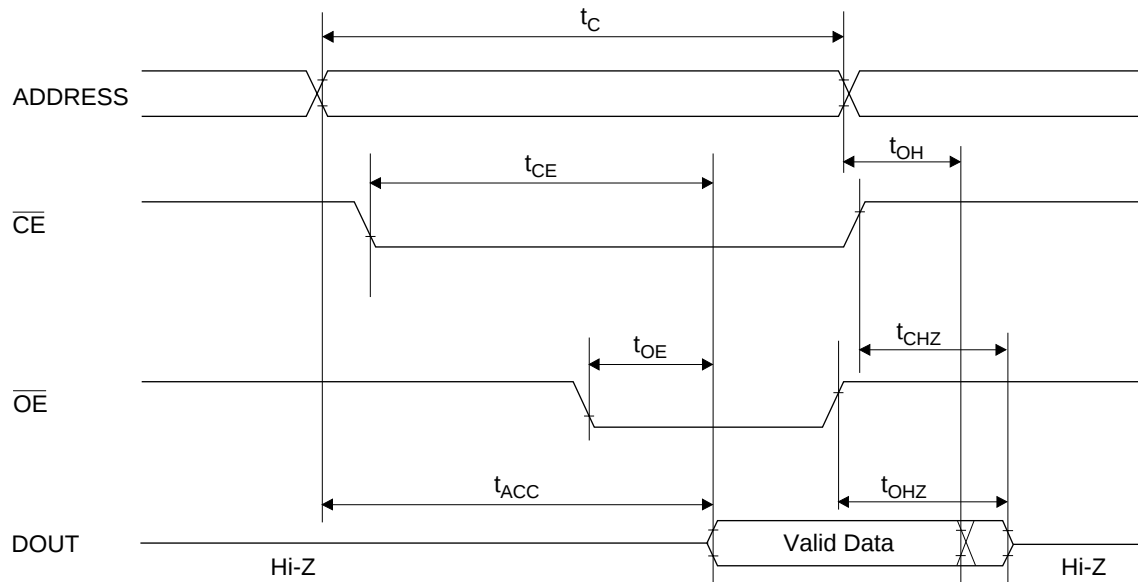
Measurement conditions

Input signal level	-----	0V/3V
Input timing reference level	-----	0.8V/2.0V
Output load	-----	100pF
Output timing reference level	-----	0.8V/2.0V

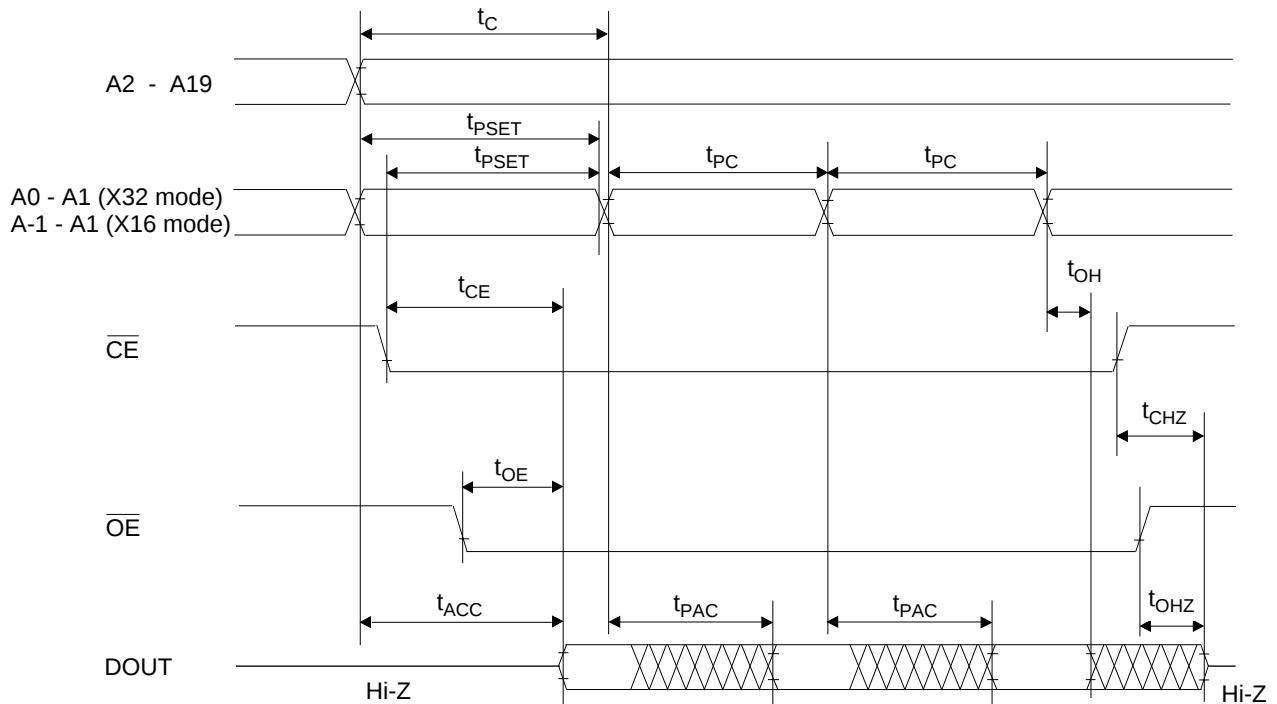


TIMING CHART

NORMAL MODE READ CYCLE



PAGE MODE READ CYCLE



ELECTRICAL CHARACTERISTICS (Programming operation)**DC Characteristics**

(Ta=25°C±5°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I_{LI}	$V_I = V_{CC} + 0.5V$	-	-	10	μA
V_{PP} power supply current (Program)	I_{PP2}	$\overline{CE} = V_{IL}$	-	-	50	mA
V_{CC} power supply current	I_{CC}	-	-	-	100	mA
Input "H" level	V_{IH}	-	2.2	-	$V_{CC} + 0.5$	V
Input "L" level	V_{IL}	-	-0.5	-	0.8	V
Output "H" level	V_{OH}	$I_{OH} = -400\mu A$	2.4	-	-	V
Output "L" level	V_{OL}	$I_{OL} = 2.1mA$	-	-	0.45	V
Program voltage	V_{PP}	-	10.75	11.0	11.25	V
V_{CC} power supply voltage	V_{CC}	-	4.75	5.0	5.25	V

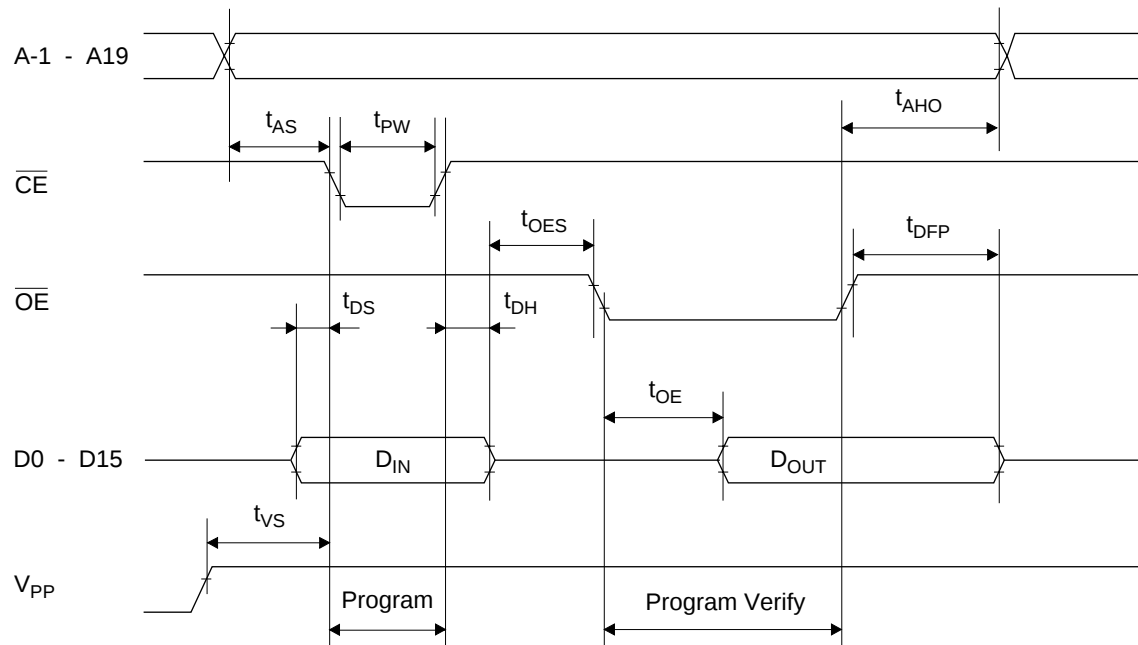
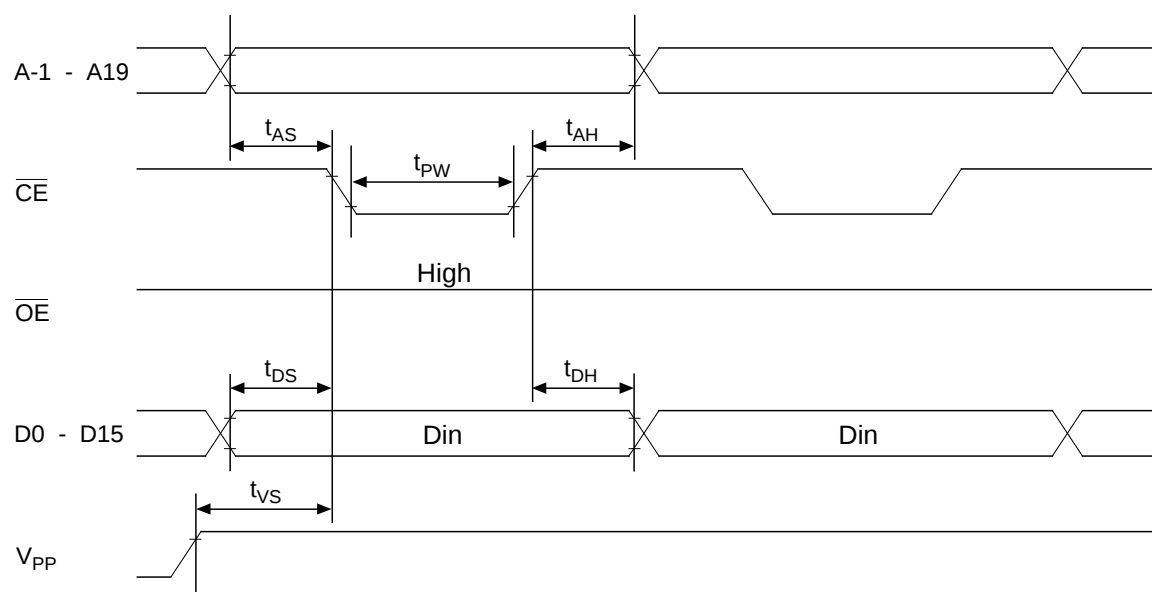
Voltage is relative to Vss

AC Characteristics(V_{CC}=5.0V±0.25V, V_{pp}=11.0V±0.25V, Ta=25°C±5°C)

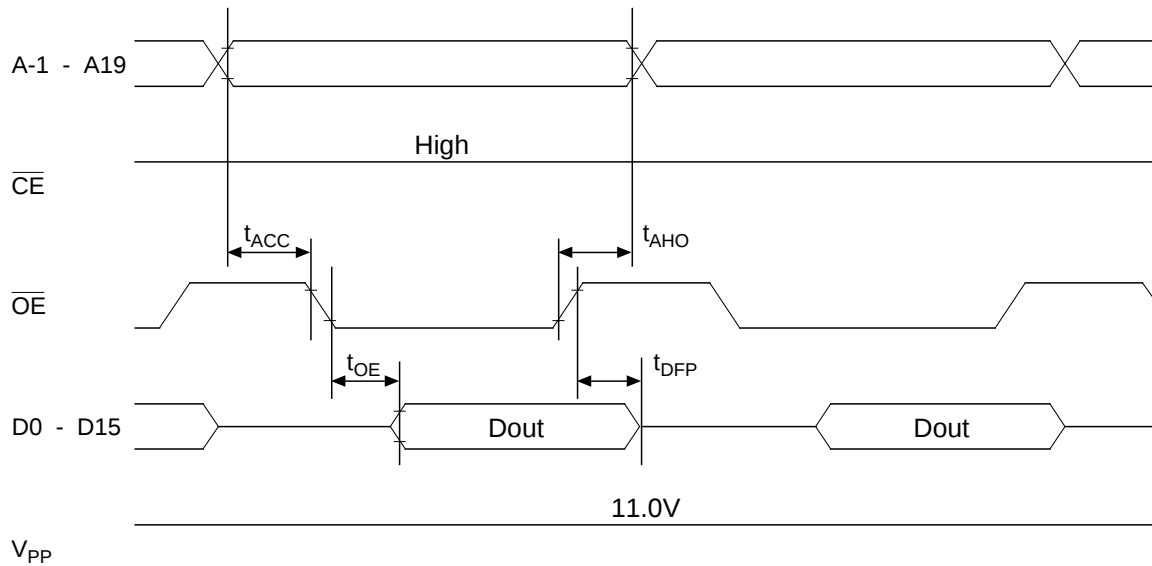
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Address set-up time	T_{AS}	-	2	-	-	μs
$\overline{OE}$ set-up time	T_{OES}	-	2	-	-	μs
Data set-up time	T_{DS}	-	2	-	-	μs
Address hold time	T_{AH}	-	0	-	-	μs
Data hold time	T_{DH}	-	2	-	-	μs
Output float delay from $\overline{OE}$	T_{DFP}	-	0	-	130	ns
V_{PP} voltage set-up time	T_{VS}	-	2	-	-	μs
Program pulse width	T_{PW}	-	23	25	27	μs
Data valid from $\overline{OE}$	T_{OE}	-	-	-	150	ns
Address hold from $\overline{OE}$ high	T_{AHO}	-	0	-	-	μs

PIN Capacitance(V_{CC}=3.3V, Ta=25°C, f=1MHz)

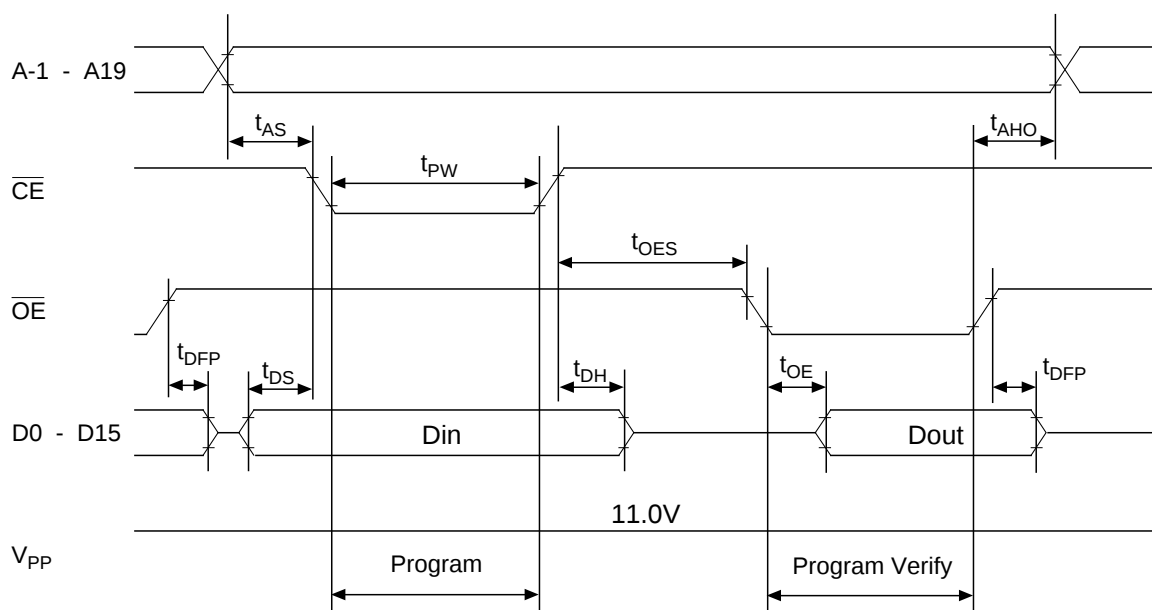
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C_{IN}	$V_I = 0V$	-	-	12	pF
Output	C_{OUT}	$V_O = 0V$	-	-	15	

Programming Waveforms (I)**: Under High Speed Programming Algorithm (I)****Program and Program Verify Cycle Waveforms****Programming Waveforms (II)****: Under High Speed Programming Algorithm (II)****Consecutive Programming Waveforms**

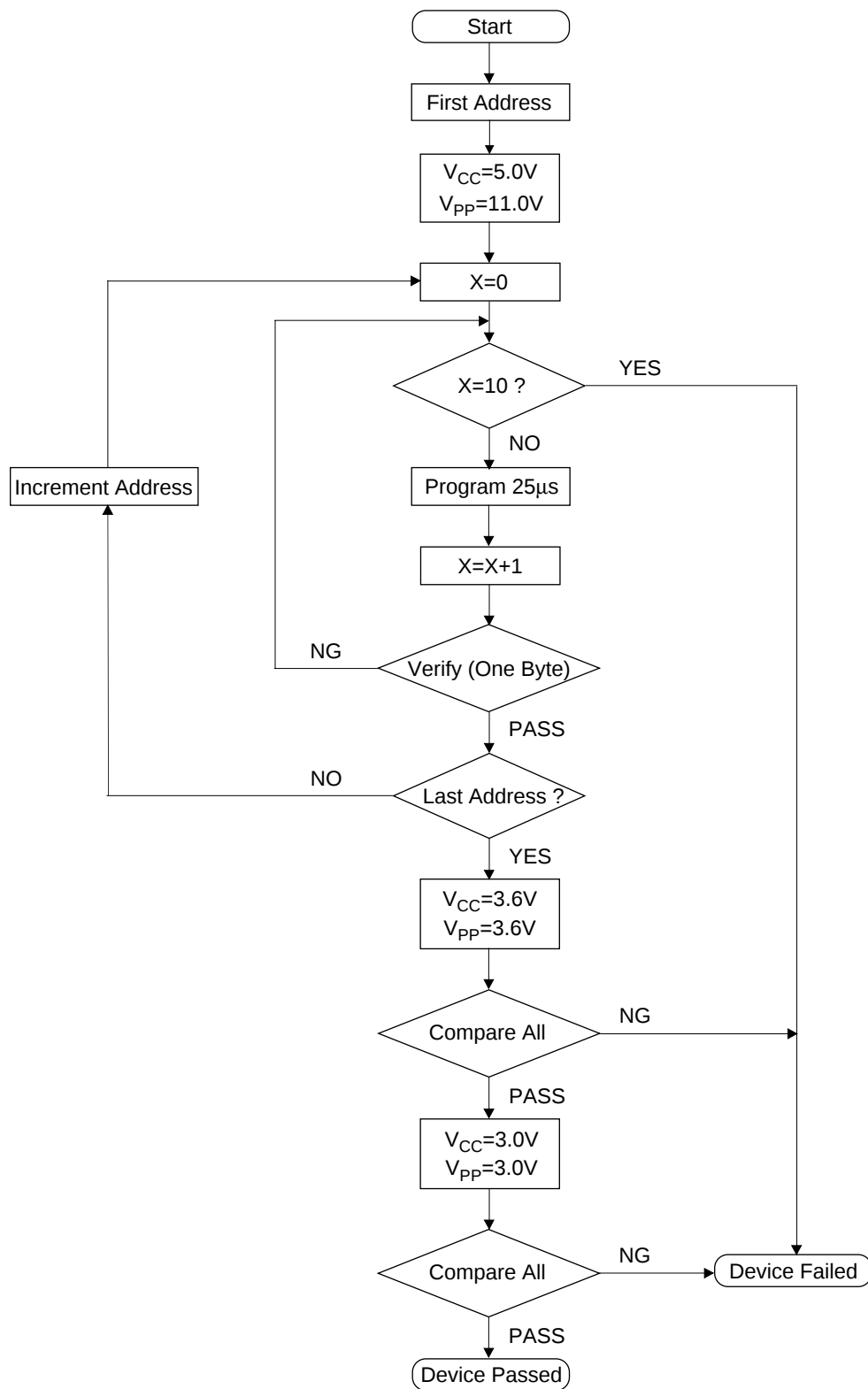
Consecutive Program Verify Waveforms



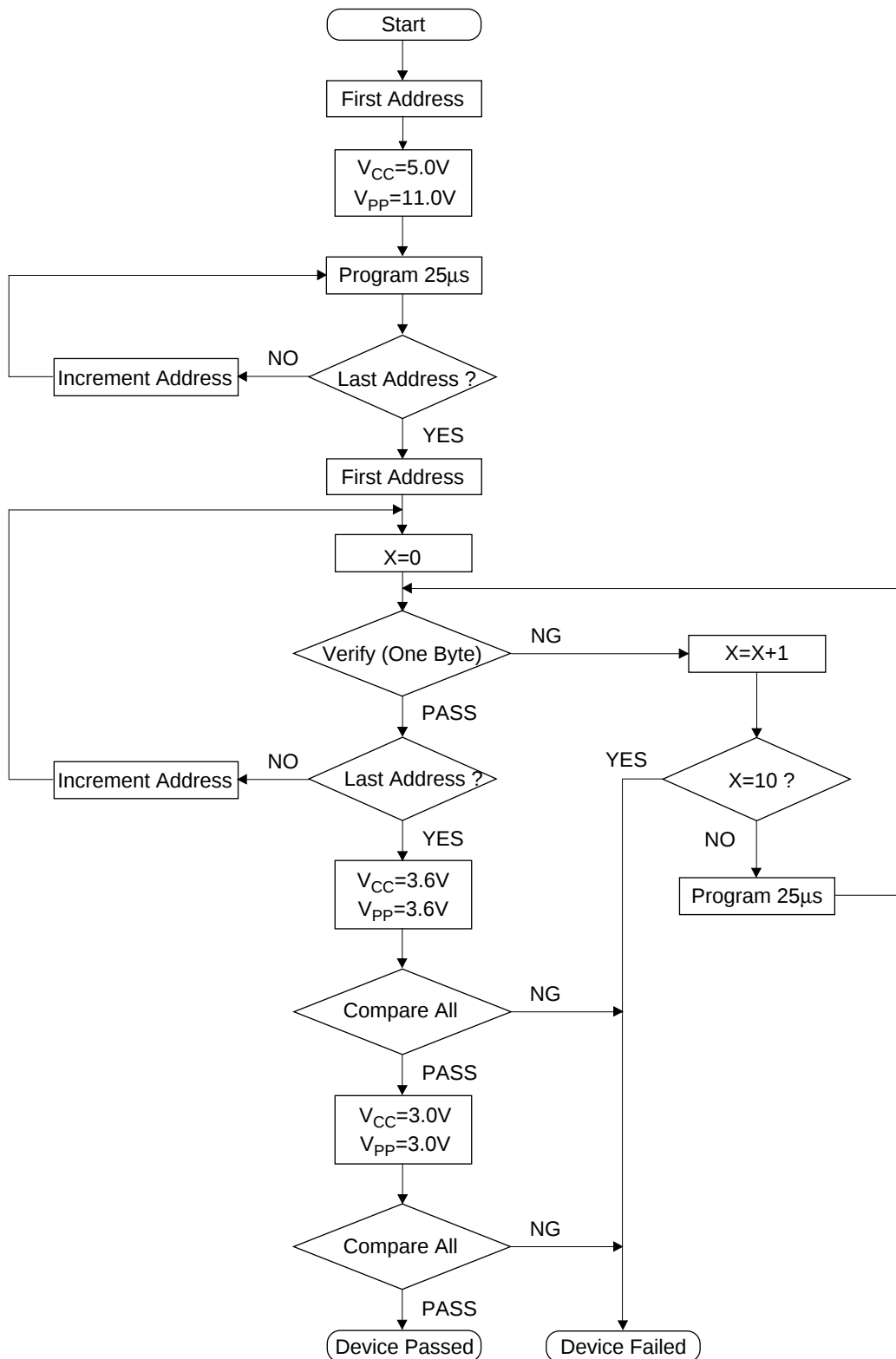
Program and Program Verify Cycle Waveforms



High Speed Programming Algorithm (I)



High Speed Programming Algorithm (II)



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