LMP8640/-Q1/HV Precision High Voltage Current Sense Amplifiers

1 Features

- Typical Values, T_A = 25°C
- High Common-Mode Voltage Range
  - LMP8640: -2 V to 42 V
  - LMP8640-Q1: -2 V to 42 V, AEC-Q100
  - LMP8640HV: -2 V to 76 V
- Supply Voltage Range: 2.7 V to 12 V
- Gain Options: 20 V/V; 50 V/V; 100 V/V
- Max Gain Error: 0.25%
- Low Offset Voltage: 900 µV
- Input Bias Current: 13 µA
- PSRR: 85 dB
- CMRR (2.1V to 42V): 103 dB
- Temperature Range: -40°C to 125°C
- 6-Pin Thin SOT-23 Package

2 Applications

- High-Side Current Sense
- Vehicle Current Measurement
- Motor Controls
- Battery Monitoring
- Remote Sensing
- Power Management

3 Description

The LMP8640, LMP8640-Q1 and the LMP8640HV are precision current sense amplifiers that detect small differential voltages across a sense resistor in the presence of high input common mode voltages with a supply voltage range from 2.7 V to 12 V.

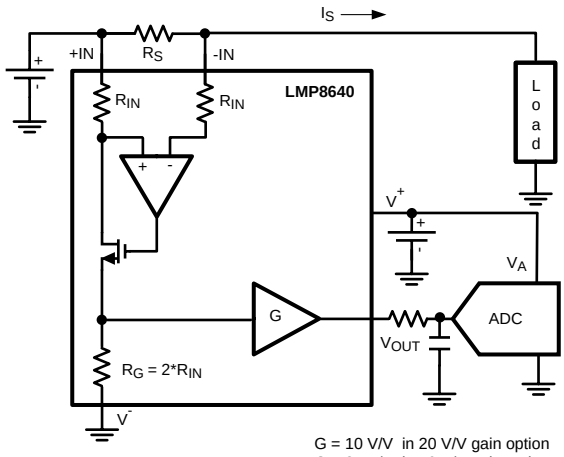
The LMP8640 and LMP8640-Q1 accept input signals with common mode voltage range from -2 V to 42 V, while the LMP8640HV accepts input signal with common mode voltage range from -2 V to 76 V. The LMP8640 and LMP8640HV have fixed gain for applications that demand accuracy over temperature. The LMP8640 and LMP8640HV come out with three different fixed gains 20 V/V, 50 V/V, 100 V/V ensuring a gain accuracy as low as 0.25%. The output is buffered in order to provide low output impedance. This high side current sense amplifier is ideal for sensing and monitoring currents in DC or battery powered systems, excellent AC and DC specifications over temperature, and keeps errors in the current sense loop to a minimum. The LMP8640 and LMP8640HV are ideal choice for industrial and consumer applications, while the LMP8640-Q1 is an AEC-Q100 grade 1 qualified version of the LMP8640 for automotive applications. The LMP8640-x is available in SOT-23-6 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMP8640	SOT23 (6)	2.9 mm x 1.6 mm
LMP8640-Q1		
LMP8640HV		

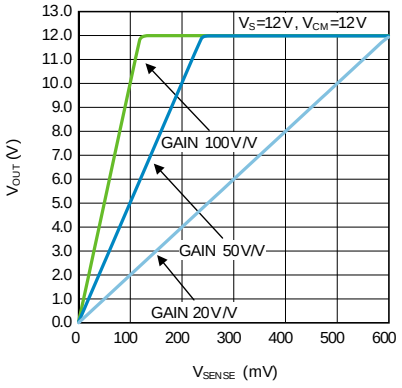
(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



G = 10 V/V in 20 V/V gain option
G = 25 V/V in 50 V/V gain option
G = 50 V/V in 100 V/V gain option

Output Voltage vs Input Voltage



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

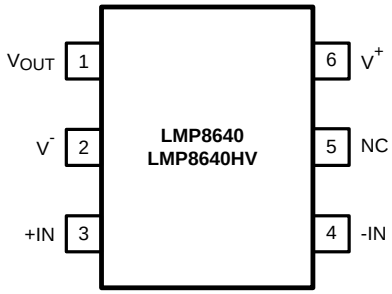
Changes from Revision F (April 2013) to Revision G	Page
• New Q Device added to datasheet	1
• Changed data sheet flow and layout to conform with new TI standards. Added the following sections: Application and Implementation; Power Supply Recommendations; Layout; Device and Documentation Support; Mechanical, Packaging, and Ordering Information	1

5 Device Comparison Table

DEVICE NAME	GAIN	QUALIFICATIONS	MAX COMMON MODE VOLTAGE
LMP8640-T	x20		-2 V to +42 V
LMP8640-T	x20		-2 V to +42 V
LMP8640-Q1-T	x20	Automotive AEC-Q100, Grade 1	-2 V to +42 V
LMP8640-F	x50		-2 V to +42 V
LMP8640-H	x100		-2 V to +42 V
LMP8640HV-T	x20		-2 V to +76 V
LMP8640HV-F	x50		-2 V to +76 V
LMP8640HV-H	x100		-2 V to +76 V

6 Pin Configuration and Functions

6-Pin SOT-23
DDC0006A Package
(Top View)



Pin Functions

PIN		DESCRIPTION
NUMBER	NAME	
1	V_{OUT}	Output
2	V^-	Negative Supply Voltage
3	+IN	Positive Input
4	-IN	Negative Input
5	NC	Not Internally Connected
6	V^+	Positive Supply Voltage

7 Specifications

7.1 Absolute Maximum Ratings(1)(2)(3)

LMP8640 limits also apply to the LMP8640-Q1.

		MIN	MAX	UNIT
Supply Voltage ($V_S = V^+ - V^-$)		-0.3	13.2	V
Differential Voltage +IN- (-IN)		-6	6	V
Voltage at pins +IN, -IN	LMP8640HV	-6	80	V
	LMP8640, LMP8640-Q1	-6	60	V
Voltage at V_{OUT} pin		V^-	V^+	V
Junction Temperature (4)		-40	150	°C

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) For soldering specifications,see product folder at www.ti.com and http://www.ti.com/lit/SNOA549.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} - T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

7.2 Handling Ratings - LMP8640, LMP8640HV

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			-65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM(1))	For input pins +IN, -IN	-5000	5000	V
			For all other pins	-2000	2000	
		Charged device model (CDM)(2)	All pins	-1250	1250	
		Machine model (MM) (3)		-200	200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)

7.3 Handling Ratings - LMP8640-Q1

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			-65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		-2000	2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	-1000	1000	
		Machine model (MM) (2)	All pins	-200	200	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)

7.4 Recommended Operating Conditions(1)

	MIN	MAX	UNIT
Supply Voltage ($V_S = V^+ - V^-$)	2.7	12	V
Operating Junction Temperature Range (2)	-40	125	°C

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} - T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

7.5 Thermal Information

THERMAL METRIC[1]		LMP8640 LMP8640HV LMP8640-Q1 THIN SOT-23 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance [2]	165	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28	
$R_{\theta JB}$	Junction-to-board thermal resistance	24.6	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	23.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} - T_A)/ \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

7.6 Electrical Characteristics 2.7 V [1]

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S= V^+ – V^-, V_{SENSE}= +IN-(-IN), V^+ = 2.7 V, V^- = 0 V, −2 V < V_{CM} < 76 V, R_L = 10 MΩ. LMP8640 limits also apply to the LMP8640-Q1.

PARAMETER		TEST CONDITIONS	MIN[2]	TYP[3]	MAX[2]	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 2.1 V	-900		900	µV
		V_{CM} = 2.1 V, Over Temperature	-1160		1160	
TCV_{OS}	Input Offset Voltage Drift[4] [5]	V_{CM} = 2.1 V			2.6	µV/°C
I_B	Input Bias Current [6]	V_{CM} = 2.1 V, V_{SENSE} = 0 V		12	20	µA
		V_{CM} = 2.1 V, Over Temperature, V_{SENSE} = 0 V			27	
e_{ni}	Input Voltage Noise [5]	f > 10 kHz		117		nV/√Hz
Gain A_V	Gain LMP8640-T LMP8640HV-T			20		V/V
	Gain LMP8640-F LMP8640HV-F			50		
	Gain LMP8640-H LMP8640HV-H			100		
	Gain error	V_{CM} = 2.1 V	-0.25%		0.25%	
		V_{CM} = 2.1 V, Over Temperature	-0.51%		0.51%	
	Accuracy over temperature[5]	V_{CM} = 2.1V, Over Temperature			26.2	ppm/°C
PSRR	Power Supply Rejection Ratio	V_{CM} = 2.1 V, 2.7 V < V^+ < 12 V,	85			dB
CMRR	Common Mode Rejection Ratio	LMP8640HV 2.1 V < V_{CM} < 42 V LMP8640 2.1 V < V_{CM}< 42 V	103			dB
		LMP8640HV 2.1 V < V_{CM} < 76 V	95			
		-2 V <V_{CM} < 2 V,	60			

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(5) This parameter is ensured by design and/or characterization and is not tested in production.
(6) Positive Bias Current corresponds to current flowing into the device. Spec does not include input signal dependent currents on the positive input of approximately Vsense / 5KΩ due to topology feedback action.

Electrical Characteristics 2.7 V (1) (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S= V^+ – V^-, V_{SENSE}= +IN-(-IN), V^+ = 2.7 V, V^- = 0 V, −2 V < V_{CM} < 76 V, R_L = 10 MΩ. LMP8640 limits also apply to the LMP8640-Q1.

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
BW	Fixed Gain LMP8640-T LMP8640HV-T (5)	DC V_{SENSE} = 67.5 mV, C_L = 30 pF,R_L= 1MΩ		950		kHz
	Fixed Gain LMP8640-F LMP8640HV-F (5)	DC V_{SENSE} =27 mV, C_L = 30 pF, R_L= 1MΩ		450		
	Fixed Gain LMP8640-H LMP8640HV-H (5)	DC V_{SENSE} = 13.5 mV, C_L = 30 pF ,R_L= 1 MΩ		230		
SR	Slew Rate (7)(5)	V_{CM} =5 V, C_L = 30 pF, R_L = 1 MΩ, LMP8640-T LMP8640HV-T V_{SENSE} =100 mVpp, LMP8640-F LMP8640HV-F V_{SENSE} =40 mVpp, LMP8640-H LMP8640HV-H V_{SENSE} =20 mVpp,		1.4		V/µs
R_{IN}	Differential Mode Input Impedance(5)			5		kΩ
I_S	Supply Current	V_{CM} = 2.1 V		420	600	µA
		V_{CM} = 2.1 V, Over Temperature			800	
		V_{CM} = −2 V		2000	2500	
		V_{CM} = −2 V, Over Temperature			2750	
V_{OUT}	Maximum Output Voltage	V_{CM} = 2.1 V	2.65			V
	Minimum Output Voltage	LMP8640-T LMP8640HV-T V_{CM} = 2.1 V			18.2	mV
		LMP8640-F LMP8640HV-F V_{CM} = 2.1 V			40	
		LMP8640-H LMP8640HV-H V_{CM} = 2.1 V			80	
C_{LOAD}	Max Output Capacitance Load(5)			30		pF

(7) The number specified is the average of rising and falling slew rates and measured at 90% to 10%.

7.7 Electrical Characteristics 5 V (1)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S= V^+ – V^-, V_{SENSE}= +IN-(-IN), V^+ = 5 V, V^- = 0 V, −2 V < V_{CM} < 76 V, R_L = 10 MΩ. LMP8640 electrical limits also apply to the LMP8640-Q1 unless noted.

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 2.1 V	-900		900	µV
		V_{CM} = 2.1 V, Over Temperature	-1160		1160	
TCV_{OS}	Input Offset Voltage Drift(4) (5)	V_{CM} = 2.1 V			2.6	µV/°C
I_B	Input Bias Current (6)	V_{CM} = 2.1 V, V_{SENSE} = 0 V		13	21	µA
		V_{CM} = 2.1 V, Over Temperature,V_{SENSE} = 0 V			28	
e_{ni}	Input Voltage Noise (5)	f > 10 kHz		117		nV/√Hz

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(5) This parameter is ensured by design and/or characterization and is not tested in production.
(6) Positive Bias Current corresponds to current flowing into the device. Spec does not include input signal dependent currents on the positive input of approximately Vsense / 5KΩ due to topology feedback action.

Electrical Characteristics 5 V [1] (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S= V^+ – V^-, V_{SENSE}= +IN-(-IN), V^+ = 5 V, V^- = 0 V, −2 V < V_{CM} < 76 V, R_L = 10 MΩ. LMP8640 electrical limits also apply to the LMP8640-Q1 unless noted.

PARAMETER		TEST CONDITIONS	MIN[2]	TYP[3]	MAX[2]	UNIT
Gain A_V	Gain LMP8640-T LMP8640HV-T			20		V/V
	Gain LMP8640-F LMP8640HV-F			50		
	Gain LMP8640-H LMP8640HV-H			100		
	Gain error	V_{CM} = 2.1 V	-0.25%		0.25%	
		V_{CM} = 2.1 V, Over Temperature	-0.51%		0.51%	
	Accuracy over temperature[5]	−40°C to 125°C, V_{CM}=2.1 V			26.2	ppm/°C
PSRR	Power Supply Rejection Ratio	V_{CM} = 2.1 V, 2.7V < V^+ < 12 V,	85			dB
CMRR	Common Mode Rejection Ratio	LMP8640HV 2.1 V < V_{CM} < 42 V LMP8640 2.1 V < V_{CM}< 42 V	103			dB
		LMP8640HV 2.1 V < V_{CM} < 76 V	95			
		-2 V <V_{CM} < 2 V,	60			
BW	Fixed Gain LMP8640-T LMP8640HV-T [5]	DC V_{SENSE} = 67.5 mV, C_L = 30 pF ,R_L= 1 MΩ		950		kHz
	Fixed Gain LMP8640-F LMP8640HV-F[5]	DC V_{SENSE} =27 mV, C_L = 30 pF ,R_L= 1 MΩ		450		
	Fixed Gain LMP8640-H LMP8640HV-H[5]	DC V_{SENSE} = 13.5 mV, C_L = 30 pF ,R_L= 1MΩ		230		
SR	Slew Rate [7][5]	V_{CM} =5 V, C_L = 30 pF, R_L = 1MΩ, LMP8640-T LMP8640HV-T V_{SENSE} = 200 mVpp, LMP8640-F LMP8640HV-F V_{SENSE} = 80 mVpp, LMP8640-H LMP8640HV-H V_{SENSE} = 40 mVpp,		1.6		V/µs
R_{IN}	Differential Mode Input Impedance[5]			5		kΩ
I_S	Supply Current	V_{CM} = 2.1 V		500	722	µA
		V_{CM} = 2.1 V, Over Temperature			922	
		V_{CM} = −2 V		2050	2500	
		V_{CM} = −2 V, Over Temperature			2750	
V_{OUT}	Maximum Output Voltage	V_{CM} = 2.1 V	4.95			V
	Minimum Output Voltage	LMP8640-T LMP8640HV-T V_{CM} = 2.1 V			18.2	mV
		LMP8640-F LMP8640HV-F V_{CM} = 2.1 V			40	
		LMP8640-H LMP8640HV-H V_{CM} = 2.1 V			80	
C_{LOAD}	Max Output Capacitance Load[5]			30		pF

(7) The number specified is the average of rising and falling slew rates and measured at 90% to 10%.

7.8 Electrical Characteristics 12 V (1)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S= V^+ – V^-, V_{SENSE}= +IN-(-IN), V^+ = 12 V, V^- = 0V, −2 V < V_{CM} < 76 V, R_L = 10 MΩ. LMP8640 electrical limits also apply to the LMP8640-Q1 unless noted.

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 2.1 V	-900		900	µV
		V_{CM} = 2.1 V, Over Temperature	-1160		1160	
TCV_{OS}	Input Offset Voltage Drift(4) (5)	V_{CM} = 2.1 V			2.6	µV/°C
I_B	Input Bias Current (6)	V_{CM} = 2.1 V, V_{SENSE} = 0 V		13	22	µA
		V_{CM} = 2.1 V, Over Temperature, V_{SENSE} = 0 V			28	
e_{ni}	Input Voltage Noise (5)	f > 10 kHz		117		nV/√Hz
Gain A_V	Gain LMP8640-T LMP8640HV-T			20		V/V
	Gain LMP8640-F LMP8640HV-F			50		
	Gain LMP8640-H LMP8640HV-H			100		
	Gain error	V_{CM} = 2.1 V	-0.25%		0.25%	
		V_{CM} = 2.1 V, Over Temperature	-0.51%		0.51%	
	Accuracy over temperature(5)	−40°C to 125°C, V_{CM}= 2.1 V			26.2	ppm/°C
PSRR	Power Supply Rejection Ratio	V_{CM} = 2.1 V, 2.7 V < V^+ < 12 V,	85			dB
CMRR	Common Mode Rejection Ratio	LMP8640HV 2.1 V < V_{CM} < 42 V LMP8640 2.1 V < V_{CM}< 42 V	103			dB
		LMP8640HV 2.1 V < V_{CM} < 76 V	95			
		-2 V < V_{CM} < 2 V,	60			
BW	Fixed Gain LMP8640-T LMP8640HV-T (5)	DC V_{SENSE} = 67.5 mV, C_L = 30 pF, R_L= 1 MΩ		950		kHz
	Fixed Gain LMP8640-F LMP8640HV-F (5)	DC V_{SENSE} =27 mV, C_L = 30 pF, R_L= 1 MΩ		450		
	Fixed Gain LMP8640-H LMP8640HV-H (5)	DC V_{SENSE} = 13.5 mV, C_L = 30 pF, R_L= 1 MΩ		230		
SR	Slew Rate (7)(5)	V_{CM} =5 V, C_L = 30 pF, R_L = 1 MΩ, LMP8640-T LMP8640HV-T V_{SENSE} = 500 mVpp, LMP8640-F LMP8640HV-F V_{SENSE} =200 mVpp, LMP8640-H LMP8640HV-H V_{SENSE} =100 mVpp,		1.8		V/µs
R_{IN}	Differential Mode Input Impedance(5)			5		kΩ

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage temperature drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.
(5) This parameter is ensured by design and/or characterization and is not tested in production.
(6) Positive Bias Current corresponds to current flowing into the device. Spec does not include input signal dependent currents on the positive input of approximately Vsense / 5KΩ due to topology feedback action.
(7) The number specified is the average of rising and falling slew rates and measured at 90% to 10%.

Electrical Characteristics 12 V [1] (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S= V^+ – V^-, V_{SENSE}= +IN-(-IN), V^+ = 12 V, V^- = 0V, −2 V < V_{CM} < 76 V, R_L = 10 MΩ. LMP8640 electrical limits also apply to the LMP8640-Q1 unless noted.

PARAMETER		TEST CONDITIONS	MIN [2]	TYP [3]	MAX [2]	UNIT
I_S	Supply Current	V_{CM} = 2.1 V		720	1050	µA
		V_{CM} = 2.1 V, Over Temperature			1250	
		V_{CM} = −2 V		2300	2800	
		V_{CM} = −2 V, Over Temperature			3000	
V_{OUT}	Maximum Output Voltage	V_{CM} = 2.1 V	11.85			V
	Minimum Output Voltage	LMP8640-T LMP8640HV-T V_{CM} = 2.1 V			18.2	mV
		LMP8640-F LMP8640HV-F V_{CM} = 2.1 V			40	
		LMP8640-H LMP8640HV-H V_{CM} = 2.1 V			80	
C_{LOAD}	Max Output Capacitance Load [5]			30		pF

7.9 Typical Characteristics

Unless otherwise specified: T_A = 25°C, V_S=V^+-V^-, V_{SENSE}= +IN - (-IN), R_L = 10 MΩ.

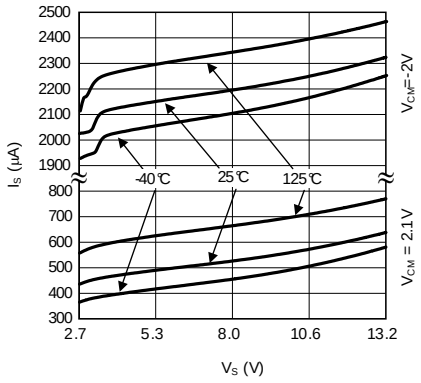


Figure 1. Supply Curent vs. Supply Voltage

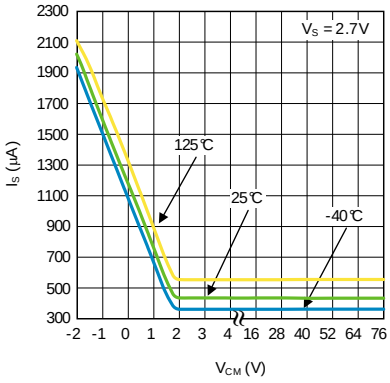


Figure 2. Supply Current vs. V_{CM}

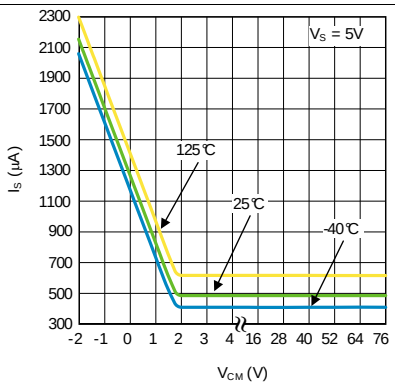


Figure 3. Supply Current vs. V_{CM}

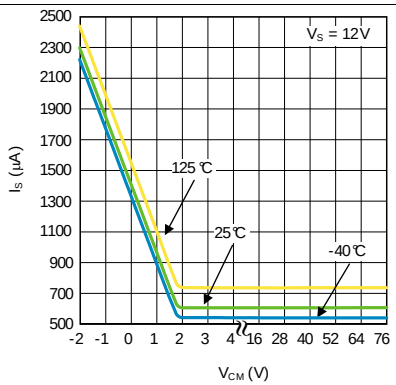


Figure 4. Supply Current vs. V_{CM}

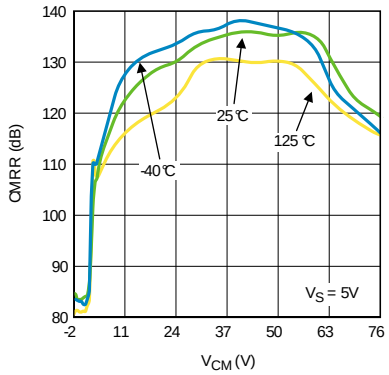


Figure 5. CMRR vs. V_{CM} (Gain 20 V/V)

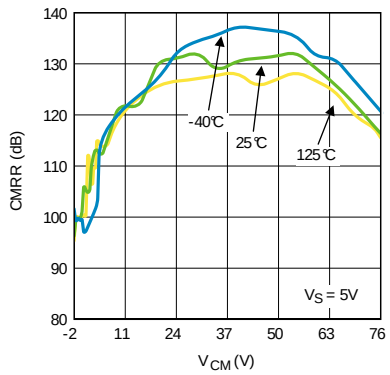


Figure 6. CMRR vs. V_{CM} (Gain 50 V/V)

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_S=V^+-V^-, V_{SENSE}= +IN - (-IN), R_L = 10 MΩ.

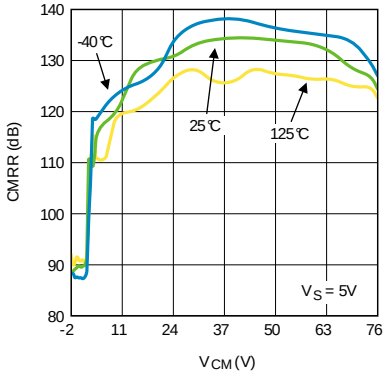


Figure 7. CMRR vs. V_{CM} (Gain 100 V/V)

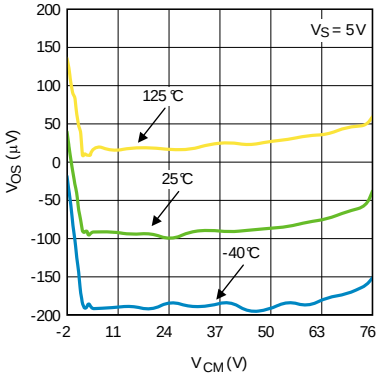


Figure 8. Input Voltage Offset vs. V_{CM}

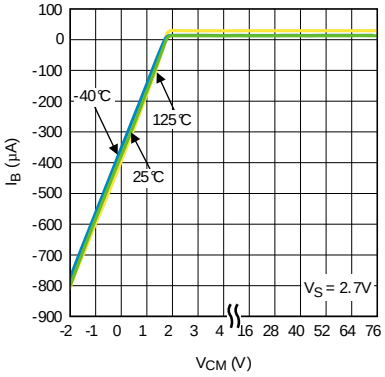


Figure 9. Ibias vs. V_{CM}

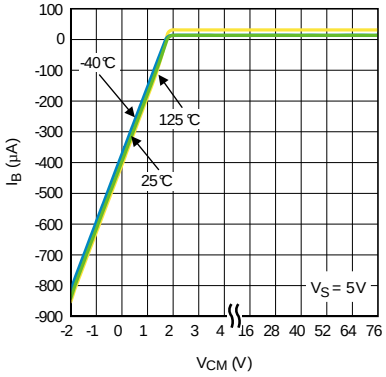


Figure 10. Ibias vs. V_{CM}

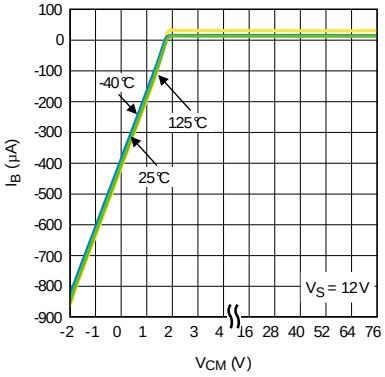


Figure 11. Ibias vs. V_{CM}

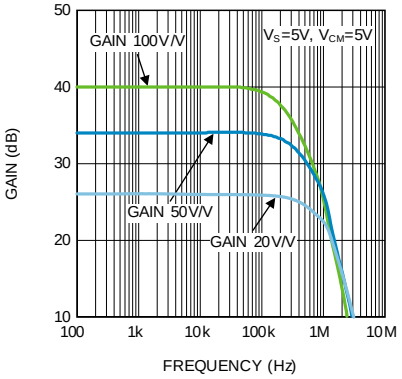


Figure 12. Gain vs. Frequency

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_S=V^+-V^-, V_{SENSE}= +IN - (-IN), R_L = 10 MΩ.

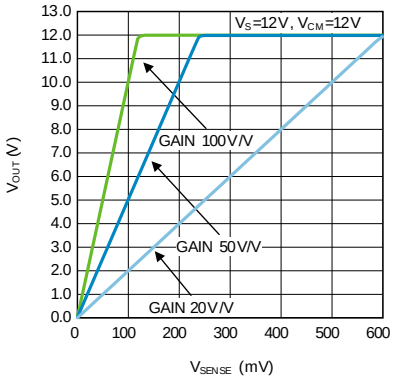


Figure 13. Output voltage vs. V_{SENSE}

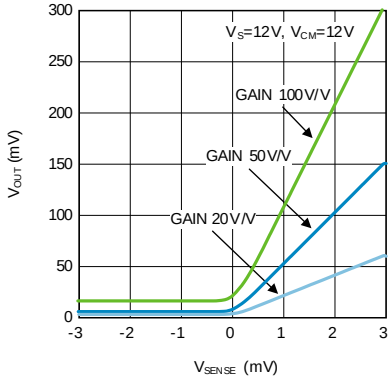


Figure 14. Output Voltage vs. V_{SENSE} (ZOOM Close to 0 V)

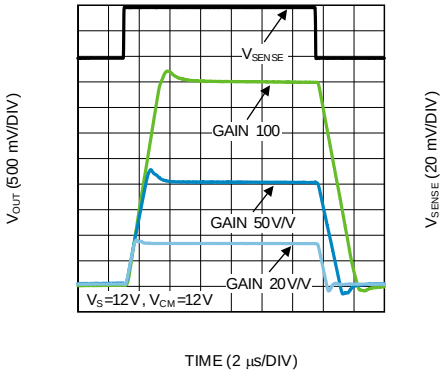


Figure 15. Large Step Response

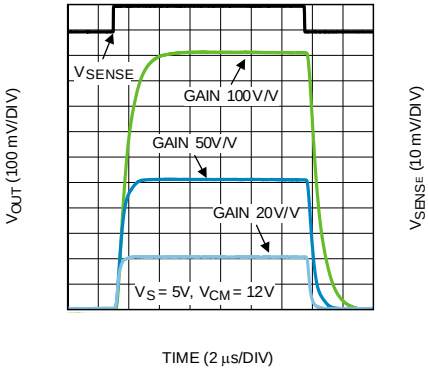


Figure 16. Small Step Response

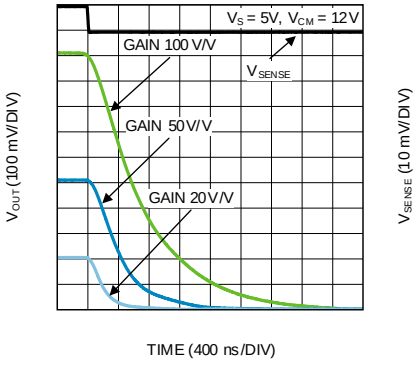


Figure 17. Settling Time (Fall)

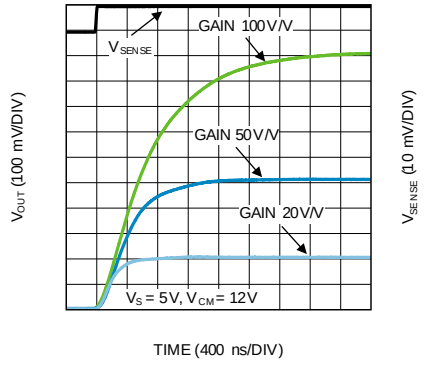


Figure 18. Settling Time (Rise)

Typical Characteristics (continued)

Unless otherwise specified: T_A = 25°C, V_S=V^+-V^-, V_{SENSE}= +IN - (-IN), R_L = 10 MΩ.

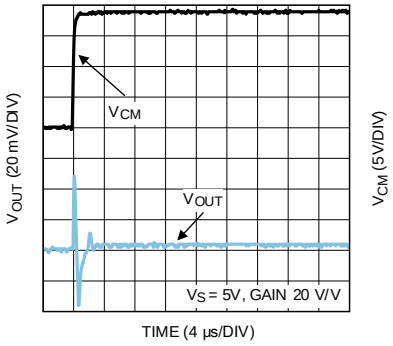


Figure 19. Common Mode Step Response (Rise)

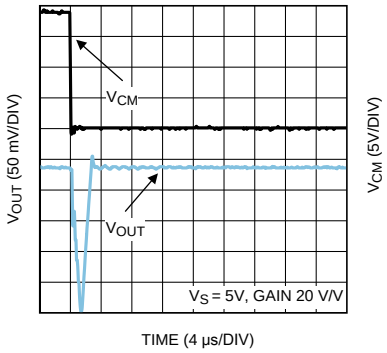


Figure 20. Common Mode Step Response (Fall)

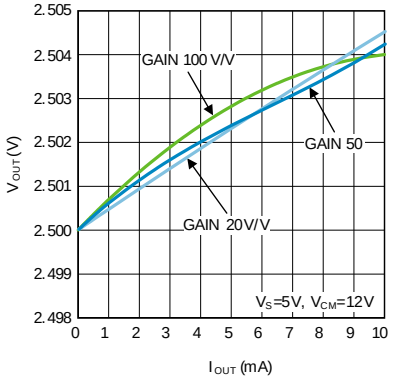


Figure 21. Load Regulation (Sinking)

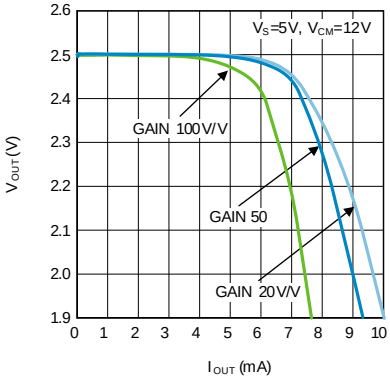


Figure 22. Load Regulation (Sourcing)

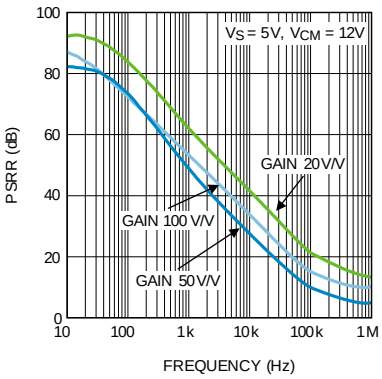


Figure 23. AC PSRR vs. Frequency

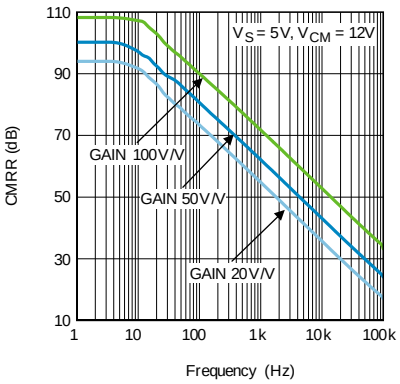


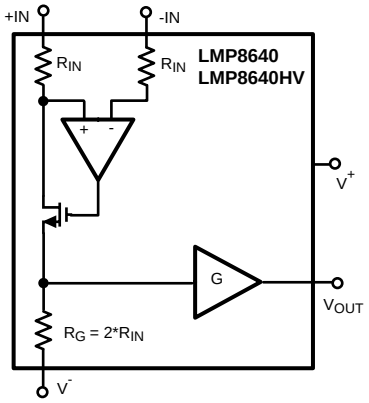
Figure 24. AC CMRR vs. Frequency

8 Detailed Description

8.1 Overview

The LMP8640 and LMP8640HV are single supply high side current sense amplifiers with a fixed gain of 20 V/V, 50 V/V, 100 V/V and a common mode voltage range of -2 V to 42 V (LMP8640-x) or -2 V to 76 V (LMP8640HV-x) with a buffered voltage output.

8.2 Functional Block Diagram



8.3 Feature Description

As seen in Figure 25, the current flowing through sense resistor R_S develops a voltage drop equal to V_{SENSE} across R_S. The voltage at the -IN pin will now be less than +IN by an amount proportional to the V_{SENSE} voltage.

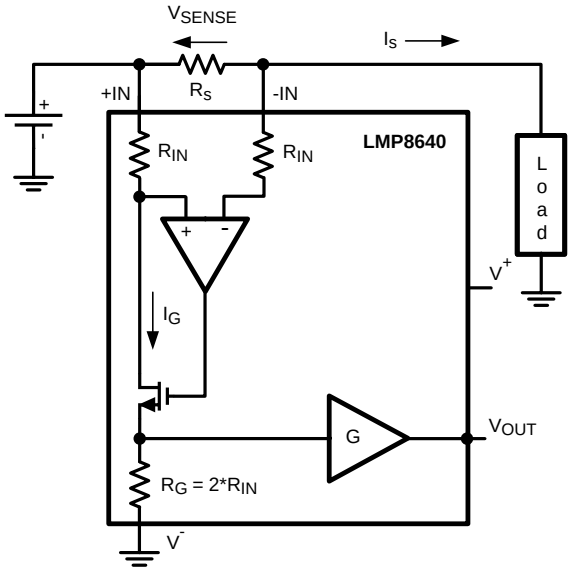


Figure 25. Simple Current Monitor

The low bias currents of the error amplifier cause little voltage drop through R_{IN-}, so the negative input of the internal error amplifier is at essentially the same potential as the -IN input. The R_{IN} resistors are 5 KΩ each.

Feature Description (continued)

The error amplifier will detect this voltage error between it's inputs and drive the MOSFET gate to conduct more current, increasing the voltage drop across R_{IN+}, until the servo amplifiers positive input matches the negative input. At this point, the voltage drop across R_{IN+} now matches V_{SENSE}.

I_G, a current proportional to I_S, will flow according to the following relation:

$$I_G = V_{SENSE}/R_{IN} = R_S * I_S/R_{IN} \quad (1)$$

I_G also flows through the internal gain resistor R_G developing a voltage drop equal to:

$$V_{RG} = I_G * R_G = (V_{SENSE}/R_{IN}) * R_G = ((R_S * I_S)/ R_{IN}) * R_G \quad (2)$$

$$V_{OUT} = 2*(R_S*I_S)*G, \quad (3)$$

where $G=R_G/R_{IN}$ = 10 V/V, 25 V/V or 50 V/V, according to the gain option selected.

The voltage on R_G is then amplified by a gain of 2 by the output gain stage to create the final overall gain of x20, x50 and x100. The output stage has a low impedance drive allowing the LMP8640 to easily interface with other IC's (ADC, Mux, µC…). No external buffering is required.

8.3.1 Selection of Sense Resistor

The value chosen for the shunt resistor, R_S, depends on the application. It plays a big role in a current sensing system and must be chosen with care. The selection of the shunt resistor needs to take in account the tradeoffs in small-signal accuracy, the power dissipated and the voltage loss across the shunt itself.

In applications where a small current is sensed, a bigger value of R_S is selected to minimize the error in the proportional output voltage. Higher resistor value improves the signal-to-noise ratio (SNR) at the input of the current sense amplifier and hence gives a more accurate output.

Similarly when high current is sensed, the power losses in R_S can be significant so a smaller value of R_S is desired. In this condition it is also required to take in account also the power rating of R_S resistor. The low input offset of the LMP8640 allows the use of small sense resistors to reduce power dissipation still providing a good input dynamic range. The input dynamic range is the ratio between the maximum signal that can be measured and the minimum signal that can be detected, where usually the input offset is the principal limiting factor.

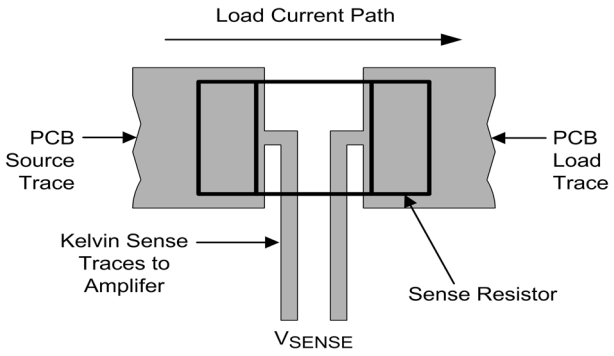


Figure 26. Example of a Kelvin (4-Wire) Connection to a Two-Terminal Resistor

The amplifier inputs should be directly connected to the sense resistor pads using “Kelvin” or “4-wire” connection techniques. The paths of the input traces should be identical, including connectors and vias, so that these errors will be equal and cancel.

Feature Description (continued)

8.3.1.1 Resistor Power Rating and Thermal Issues

The power dissipated by the sense resistor can be calculated from:

$$P_D = I_{MAX}^2 * R_S \quad (4)$$

where

- P_D is the power dissipated by the resistor in Watts
- I_{MAX} is the maximum load current in Amps
- R_S is the sense resistor value in ohms.

The resistor must be rated for more than the expected maximum power (P_D), with margin for temperature derating. Be sure to observe any power derating curves provided by the resistor manufacturer.

Running the resistor at higher temperatures will also affect the accuracy. As the resistor heats up, the resistance generally goes up, which will cause a change in the measurement. The sense resistor should have as much heat-sinking as possible to remove this heat through the use of heatsinks or large copper areas coupled to the resistor pads. A reading drifting slightly after turn-on can usually be traced back to sense resistor heating.

8.3.1.2 Using PCB Trace as a Sense Resistor

While it may be tempting to use the resistance of a known area of PCB trace or copper area as a sense resistor, it is not recommended for precision measurements.

The tempco of copper is typically 3300-4000ppm/°K (0.33% to 0.4% per °C), which can vary with PCB processes.

A typical surface mount sense resistor temperature coefficient (tempco) is in the 50ppm to 500ppm per °C range offering more measurement consistency and accuracy over the copper trace. Special low tempco resistors are available in the 0.1 to 50ppm range, but at a much higher cost.

8.3.2 Sense Line Inputs

The sense lines should be connected to a point on the resistor that is not shared with the main current path, as shown in Figure 26 above. For lowest drift, the amplifier should be mounted away from any heat generating devices, which may include the sense resistor. The traces should be one continuous trace of copper from the sense resistor pad to the amplifier input pin pad, and ideally on the same copper layer with minimal vias or connectors. This can be important around the sense resistor if it is generating any significant heat gradients. Vias in the sense lines should be formed from continuous plated copper and routing through connectors should be avoided. It is better to extend the sense lines than to place the amplifier in a hostile environment.

To minimize noise pickup and thermal errors, the input traces should be treated like a high-speed differential signal pair and routed tightly together with a direct path to the input pins on the same copper layer. They do not need to be "impedance matched", but should follow the same matching rules about vias, spacing and equal lengths. The input traces should be run away from noise sources, such as digital lines, switching supplies or motor drive lines. Remember that these input traces can contain high voltage, and should have the appropriate trace routing clearances to other traces and layers. Since the sense traces only carry the amplifier bias current (typically about 12µA per input at room temp), the connecting input traces can be thin traces running close together. This can help with routing or creating the required spacings.

It should also be noted that, due to the nature of the device topology, the positive input bias current will vary with V_{SENSE} with an extra current approximately equivalent to V_{SENSE} / 5 kΩ on top of the typical 12 uA bias current. The negative input bias current is not in the feedback path and will not change over V_{SENSE}. High or miss-matched source impedances should be avoided as this imbalance will create an additional error over input voltage.

8.3.3 Effects of Series Resistance on Sense Lines

Because the input stage uses precision 5 KΩ resistors internally to convert the voltage on the input pin to a current, any resistance added in series with the input pins will change this resistance, and thus alter the gain.

If a resistance is added in series with an input, the gain of that input will not track that of the other input, causing a constant gain error.

Feature Description (continued)

It is not recommended to use external resistance to alter the gain, as external resistors will not have the same thermal matching as the internal thin film resistors. Any added resistance will severely degrade the offset and CMRR specifications. It is recommended that the total trace resistance be less than 10 ohms.

If resistors are purposely added for filtering, resistance should be added equally to both inputs and the user should be aware that the gain will change slightly.

8.4 Device Functional Modes

8.4.1 Bias Current at Low Common Mode Voltage

At common mode voltages below +2 V, the input bias current starts to reverse and crosses through zero at about +1.8 V. This can be seen in the Input Bias Current graphs in Figure 9 through Figure 11. Negative currents on the graph show curent flow *out* of the input and *into* the load. The graphs show the current for each input, so the actual "bias" current will be twice graph value. This total current could be as high as 1mA, depending on the point of equilibrium.

While this will not affect the vast majority of applications, it may cause MOSFET switched designs with non-linear loads (like LED's or diode-isolated loads) to "float" above ground where the load leakage and bias currents attain equilibrium. A small resistor to ground (on the load supply side) can bleed-off this current.

8.4.2 Applying Input Voltage with No Supply Voltage

The full specified input common mode voltage range may be applied to the inputs while the LMP8640 power is off (V+ = 0 V). When the LMP8640 is powered off, the R_{IN} resistors are disconnected internally by MOSFETS and the leakage currents are very low (sub uA).

The 6 V input differential limit still applies, so at no time should the two inputs be more than 6 V apart. There are also Zener clamps on the inputs to ground, so do not exceed the input limits specified in the Absolute Maximum Ratings.

8.4.3 Driving an ADC

The input stage of an Analog to Digital converter can be modeled with a resistor and a capacitance to ground. So if the voltage source doesn't have a low impedance, an error in amplitude measurement will occur. In this case, a buffer is needed to drive the ADC. The LMP8640 has an internal output buffer able to directly drive a capacitive load up to 30 pF, or, the input stage of an ADC. It is recommended that an external low pass RC filter be added to the output of the LMP8640 to reduce the noise and limit the bandwidth of the current sense measurement.

If the supply voltage of the LMP8640 is higher than the ADC supply voltage, care should be taken to prevent the LMP8640 output from over-driving the ADC input.

This can be accomplished with a series resistance (which should be present when driving a ADC) and a clamping diode to the ADC's power supply. The diode will clamp the ADC input to a safe level. Do not completely rely on a calculated maximum output voltage. Transients or fault conditions outside the normal conditions area can cause the output to swing to a higher than expected voltage.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMP8640x amplifies the voltage developed across a current-sensing resistor.

9.2 Typical Application

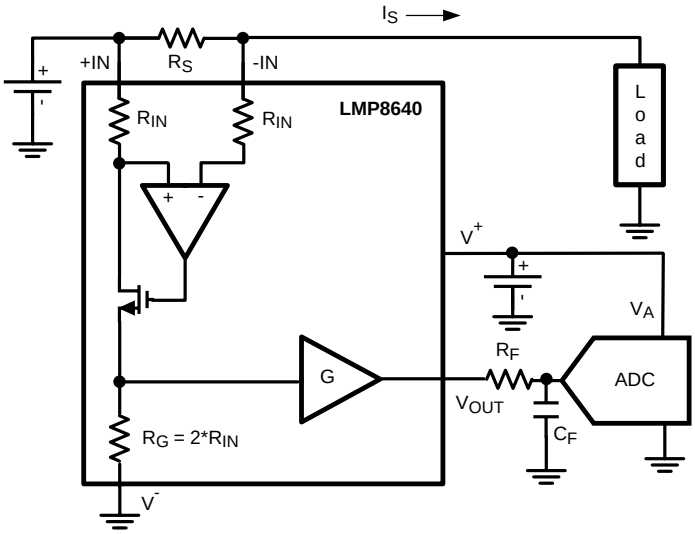


Figure 27. Typical Application Example

9.2.1 Design Requirements

In this example, a current monitor application is required to measure the current into a load (peak current 10 A) with a resolution of 10 mA and 0.5% of accuracy.

The 10bit analog to digital converter accepts a max input voltage of 4.1 V. In order to not burn too much power on the shunt resistor, it needs to be less than 10 mΩ. Table 1 below summarizes the other design conditions.

Table 1. Example Design Requirements

WORKING CONDITION	VALUE	
	MIN	MAX
Supply Voltage	5 V	5.5 V
Common mode Voltage	48 V	70 V
Temperature	0°C	70°C
Signal BW	50 kHz	

9.2.2 Design Procedure

9.2.2.1 First Step – LMP8640 or LMP8640HV Selection

The required common mode voltage of the application implies that the right choice is the LMP8640HV (High common mode voltage up tp 76 V).

9.2.2.2 Second Step – Gain Option Selection

We can choose between three gain option (20 V/V, 50 V/V, 100 V/V). Considering the max input voltage of the ADC (4.1 V) , the max Sense voltage across the shunt resistor is evaluated according the following formula:

V_{SENSE}= (MAX Vin ADC) / Gain; (5)

hence the max V_{SENSE} will be 205 mV, 82 mV, 41 mV respectively. The shunt resistor are then evaluated considering the maximum monitored current :

R_S = (max V_{SENSE}) / I_MAX (6)

For each gain option the max shunt resistors are the following : 20.5 mΩ, 8.2 mΩ, 4.1 mΩ respectively.

One of the project constraints requires RS<10 mΩ, it means that the 20.5 mΩ will be discarded and hence the 50 V/V and 100 V/V gain options are still in play.

9.2.2.3 Third Step – Shunt Resistor Selection

At this point an error budget calculation, considering the calibration of the Gain, Offset, CMRR, and PSRR, helps in the selection of the shunt resistor. In the table below the contribution of each error source is calculated considering the values of the Electrical Characteristics table at 5 V supply.

Table 2. Resolution Calculation

ERROR SOURCE	R_S = 4.1 mΩ	R_S = 8.1 mΩ
CMRR calibrated at mid VCM range	77.9 µV	77.9 µV
PSRR calibrated at 5 V	8.9 µV	8.9 µV
Total error (squared sum of contribution)	78 µV	78 µV
Resolution (Total error / R_S)	19.2 mA	9.6 mA

Table 3. Accuracy Calculation

ERROR SOURCE	R_S = 4.1 mΩ	R_S = 8.1 mΩ
Tc Vos	182 µV	182 µV
Nosie	216 µV	216 µV
Gain drift	75.2 µV	151 µV
Total error (squared sum of contribution)	293 µV	320 µV
Accuracy 100*(Max_V_{SENSE} / Total Error)	0.7%	0.4%

From the tables above is clear that the 8.2 mΩ shunt resistor allows the respect of the project's constraints. The power burned on the Shunt is 820 mW at 10 A.

9.2.3 Application Performance Plot

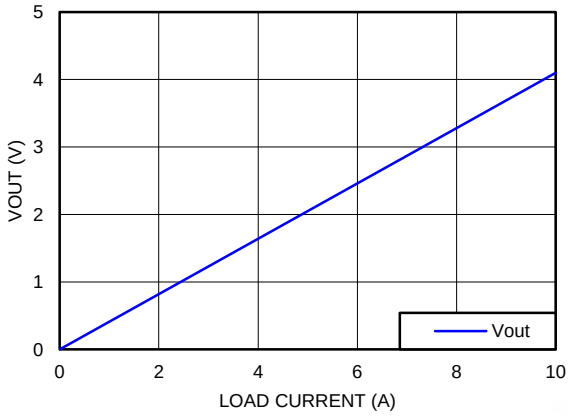


Figure 28. Application Example Results using 8.2 mΩ Resistor

9.3 Do's and Don'ts

Do properly bypass the power supplies.

Do add series resistance to the output when driving capacitive loads, cables, long traces, muxes and ADC inputs.

Do not exceed the input common mode range.

10 Power Supply Recommendations

The input circuitry of the device can accurately measure signals on common-mode voltages beyond its power supply voltage, V^+. For example, the voltage applied to the VS power supply terminal can be 5 V, whereas the load power-supply voltage being monitored (the common-mode voltage) can be as high as +76 V. Power-supply bypass capacitors are required for stability and should be placed as closely as possible to the supply and ground terminals of the device. A typical value for this supply bypass capacitor is 0.1 µF close to the V^+ pin. The capacitors should be rated for at least twice the maximum expected applied voltage. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

11 Layout

11.1 Layout Guidelines

- Use 4-wire (Kelvin) connections to the sense resistor. Connect to the resistor at a point that is not within a direct high-current path (See Figure 29).
- Do not "share" part of the sense trace path with the load current.
- Maintain proper clearance and spacings around the input traces, as they may be at a higher voltage (up to 76 V) than the surrounding traces and planes.
- Input traces from the sense resistor pads should follow the same path, be spaced tightly together, and ideally on the same copper layer.
- Vias used in the input traces should be of continuous plated copper to avoid creating thermocouples.
- Avoid routing inputs through jumpers and connectors. Even the best connectors introduce thermal errors ("thermocouples"). Each input trace should have the same number of "thermocouples" if they cannot be avoided.
- Keep the amplifier away from heat generating devices. The copper-solder-lead junction on the input pins will form a thermocouple. The copper mass should be equal on both input pins.
- Avoid temperature gradients across the input pins. Input pins should be equal distance to the heat source.
- Place the LMP8640 in the most temperature-stable area possible and away from high-velocity air flows. It is better to carefully extend the input traces than to place the amplifier in a less-than-ideal environment.
- Give the sense resistor as much copper trace area as possible to dissipate heat as the resistor value will change slightly with temperature. Also see the resistor manufacturers datasheet or application notes for further layout guidelines.
- The power-supply bypass capacitor should be placed as closely as possible to the supply and ground terminals. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

11.2 Layout Example

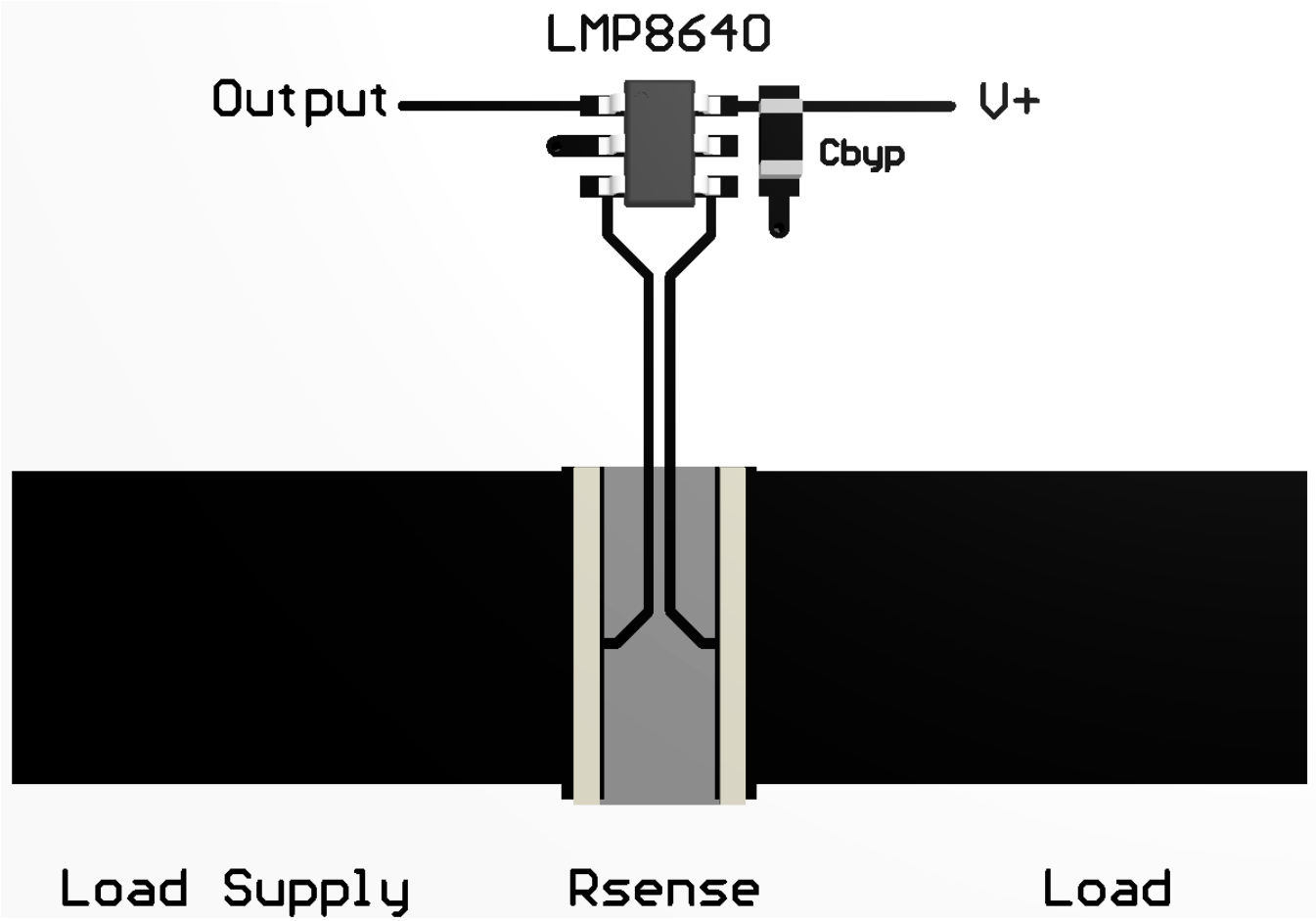


Figure 29. Layout Example - Kelvin Connection to a Two-Terminal Resistor

Layout Example (continued)

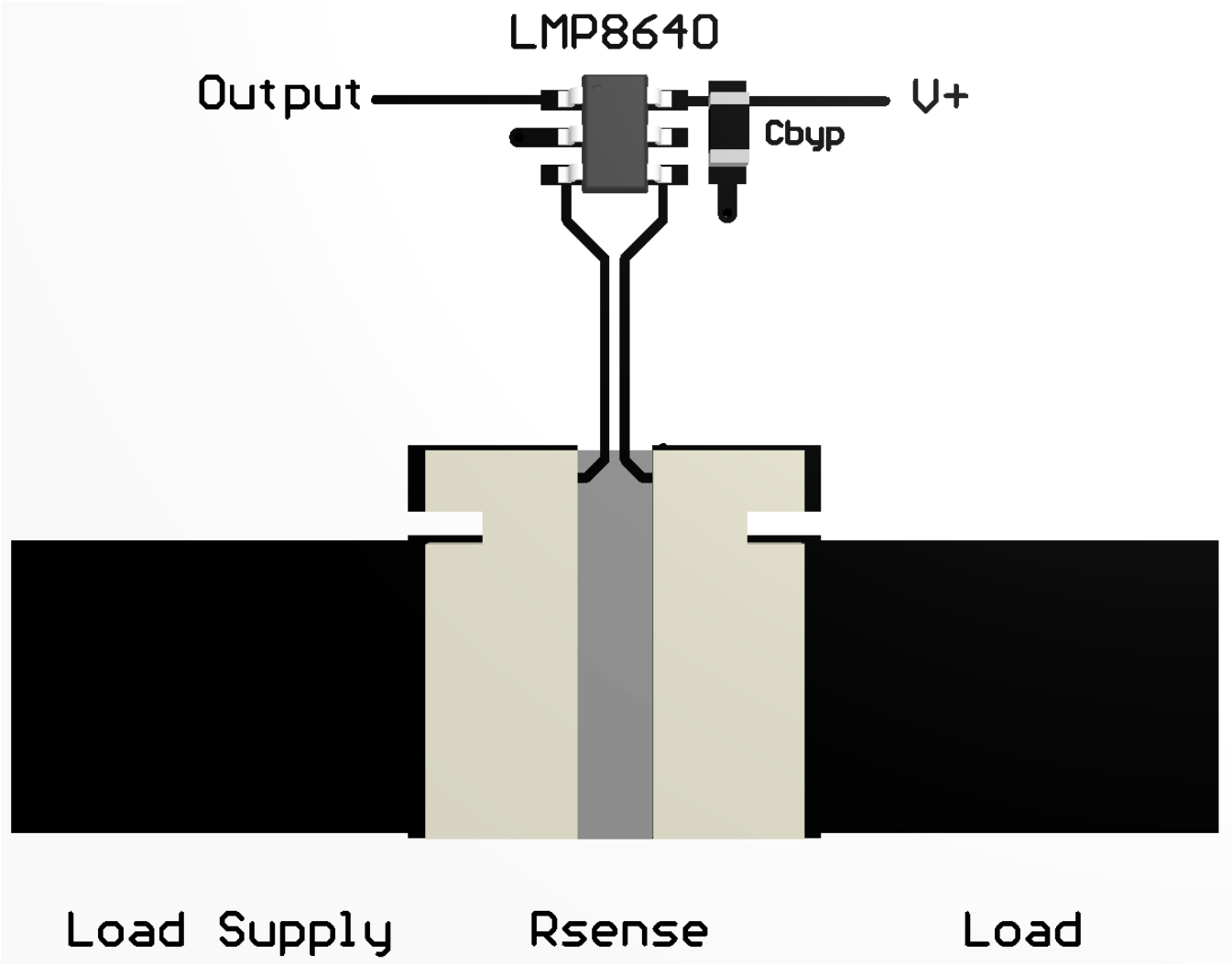


Figure 30. Layout Example - Four-Wire (Kelvin) Resistor Connection

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

- Evaluation Board for LMP8640HV-F, http://www.ti.com/tool/lmp8640hv-feval
- Evaluation Board for LMP8640HV-H, http://www.ti.com/tool/lmp8640hv-heval
- Evaluation Board for LMP8640HV-T, http://www.ti.com/tool/lmp8640hv-teval
- TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti

12.2 Documentation Support

12.2.1 Related Documentation

For related documantation, see the following:

- AN-1975 LMP8640 / LMP8645 Evaluation Board User Guide, SNOA546
- Absolute Maximum Ratings for Soldering, SNOA549

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMP8640	Click here	Click here	Click here	Click here	Click here
LMP8640-Q1	Click here	Click here	Click here	Click here	Click here
LMP8640HV	Click here	Click here	Click here	Click here	Click here

12.4 Trademarks

All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP8640HVMK-F/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD6A	Samples
LMP8640HVMK-H/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AF6A	Samples
LMP8640HVMK-T/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AB6A	Samples
LMP8640HVMKE-F/NOPB	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD6A	Samples
LMP8640HVMKE-H/NOPB	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AF6A	Samples
LMP8640HVMKE-T/NOPB	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AB6A	Samples
LMP8640HVMKX-F/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AD6A	Samples
LMP8640HVMKX-H/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AF6A	Samples
LMP8640HVMKX-T/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AB6A	Samples
LMP8640MK-F/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC6A	Samples
LMP8640MK-H/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AE6A	Samples
LMP8640MK-T/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AA6A	Samples
LMP8640MKE-F/NOPB	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC6A	Samples
LMP8640MKE-H/NOPB	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AE6A	Samples
LMP8640MKE-T/NOPB	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AA6A	Samples
LMP8640MKX-F/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC6A	Samples
LMP8640MKX-H/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AE6A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP8640MKX-T/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AA6A	Samples
LMP8640QMKE-T/NOPB	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AUAA	Samples
LMP8640QMKX-T/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AUAA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMP8640, LMP8640-Q1 :

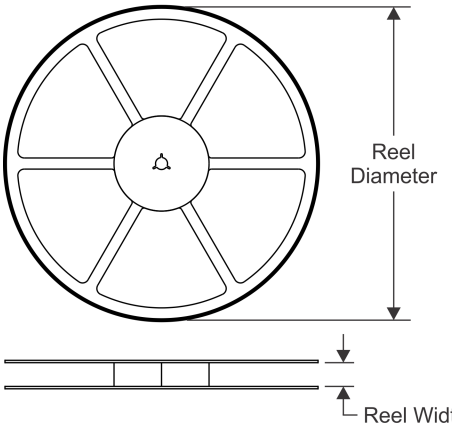
- Catalog: LMP8640
- Automotive: LMP8640-Q1

NOTE: Qualified Version Definitions:

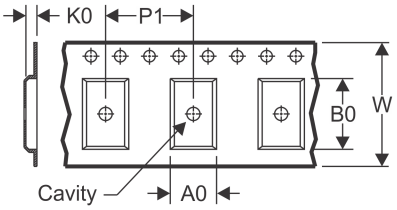
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

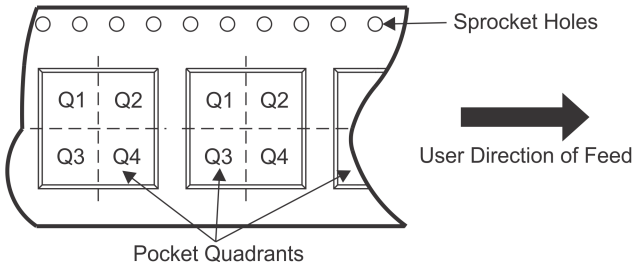


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

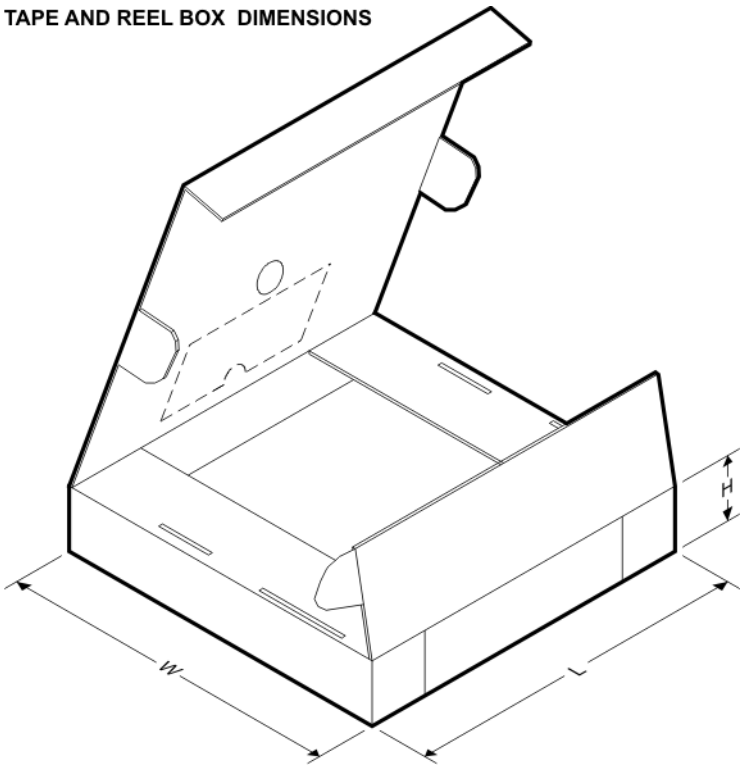


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP8640HVMK-F/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640HVMK-H/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640HVMK-T/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640HVMKE-F/NOPB	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640HVMKE-H/NOPB	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640HVMKE-T/NOPB	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640HVMKX-F/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640HVMKX-H/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640HVMKX-T/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640MK-F/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640MK-H/NOPB	SOT-	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	23-THIN											
LMP8640MK-T/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640MKE-F/NOPB	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640MKE-H/NOPB	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640MKE-T/NOPB	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640MKX-F/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640MKX-H/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640MKX-T/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640QMKE-T/NOPB	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMP8640QMKX-T/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

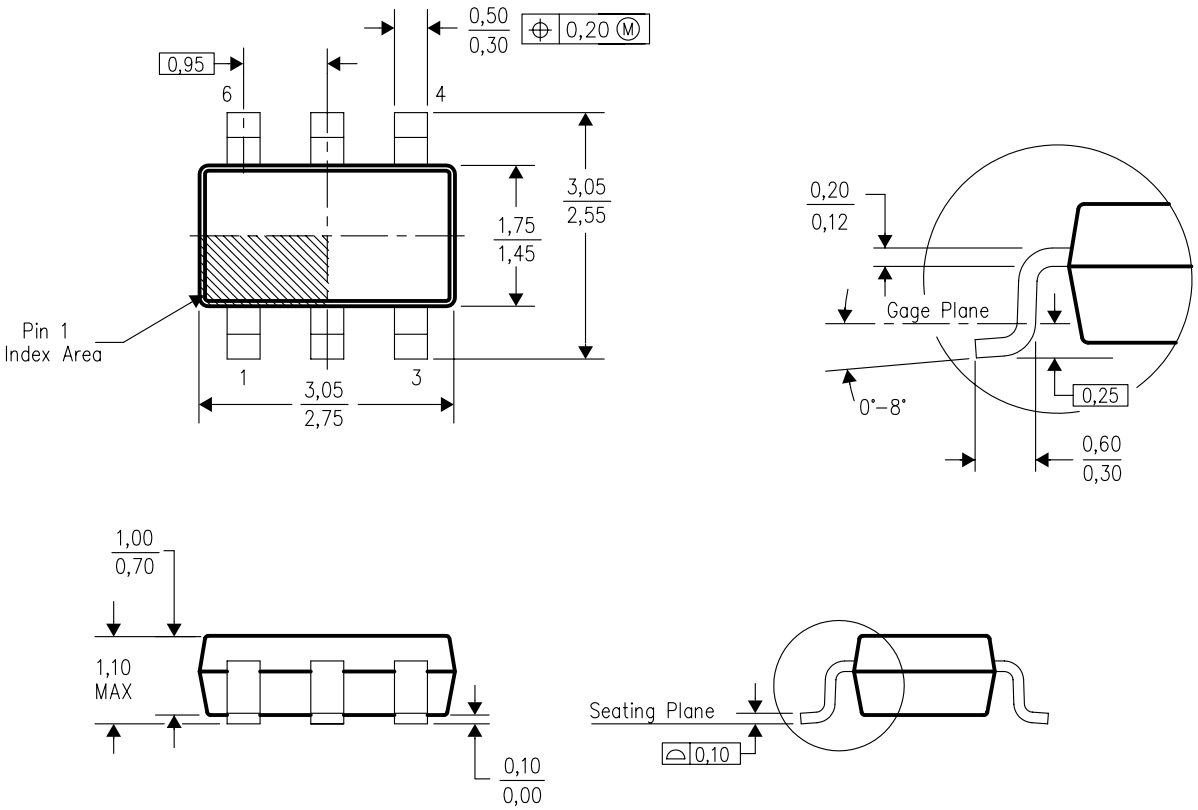


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP8640HVMK-F/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP8640HVMK-H/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
LMP8640HVMK-T/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
LMP8640HVMKE-F/NOPB	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
LMP8640HVMKE-H/NOPB	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
LMP8640HVMKE-T/NOPB	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
LMP8640HVMKX-F/NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMP8640HVMKX-H/NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMP8640HVMKX-T/NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMP8640MK-F/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
LMP8640MK-H/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
LMP8640MK-T/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
LMP8640MKE-F/NOPB	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
LMP8640MKE-H/NOPB	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
LMP8640MKE-T/NOPB	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
LMP8640MKX-F/NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMP8640MKX-H/NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMP8640MKX-T/NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
LMP8640QMKE-T/NOPB	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
LMP8640QMKX-T/NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0

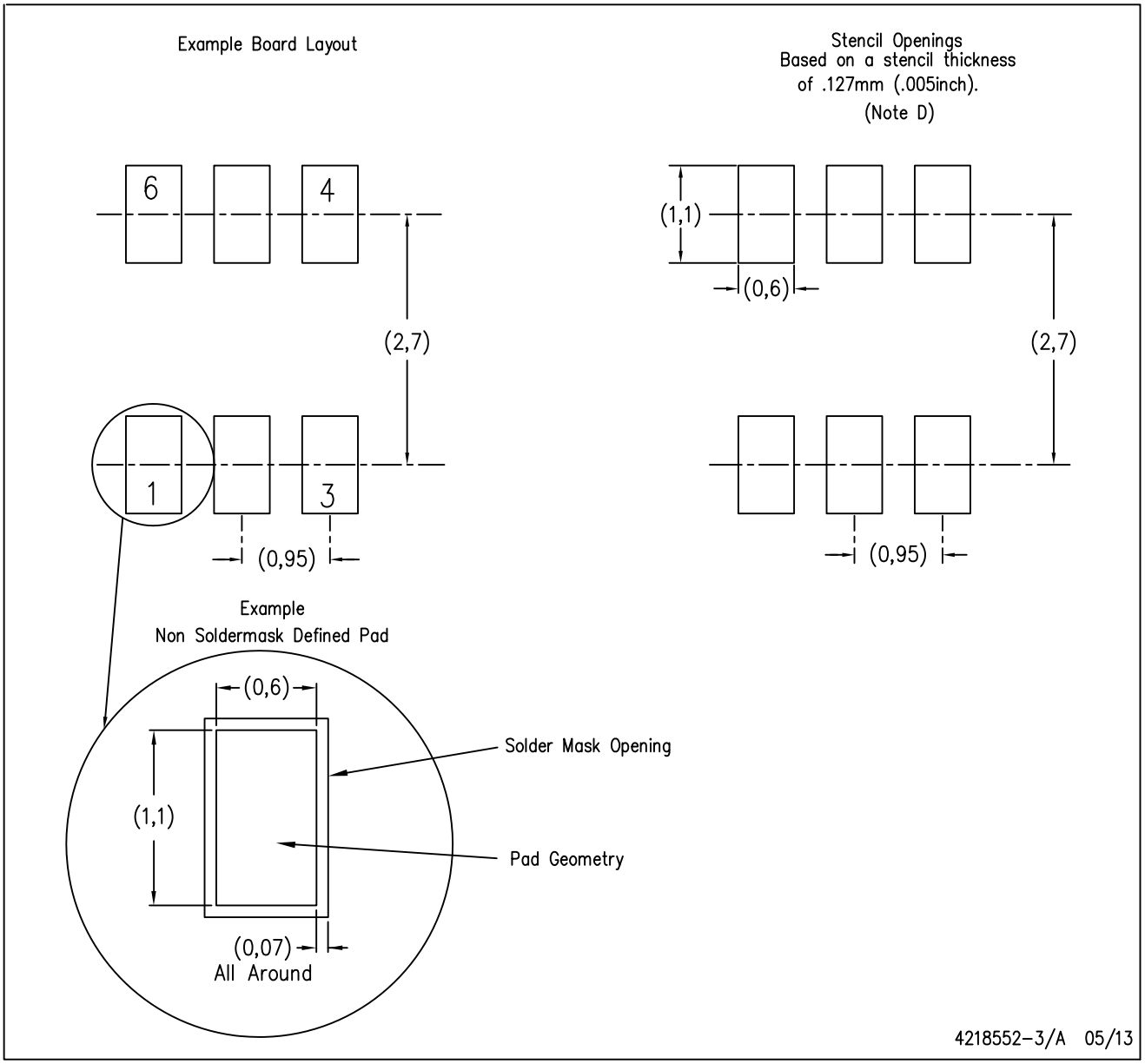
DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE



4204403–3/E 06/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AA (6 pin).

DDC (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

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