AUTOMOTIVE GRADE

CS8121

5V, 1A Linear Regulator with $\overline{\text{RESET}}$ and $\overline{\text{ENABLE}}$

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DEVICE NOT RECOMMENDED FOR NEW DESIGN

Description

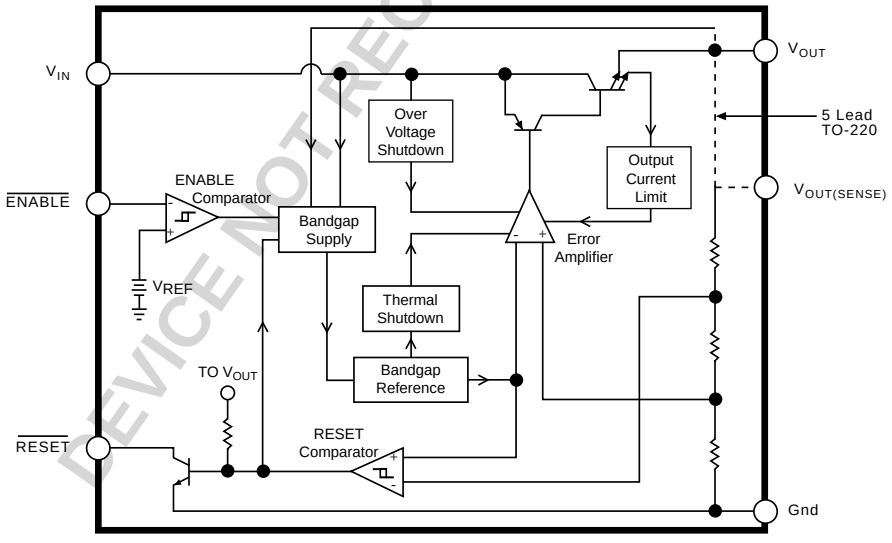
The CS8121 is a 5V, 1A precision linear regulator with two microprocessor compatible control functions and protection circuitry included on chip. The composite NPN-PNP output pass transistor assures a lower dropout voltage (1.2V @ 1A) without requiring excessive supply current (4mA).

The CS8121's two logic control functions make this regulator well suited to applications requiring microprocessor-based control at the board or module level. $\overline{\text{ENABLE}}$ controls the output stage. A high voltage (>2.9V) on the $\overline{\text{ENABLE}}$ lead turns off the regulator's pass transistor and sends the IC into Sleep mode where it draws only 250µA. $\overline{\text{RESET}}$ sends a $\overline{\text{RESET}}$ signal when the IC is powering up or whenever the output voltage falls out of regulation. The $\overline{\text{RESET}}$ signal is valid down to V_{OUT} = 1V.

The CS8121 design optimizes supply rejection by switching the internal bandgap reference from the supply input to the regulator output as soon as the nominal output voltage is achieved. Additional on chip filtering enhances rejection of high frequency transients on all external leads.

The CS8121 is fault protected against short circuit, over voltage and thermal runaway conditions.

Block Diagram

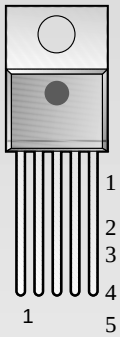


Features

- **5V ± 4% Output Voltage**
- **Low Dropout Voltage (1.2V @ 1A)**
- **Low Quiescent Current (4mA @ I_{OUT} = 1A)**
- **µP Compatible Control Functions**
  - **$\overline{\text{RESET}}$**
  - **$\overline{\text{ENABLE}}$**
- **Low Current Sleep Mode I_Q = 250µA**
- **Fault Protection**
  - **Thermal Shutdown**
  - **Short Circuit**
  - **60V Peak Transient Voltage**

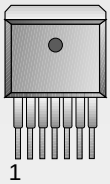
Package Options

5 Lead TO-220



1 V_{IN}
2 $\overline{\text{ENABLE}}$
3 Gnd
4 $\overline{\text{RESET}}$
5 V_{OUT}

7 Lead D²PAK



1 NC
2 V_{IN}
3 $\overline{\text{ENABLE}}$
4 Gnd
5 $\overline{\text{RESET}}$
6 V_{OUT}
7 $V_{OUT(SENSE)}$

ON Semiconductor

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Absolute Maximum Ratings

DC Input Voltage .....-0.7 to 26V
Peak Transient Voltage (46V Load Dump).....60V
Output Current .....Internally Limited
Electrostatic Discharge (Human Body Model).....2kV
Operating, Temperature .....-40C to 125°C
Junction Temperature.....-40C to 150°C
Storage Temperatures.....-55°C to 150°C
Lead Temperature Soldering
Wave Solder (through hole styles only) .....10 sec. max, 260°C peak
Reflow (SMD styles only) .....60 sec. max above 183°C, 230°C peak

Electrical Characteristics: I_{OUT} = 5mA, -40°C ≤ T_J ≤150°C , 7V ≤ V_{IN} ≤ 26V, -40°C ≤ T_A ≤ 125°C unless otherwise specified

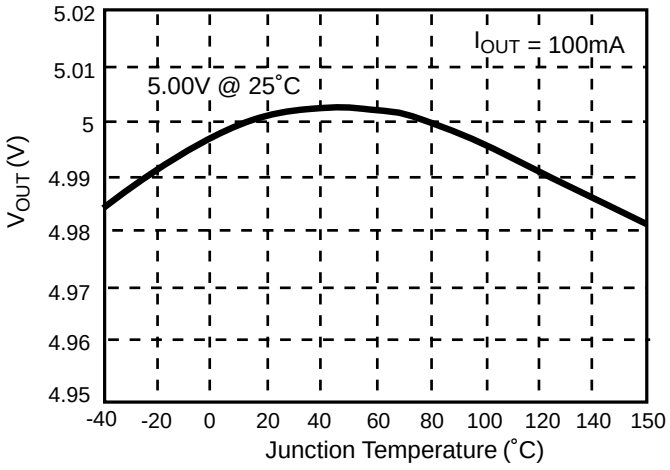
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Output Stage					
Output Voltage, V_{OUT}	7V ≤ V_{IN} ≤ 26V, 1mA ≤ I_{OUT} ≤ 1A	4.8	5.0	5.2	V
Line Regulation	7V ≤ V_{IN} ≤ 26V, I_{OUT} = 5mA		0	50	mV
Load Regulation	5mA ≤ I_{OUT} ≤ 1A		10	70	mV
Supply Voltage Rejection	V_{IN} = 14V_{DC} + 1V_{RMS} @120Hz, I_{LOAD} = 50Ω	54	70		dB
Dropout Voltage	I_{OUT} = 1A		1.2	1.8	V
Quiescent Current	$\overline{ENABLE}$ = High, V_{IN} = 12V $\overline{ENABLE}$ = Low, I_{OUT} = 1A		0.25 4	0.65 20	mA mA
■ Protection Circuits					
Short Circuit Current			1.5		A
Thermal Shutdown		150	190		°C
Overvoltage Shutdown		26	40		V
■ $\overline{RESET}$					
$\overline{RESET}$ Saturation Voltage	1V < V_{OUT} < $V_{RT(OFF)}$, 3.1kΩ pull-up to V_{OUT}		0.1	0.4	V
$\overline{RESET}$ Output Leakage Current	$\overline{ENABLE}$ = Low V_{OUT} > $V_{RT(ON)}$, $V_{\overline{RESET}}$ = V_{OUT}		0	25	µA
Power ON / OFF $\overline{RESET}$ Peak Output Voltage	3.1kΩ pull-up to V_{OUT}		0.7	1.0	V
$\overline{RESET}$ Threshold ON (V_{OUT} Increasing)			V_{OUT} - 0.10	V_{OUT} - 0.04	V
$\overline{RESET}$ Threshold OFF (V_{OUT} Decreasing)		4.75	V_{OUT} - 0.14		V
$\overline{RESET}$ Threshold Hysteresis		10	40		mV
■ $\overline{ENABLE}$					
Input High Voltage	7V < V_{IN} < 26V		2.9	3.9	V
Input Low Voltage	7V < V_{IN} < 26V	1.1	2.1		V
Input Hysteresis	7V < V_{IN} < 26V	0.4	0.8	2.8	V
Input Current	Gnd < $V_{IN(HI)}$ < V_{OUT}		0	±10	µA

Package Lead Description

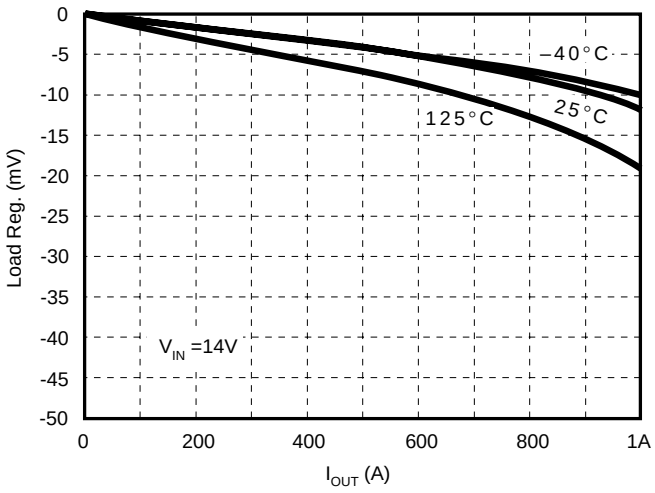
PACKAGE LEAD #		LEAD SYMBOL	FUNCTION
7 Lead D²PAK	**5 Lead TO-220**		
1		NC	No Connection.
2	1	V_{IN}	Supply voltage to IC, usually direct from the battery.
3	2	$\overline{ENABLE}$	CMOS compatible logical. V_{OUT} is disabled i.e. placed in a high impedance state when ENABLE is high.
4	3	Gnd	Ground connection.
5	4	$\overline{RESET}$	CMOS compatible output lead. $\overline{RESET}$ goes low whenever V_{OUT} falls out of regulation. The $\overline{RESET}$ delay is externally programmed.
6	5	V_{OUT}	Regulated output voltage, 5V (typ).
7		$V_{OUT(SENSE)}$	Remote sensing of output voltage.

Typical Performance Characteristics

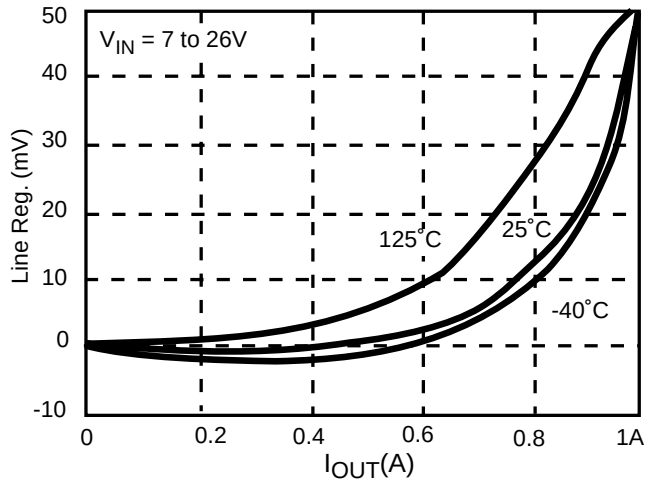
Output Voltage vs. Temperature



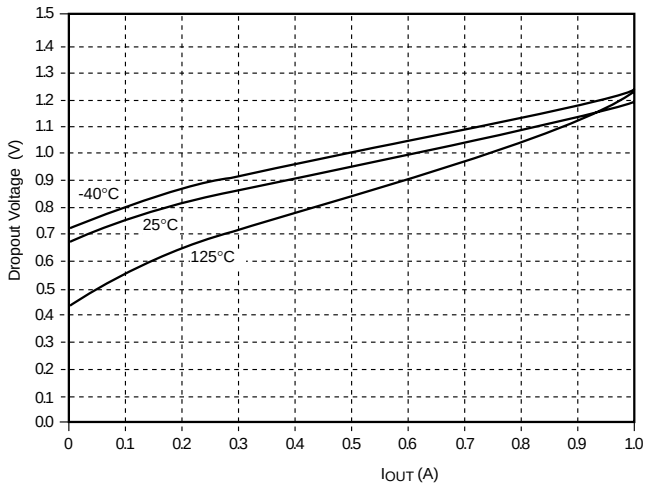
Load Regulation vs. Output Current Over Temperature



Line Regulation vs. Output Current Over Temperature

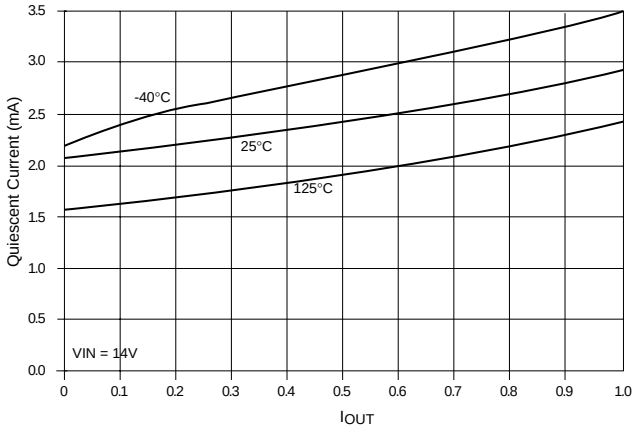


Dropout Voltage vs. Output Current Over Temperature

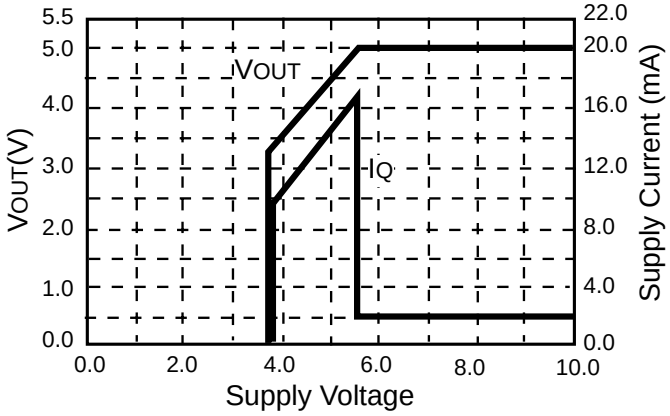


Typical Performance Characteristics: continued

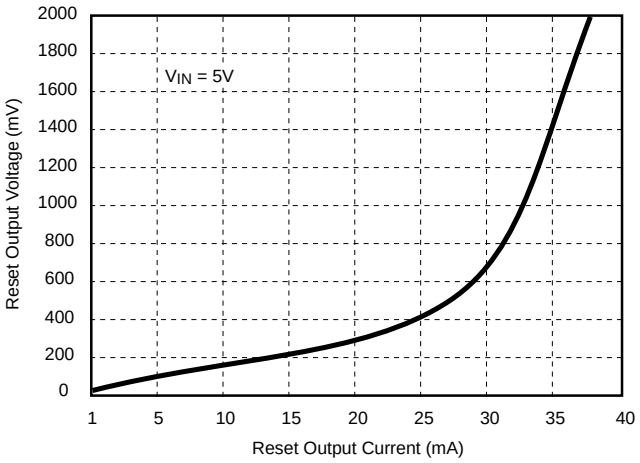
Quiescent Current vs. Output Current Over Temperature



Output Voltage and Supply Current vs. Input Voltage



$\overline{\text{RESET}}$ Output Voltage vs. Output Current



Circuit Description

Voltage Reference and Output Circuitry

Precision Voltage Reference

The regulated output voltage depends on the precision band gap voltage reference in the IC. By adding an error amplifier into the feedback loop, the output voltage is maintained within ±4% over temperature and supply variation.

Output Stage

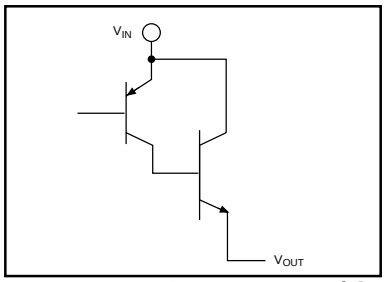


Figure 1. Composite Output Stage of the CS8121

The composite PNP-NPN output structure (Figure 1) provides 1A (typ) of output current while maintaining a low drop out voltage (1.2V) and drawing little quiescent current (4mA).

The NPN pass device prevents deep saturation of the output stage which in turn improves the IC's efficiency by preventing excess current from being used and dissipated by the IC.

Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 2).

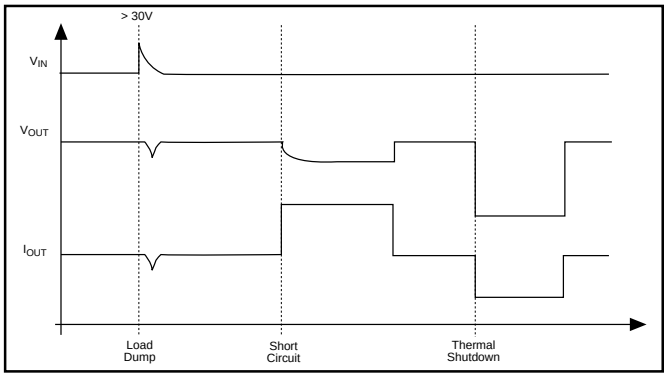


Figure 2. Typical Circuit Waveforms for Output Stage Protection.

Circuit Description: continued

If the input voltage rises above 30V (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.

Using an emitter sense scheme, the amount of current through the NPN pass transistor is monitored. Feedback circuitry insures that the output current never exceeds a preset limit.

Should the junction temperature of the power device exceed 180°C (typ) the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.

Regulator Control Functions

The CS8121 contains two microprocessor compatible control functions: $\overline{\text{ENABLE}}$ and $\overline{\text{RESET}}$ (Figure 3).

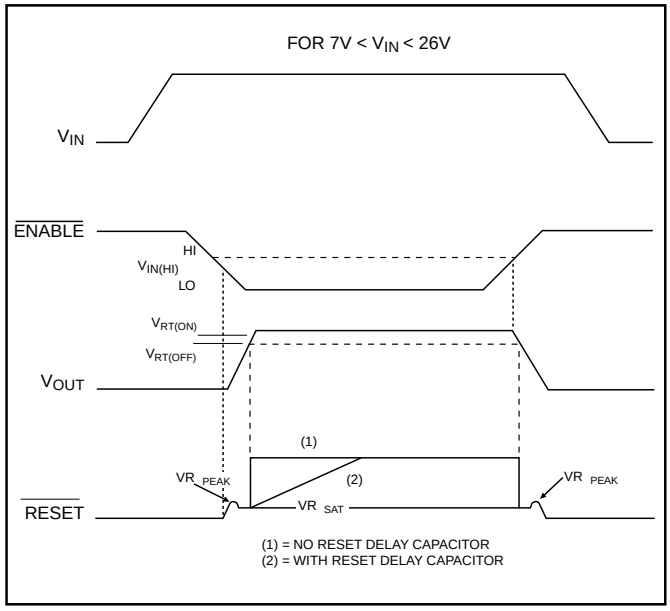


Figure 3. Circuit Waveforms for the CS8121

$\overline{\text{ENABLE}}$ Function

The $\overline{\text{ENABLE}}$ function switches the output transistor. When the voltage on the $\overline{\text{ENABLE}}$ lead exceeds 2.9V typ, the output pass transistor turns off, leaving a high impedance facing the load. The IC will remain in Sleep mode, drawing only 250µA, until the voltage on the lead drops below 2.1V typ. Hysteresis (800mV) is built into the $\overline{\text{ENABLE}}$ function to provide good noise immunity.

$\overline{\text{RESET}}$ Function

A $\overline{\text{RESET}}$ signal (low voltage) is generated as the IC powers up ($V_{OUT} > V_{OUT}$ - 100mV) or when V_{OUT} drops out of regulation ($V_{OUT} < V_{OUT}$ - 140mV, typ). 40mV of hysteresis is included in the function to minimize oscillations.

The $\overline{\text{RESET}}$ output is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC, thereby guaranteeing that the RESET signal is valid for V_{OUT} as low as 1V.

An external RC network on the $\overline{\text{RESET}}$ lead (Figure 4) provides a sufficiently long delay for most microprocessor based applications. RC values can be chosen using the following formula:

$$R_{TOT} \times C_{RST} \left[\frac{-t_{Delay}}{\ln \left(\frac{V_T - V_{OUT}}{V_{RST} - V_{OUT}} \right)} \right]$$

where:

R_{TOT} = R_{RST} in parallel with R_{IN},
R_{IN} = µP port impedance,
C_{RST} = $\overline{\text{RESET}}$ delay capacitor,
t_{Delay} = desired delay time,
V_{RST} = V_{SAT} of $\overline{\text{RESET}}$ lead (0.7V @ turn - on), and
V_T = µP logic threshold voltage.

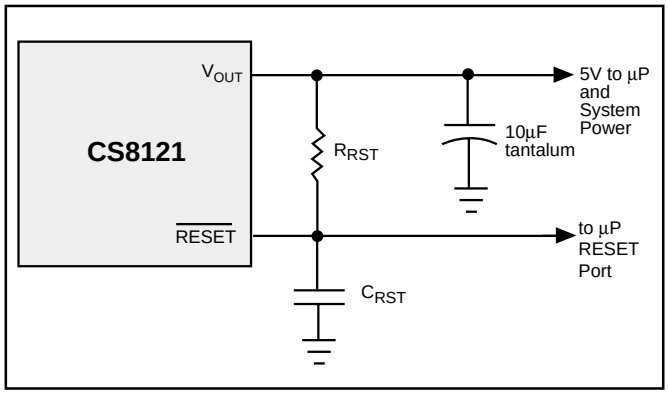


Figure 4. RC Network for $\overline{\text{RESET}}$ Delay

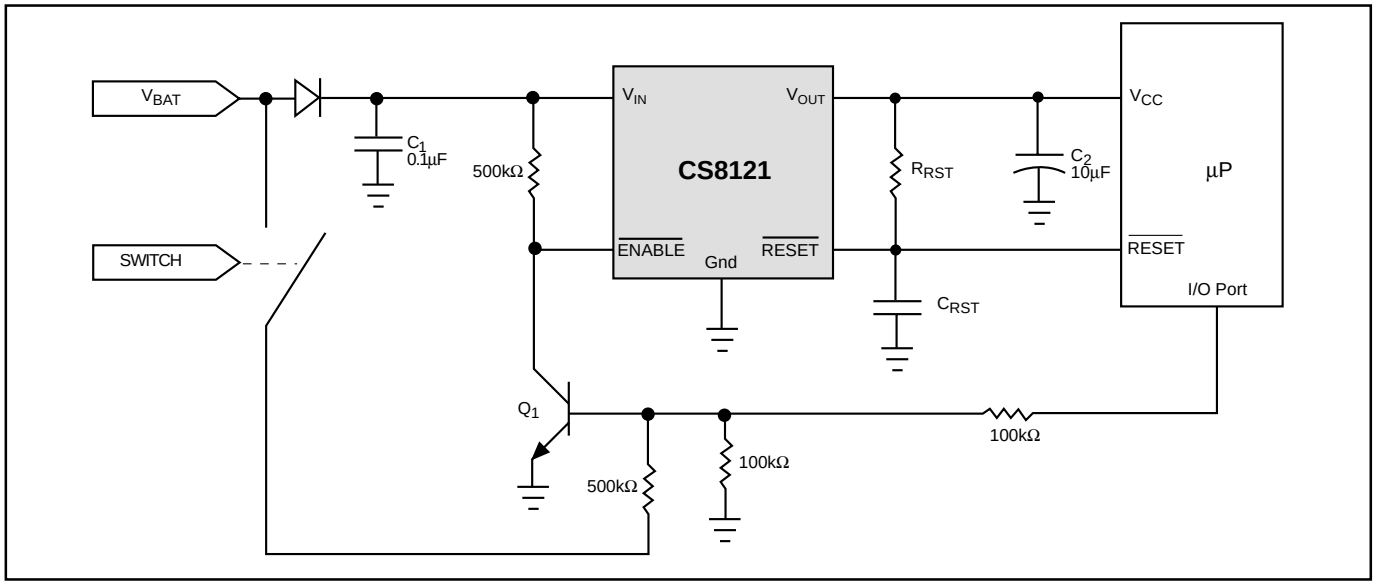


Figure 5. Microprocessor control of CS8121 using external switching transistor Q1.

The circuit depicted in Figure 5 lets the microprocessor control its power source, the CS8121 regulator. An I/O port on the µP and the SWITCH port are used to drive the base of Q1. When Q1 is driven into saturation, the voltage on the $\overline{\text{ENABLE}}$ lead falls below its lower threshold and the regulator's output is switched on. When the drive current is removed, the voltage on the $\overline{\text{ENABLE}}$ lead rises, the output is switched off and the IC moves into Sleep mode where it typically draws 250µA.

By coupling these two controls with $\overline{\text{ENABLE}}$, the system has added flexibility. Once the system is running, the state of the SWITCH is irrelevant as long as the I/O port continues to drive Q1. The µP can turn off its own power by withdrawing drive current, once the SWITCH is open. This software control at the I/O port allows the µP to finish key housekeeping functions before power is removed.

The logic options are summarized in Table 1 below

Table 1: Logic Control of CS8121 Output

µP I/O drive	SWITCH	$\overline{\text{ENABLE}}$	Output
ON	Closed	LOW	ON
	Open	LOW	ON
OFF	Closed	LOW	ON
	Open	HIGH	OFF

The I/O port of the µP typically provides 50 µA to Q1. In automotive applications the SWITCH is connected to the ignition switch.

Stability Considerations

The output or compensation capacitor C_2 helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (-25°C to -40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor C_2 shown in the test and applications circuit should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for C_2 for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

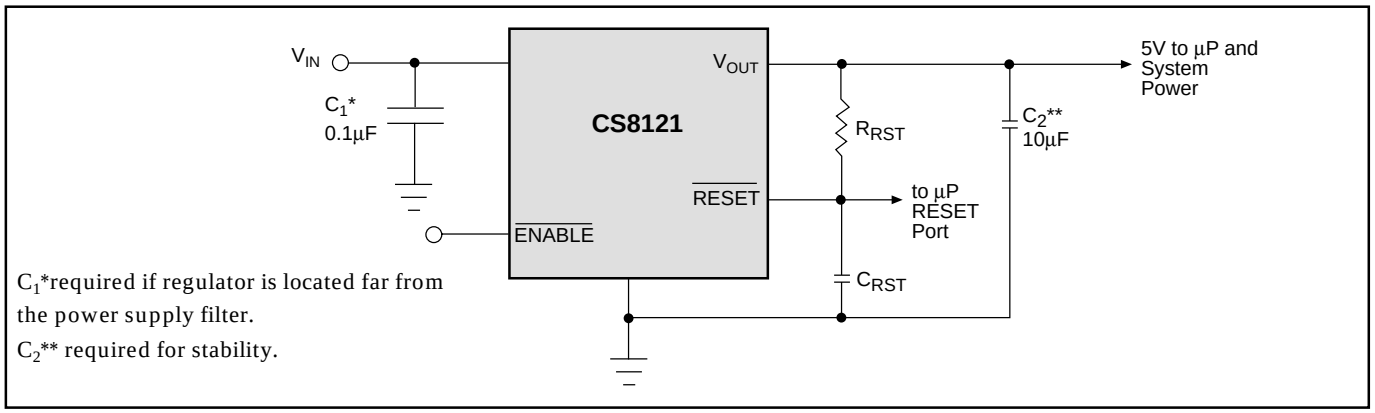


Figure 6: Test and application circuit showing output compensation.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Remove the unit from the environmental chamber and heat the IC with a heat gun. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of + / - 20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 7) is:

$$P_{D(max)} = |V_{IN(max)} - V_{OUT(min)}|I_{OUT(max)} + V_{IN(max)}I_Q \qquad (1)$$

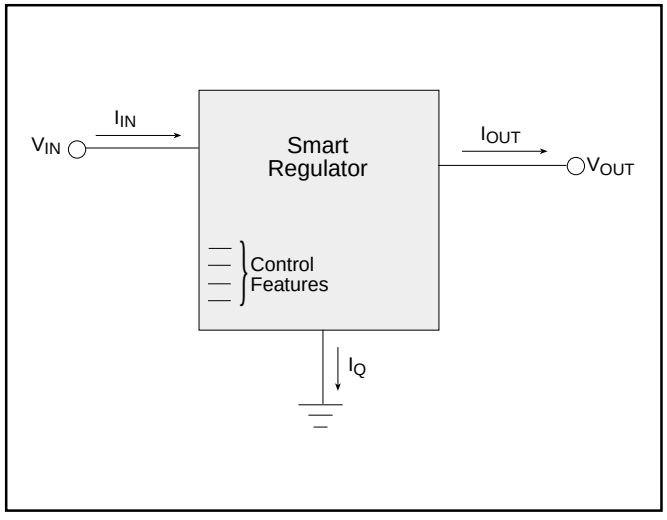


Figure 7: Single output regulator with key performance parameters labeled.

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150°C - T_A}{P_D} \qquad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \qquad (3)$$

where:

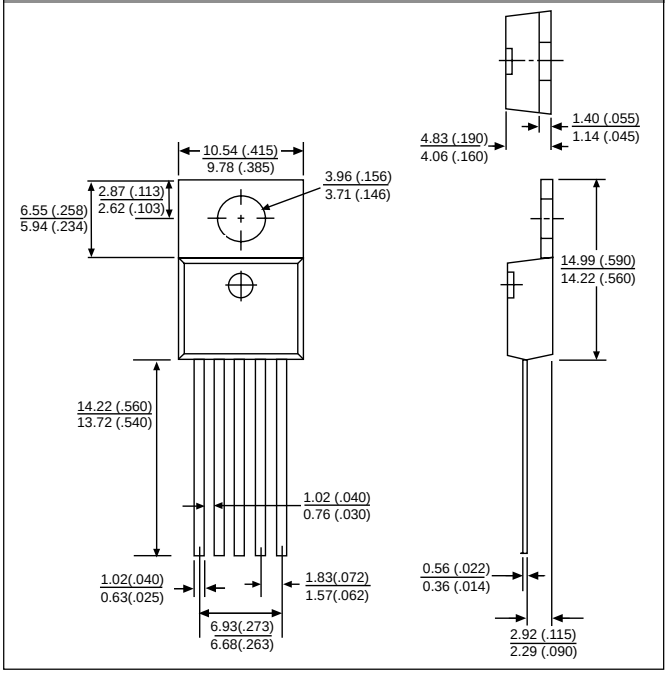
$R_{\Theta JC}$ = the junction–to–case thermal resistance,
$R_{\Theta CS}$ = the case–to–heatsink thermal resistance, and
$R_{\Theta SA}$ = the heatsink–to–ambient thermal resistance.

$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it too is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

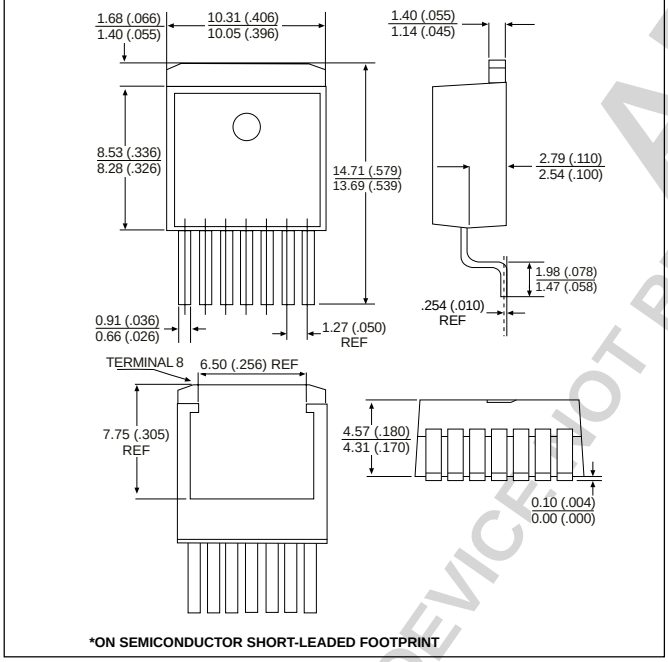
Package Specification

PACKAGE DIMENSIONS IN mm (INCHES)

5 Lead TO-220 (T) Straight



7 Lead D²PAK (DPS)* Short-Leaded



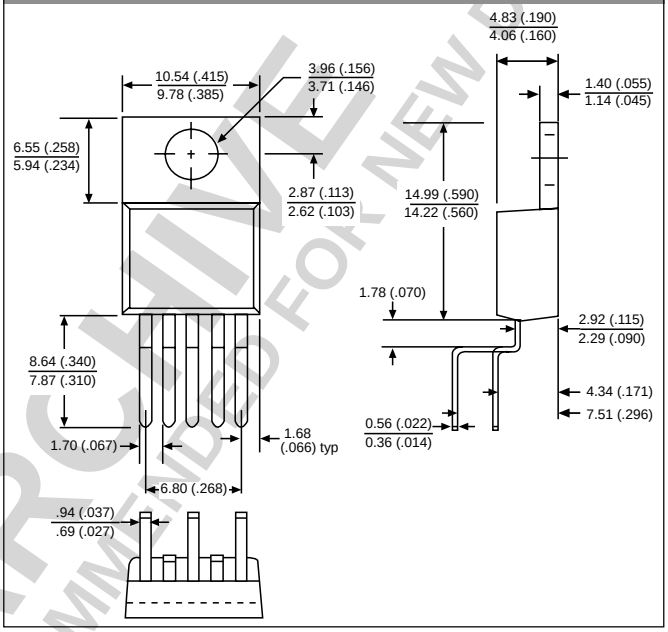
*ON SEMICONDUCTOR SHORT-LEADED FOOTPRINT

PACKAGE THERMAL DATA

Thermal Data		5 Lead TO-220	7 Lead D²PAK	
$R_{\Theta JC}$	typ	2.5	2.5	°C / W
$R_{\Theta JA}$	typ	50	10-50*	°C / W

**Depending on thermal properties of substrate,* $R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CA}$.

5 Lead TO-220 (TVA) Vertical



Ordering Information

Part Number	Description
CS8121YT5	5 Lead TO-220 Straight
CS8121YTVA5	5 Lead TO-220 Vertical
CS8121YTHA5	5 Lead TO-220 Horizontal
CS8121YDPS7	7 Lead D²PAK Short-Leaded
CS8121YDPSR7	7 Lead D²PAK Short-Leaded *(tape & reel)*

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