National Semiconductor

February 1990

LM2926/LM2927
Low Dropout Regulator with Delayed Reset

General Description

The LM2926 is a 5V, 500 mA, low dropout regulator with delayed reset. The microprocessor reset flag is set low by thermal shutdown, short circuits, overvoltage conditions, dropout, and power-up. After the fault condition is corrected, the reset flag remains low for a delay time determined by the delay capacitor. Hysteresis is included in the reset circuit to prevent oscillations, and a reset output is guaranteed down to 3.2V supply input. A latching comparator is used to discharge the delay capacitor, which guarantees a full reset pulse even when triggered by a relatively short fault condition. A patented quiescent current reduction circuit drops the ground pin current to 8 mA at full load when the input-output differential is 3V or more.

Familiar PNP regulator features such as reverse battery protection, transient protection, and overvoltage shutdown are included in the LM2926 making it suitable for use in automotive and battery operated equipment.

The LM2927 is electrically identical to the LM2926 but has a different pin-out. The LM2927 is pin-for-pin compatible with the L4947 and TLE4260 alternatives. The LM2926 is pin-for-pin compatible with the LM2925.

Features

- 5% output accuracy over entire operating range
- Dropout voltage typically 350 mV at 500 mA output
- Externally programmed reset delay
- Short circuit proof
- Reverse battery proof
- Thermally protected
- LM2926 is pin-for-pin compatible with the LM2925
- 100% electrical burn-in

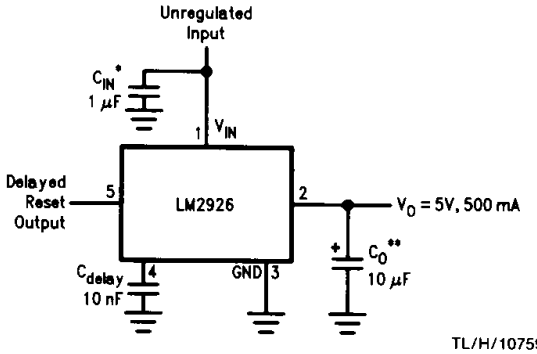
Applications

- Battery operated equipment
- Microprocessor-based systems
- Portable instruments

Typical Application

*Required if regulator is located far (>2") from power supply filter.

C_O must be at least 10 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor msut be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor is critical; see curve under **Typical Performance Characteristics.

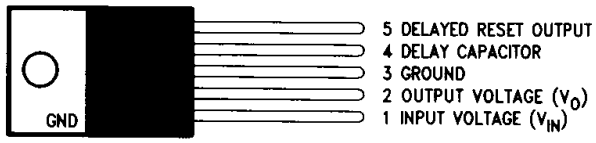


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Connection Diagrams and Ordering Information

5-Lead TO-220

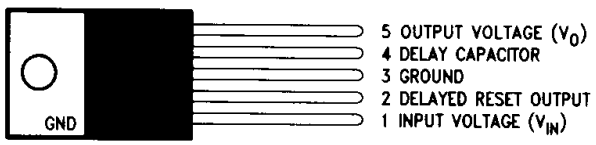
Front View
Order Number LM2926T
See NS Package Number TO5A



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5-Lead TO-220

Front View
Order Number LM2927T
See NS Package Number TO5A



TL/H/10759–14

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RRD-B20M20/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	
Survival	
t = 100 ms	80V
t = 1 ms	−50V
Continuous	−18V to +26V
Reset Output Sink Current	10 mA
ESD Susceptibility (Note 2)	2 kV
Power Dissipation (Note 3)	Internally Limited
Junction Temperature (T_{JMAX})	150°C
Storage Temperature Range	−40°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Operating Ratings (Note 1)

Junction Temperature Range (T_J)	−40°C to +125°C
Maximum Input Voltage	26V

Electrical Characteristics V_{IN} = 14.4V, C_O = 10 µF, −40°C ≤ T_J ≤ 125°C, unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	Limit (Note 5)	Units (Limit)
REGULATOR OUTPUT				
Output Voltage	5 mA ≤ I_O ≤ 500 mA, T_J = 25°C	5	4.85 5.15	V (min) V V (max)
	5 mA ≤ I_O ≤ 500 mA	5	4.75 5.25	V (min) V V (max)
Line Regulation	I_O = 5 mA, 9V ≤ V_{IN} ≤ 16V	1	25	mV mV (max)
	I_O = 5 mA, 7V ≤ V_{IN} ≤ 26V	3	50	mV mV (max)
Load Regulation	5 mA ≤ I_O ≤ 500 mA	5	60	mV mV (max)
Quiescent Current	I_O = 5 mA	2	3	mA mA (max)
	I_O = 500 mA	8	30	mA mA (max)
Quiescent Current at Low V_{IN}	I_O = 5 mA, V_{IN} = 5V	3	10	mA mA (max)
	I_O = 500 mA, V_{IN} = 6V	25	60	mA mA (max)
Dropout Voltage (Note 6)	I_O = 5 mA, T_J = 25°C	60	200	mV mV (max)
	I_O = 5 mA		300	mV (max)
	I_O = 500 mA, T_J = 25°C	350	600	mV mV (max)
	I_O = 500 mA		700	mV (max)
Short Circuit Current	V_{IN} = 8V, R_L = 1Ω	2	800 3	mA (min) A A (max)
Ripple Rejection	f_{RIPPLE} = 120 Hz, V_{RIPPLE} = 1 Vrms, I_O = 50 mA		60	dB (min)
Output Impedance	I_O = 50 mAdc and 10 mArms @ 1 kHz	100		mΩ
Output Noise	10 Hz to 100 kHz, I_O = 50 mA	1		mVrms
Long Term Stability		20		mV/1000 Hr
Maximum Operational Input Voltage	Continuous		26	V (min)

Electrical Characteristics

V_{IN} = 14.4V, C_O = 10 μF, −40°C ≤ T_J ≤ 125°C, unless otherwise specified (Continued)

Parameter	Conditions	Typ (Note 4)	Limit (Note 5)	Units (Limit)
REGULATOR OUTPUT (Continued)				
Peak Transient Input Voltage	V_O ≤ 7V, R_L = 100Ω, t_f = 100 ms		80	V (min)
Reverse DC Input Voltage	V_O ≥ −0.6V, R_L = 100Ω		−18	V (min)
Reverse Transient Input Voltage	t_r = 1 ms, R_L = 100Ω		−50	V (min)
RESET OUTPUT				
Threshold	ΔV_O Required for Reset Condition (Note 7)	−250	−80 −400	mV (min) mV mV (max)
Output Low Voltage	I_{SINK} = 1.6 mA, V_{IN} = 3.2V	0.15	 0.4	 V (max)
Internal Pull-Up Resistance		30		kΩ
Delay Time	C_{DELAY} = 10 nF (See Timing Curve)	19		ms
Minimum Operational V_{IN} on Power Up	Delayed Reset Output ≤ 0.8V, I_{SINK} = 1.6 mA, R_L = 100Ω	2.2	 3.2	V V (min)
Minimum Operational V_O on Power Down	Delay Reset Output ≤ 0.8V, I_{SINK} = 10 μA, V_{IN} = 0V	0.7		V
DELAY CAPACITOR PIN				
Threshold Difference (ΔV_{DELAY})	Change in Delay Capacitor Voltage Required for Reset Output to Return High	3.75	3.5 4.1	V (min) V V (max)
Charging Current (I_{DELAY})		2.0	1.0 3.0	μA (min) μA μA (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. **Operating Ratings** indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the **Electrical Characteristics.**

Note 2: Human body model; 100 pF discharged through a 1.5 kΩ resistor.

Note 3: The maximum power dissipation is a function of T_{JMAX}, and θ_{JA}, and T_A, and is limited by thermal shutdown. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{JMAX}-T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the device will go into thermal shutdown. For the LM2926 and LM2927, the junction-to-ambient thermal resistance is 53°C/W, and the junction-to-case thermal resistance is 3°C/W.

Note 4: Typicals are at T_J = 25°C and represent the most likely parametric norm.

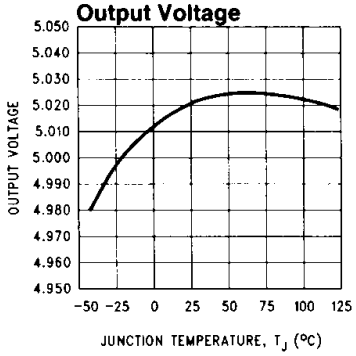
Note 5: Limits are 100% guaranteed by production testing.

Note 6: Dropout voltage is the input-output differential at which the circuit ceases to regulate against any further reduction in input voltage. Dropout voltage is measured when the output voltage (V_O) has dropped 100 mV from the nominal value measured at V_{IN} = 14.4V.

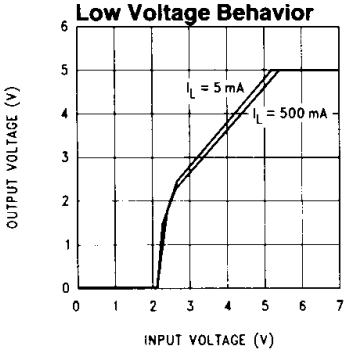
Note 7: The reset flag is set LOW when the output voltage has dropped an amount, ΔV_O, from the nominal value measured at V_{IN} = 14.4V.

Typical Performance Characteristics

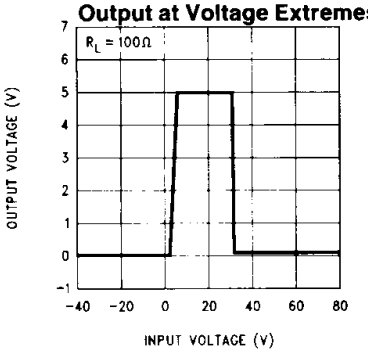
Output Voltage



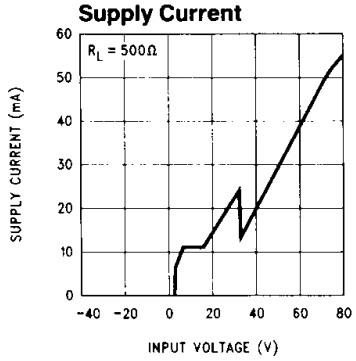
Low Voltage Behavior



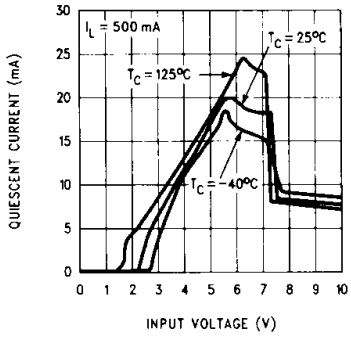
Output at Voltage Extremes



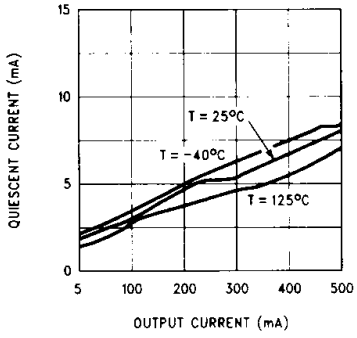
Supply Current



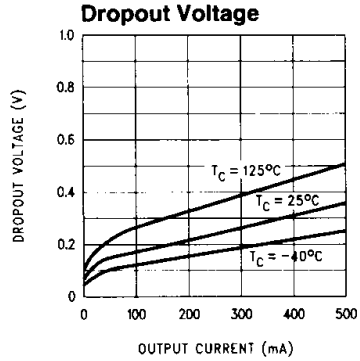
Quiescent Current



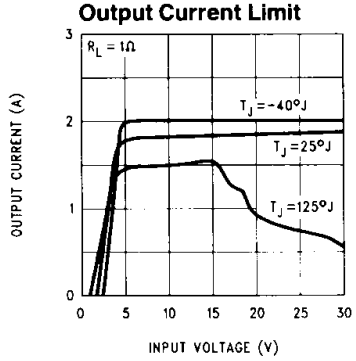
Quiescent Current



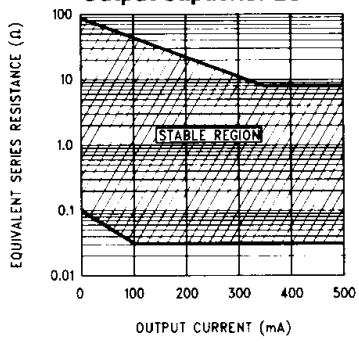
Dropout Voltage



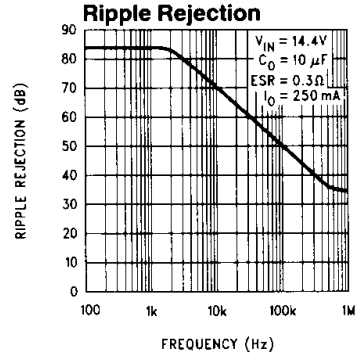
Output Current Limit



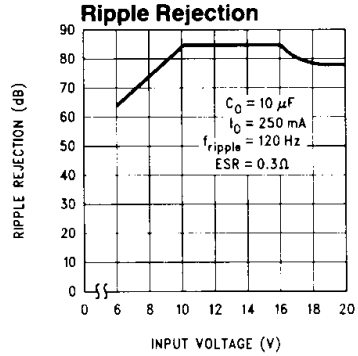
Output Capacitor ESR



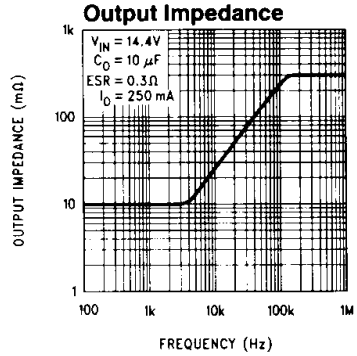
Ripple Rejection



Ripple Rejection



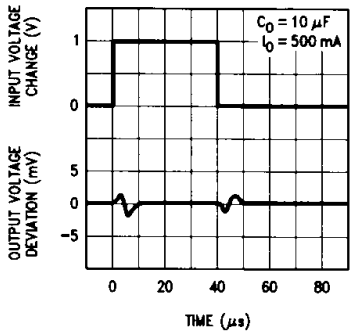
Output Impedance



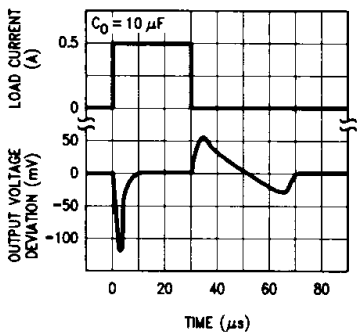
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Typical Performance Characteristics (Continued)

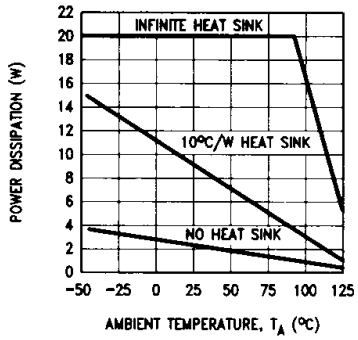
Line Transient Response



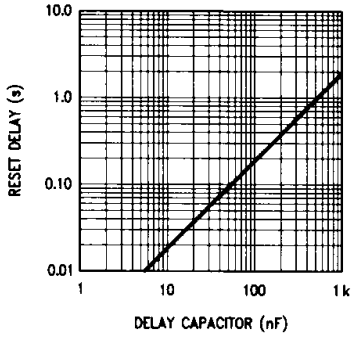
Load Transient Response



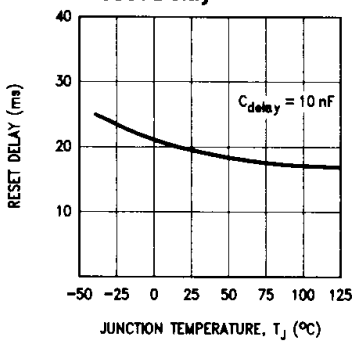
Maximum Power Dissipation (TO-220)



Reset Delay

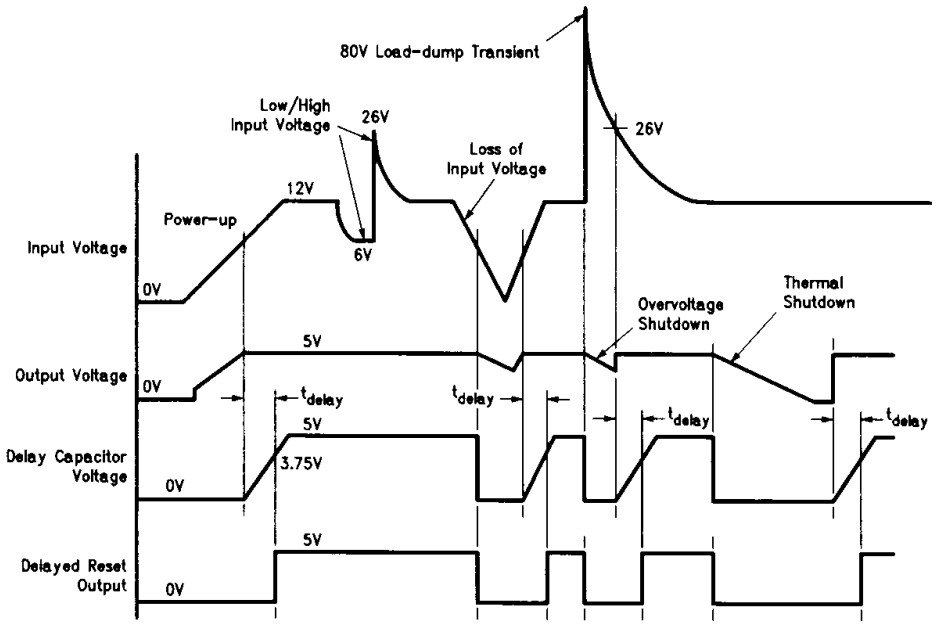


Reset Delay



TL/H/10759–4

Typical Circuit Waveforms



TL/H/10759–5

Applications Information

EXTERNAL CAPACITORS

The LM2926/7 output capacitor is required for stability. Without it, the regulator output will oscillate at amplitudes as high as several volts peak-to-peak at frequencies up to 500 kHz. Although 10 μF is the minimum recommended value, the actual size and type may vary depending upon the application load and temperature range. Capacitor equivalent series resistance (ESR) also affects stability. The region of stable operation is shown in the **Typical Performance Characteristics** (Output Capacitor ESR curve).

Output capacitors can be increased in size to any desired value above 10 μF. One possible purpose of this would be to maintain the output voltage during brief conditions of input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. Many aluminum electrolytics freeze at temperatures below $-30°C$, reducing their effective capacitance to zero. To maintain regulator stability down to $-40°C$, capacitors rated at that temperature (such as tantalums) must be used.

DELAYED RESET

The delayed reset output is designed to hold a microprocessor in a reset state on system power-up for a programmable time interval to allow the system clock and other powered circuitry to stabilize. A full reset interval is also generated whenever the output voltage falls out of regulation. The circuit is tripped whenever the output voltage of the regulator is out of regulation by the Reset Threshold value. This can be caused by low input voltages, over current conditions, over-voltage shutdown, thermal shutdown, and by both power-up and power-down sequences. When the reset circuit detects one of these conditions, the delay capacitor is discharged by an SCR and held in a discharged state by a saturated NPN switch. As long as the delay capacitor is held low, the reset output is also held low. Because of the action of the SCR, the reset output cannot glitch on noise or transient fault conditions. A full reset pulse is obtained for any fault condition that trips the reset circuit.

When the output regains regulation, the SCR is switched off and a small current (I_{DELAY} = 2 μA) begins charging the delay capacitor. When the capacitor voltage increases 3.75V (ΔV_{DELAY}) from its discharged value, the reset output is again set HIGH. The delay time is calculated by:

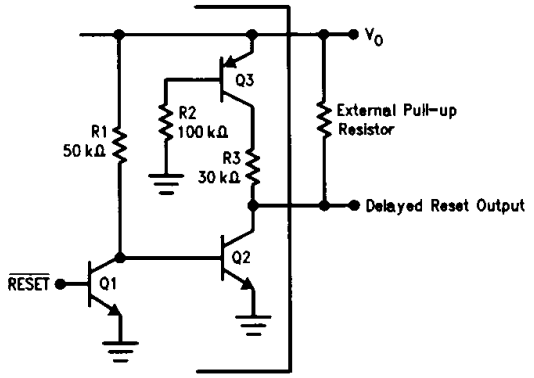
$$\text{delay time} = \frac{C_{DELAY}\,\Delta V_{DELAY}}{I_{DELAY}} \qquad (1)$$

or

$$\text{delay time} \approx 1.9 \times 10^6\, C_{DELAY} \qquad (2)$$

The constant, 1.9×10^6, has a $\pm 20\%$ tolerance from device to device. The total delay time error budget is the sum of the 20% device tolerance and the tolerance of the external capacitor. For a 20% timing capacitor tolerance, the worst case total timing variation would amount to $\pm 40\%$, or a ratio of 2.33:1. In most applications the minimum expected reset pulse is of interest. This occurs with minimum C_{DELAY}, minimum ΔV_{DELAY}, and maximum I_{DELAY}. ΔV_{DELAY} and I_{DELAY} are fully specified in the **Electrical Characteristics.** Graphs showing the relationship between delay time and both temperature and C_{DELAY} are shown in the **Typical Performance Characteristics.**

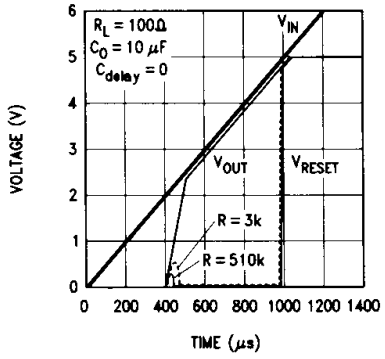
As shown in *Figure 1,* the delayed reset output is pulled low by an NPN transistor (Q2), and pulled high to V_O by an internal 30 kΩ resistor (R3) and PNP transistor (Q3). The reset output will operate when V_O is sufficient to bias Q2 (0.7V or more). At lower voltages the reset output will be in a high impedance condition. Because of differences in the V_{BE} of Q2 and Q3 and the values of R1 and R2, Q2 is guaranteed by design to bias *before* Q3, providing a smooth transition from the high impedance state when $V_O < 0.7V$, to the active low state when $V_O > 0.7V$.



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FIGURE 1. Delay Reset Output

The static reset characteristics are shown in *Figure 2.* This shows the relationship between the input voltage, the regultor output and reset output. Plots are shown for various external pull-up resistors ranging in value from 3 kΩ to an open circuit. Any external pull-up resistance causes the reset output to follow the regulator output until Q2 is biased ON. C_{DELAY} has no effect on this characteristic.



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FIGURE 2. Reset Output Behavior during Power-Up

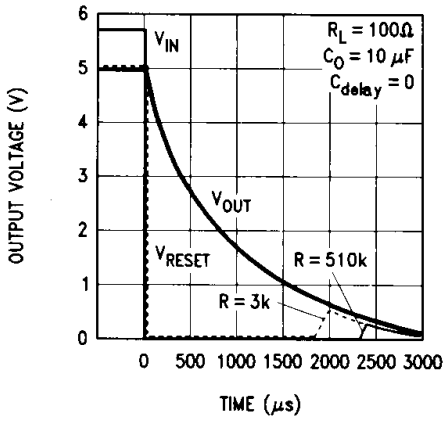
Figure 2 is useful for determing reset performance at any particular input voltage. Dynamic performance at power-up will closely follow the characteristics illustrated in *Figure 2,* except for the delay added by C_{DELAY} when V_O reaches 5V.

The dynamic reset characteristics at power-down are illustrated by the curve shown in *Figure 3.* At time t = 0 the input voltage is instantaneously brought to 0V, leaving the output powered by C_O. As the voltage on C_O decays (discharged by a 100Ω load resistor), the reset output is held low. As V_O drops below 0.7V, the reset rises up slightly should there be any external pull-up resistance. With no external resistance, the reset line stays low throughout the entire power down cycle. If the input voltage does not fall instantaneously, the reset signal will tend to follow the performance characteristics shown in *Figure 2.*

Applications Information (Continued)

SYSTEM DESIGN CONSIDERATIONS

Many microprocessors are specified for operation at 5V ±10%, although they often continue operating well outside this range. Others, such as certain members of the COPS family of microcontrollers, are specified for operation as low as 2.4V.



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FIGURE 3. Reset Output Behavior during Power-Down

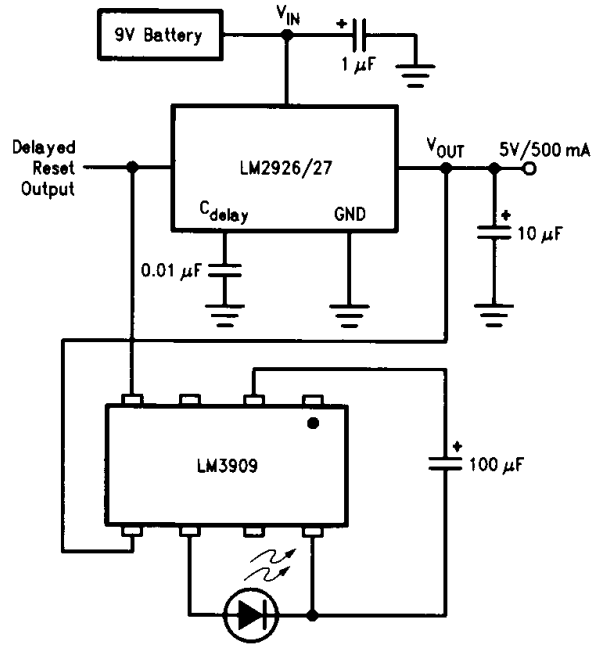
Of particular concern is low voltage operation, which occurs in battery operated systems when the battery reaches the end of its discharge cycle. Under this condition, when the supply voltage is outside the guaranteed operating range, the clock may continue to run and the microprocessor will attempt to execute instructions. If the supply voltage is outside the guaranteed operating range, the instructions may not execute properly and a hardware reset such as is supplied by the LM 2926/7 may fail to bring the processor under control. The LM2926/7 reset output may be more efficiently employed in certain applications as a means of defeating memory WRITE lines, clocks, or external loads, rather than depending on unspecified microprocessor operating conditions.

In critical applications the microprocessor reset input should be fully characterized and guaranteed to operate until the clock ceases oscillating.

INPUT TRANSIENTS

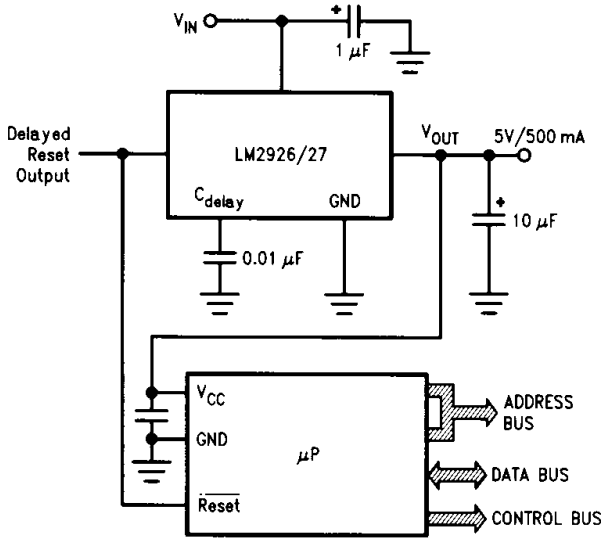
The LM2926/7 are guaranteed to withstand positive input transients to 80V followed by an exponential decay of τ = 20 ms (t_f = 100 ms, or 5 time constants) while maintaining an output of less than 7V. The regulator remains operational to 26 V_{DC}, and shuts down if this value is exceeded.

Battery Powered Regulator with Flashing LED for Low Battery Indication



TL/H/10759–9

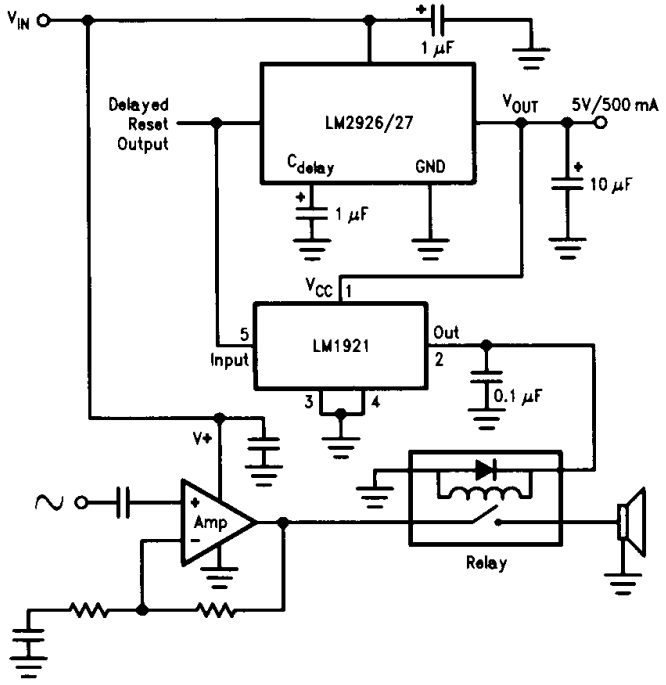
General Microprocessor Configuration



TL/H/10759–10

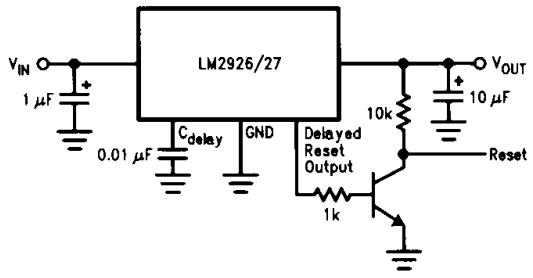
Applications Information (Continued)

Using the Reset to De-Activate Power Loads. The LM1921 is a Fully Protected 1 Amp High-Side Driver.



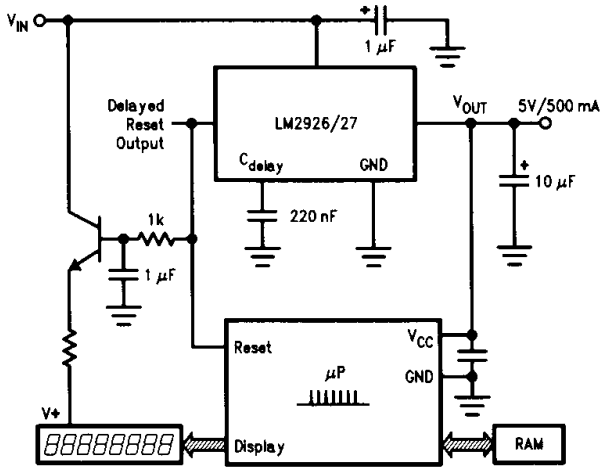
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Generating an Active High Reset Signal



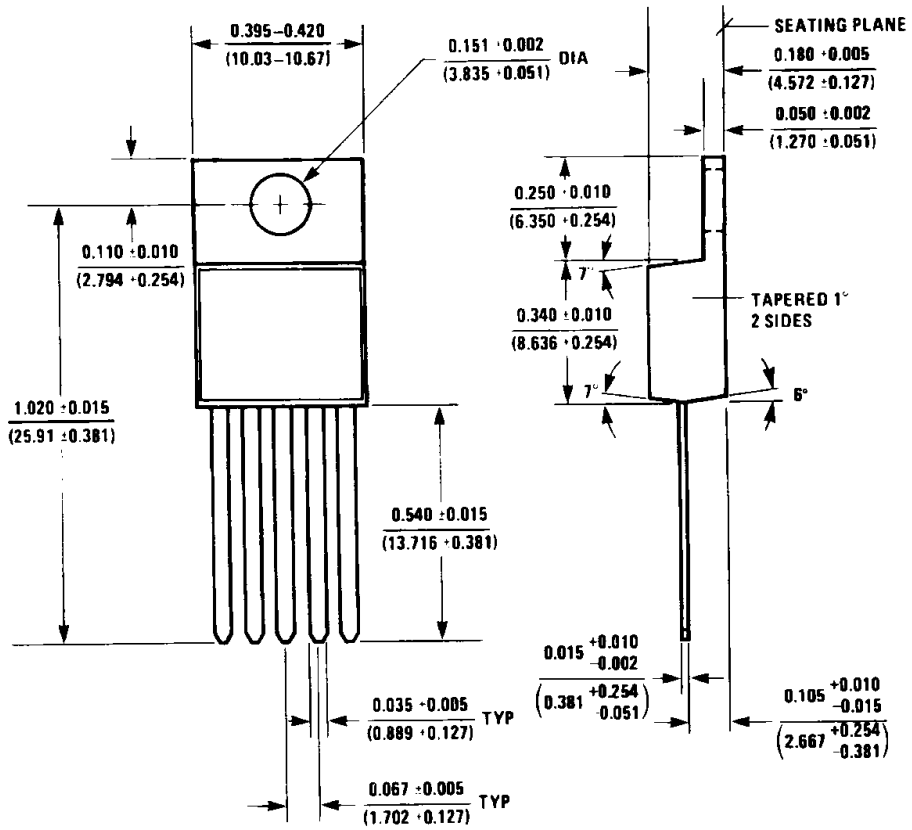
TL/H/10759–12

Using the Reset to Ensure an Accurate Display on Power-Up or Power-Down



TL/H/10759–13

Physical Dimensions inches (millimeters)



5-Lead TO-220 Outline Drawing
Order Number LM2926T or LM2927T
NS Package Number T05A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

MAR 1 2 1991

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